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A class E GaN microwave power amplifier accounting for parasitic inductance of transistor

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Abstract: The effects of parasitic inductance of transistor on finite dc-feed inductance type class E microwave power amplifier is analyzed in this letter. We find that the frequency bandwidth can be improved by fully consideration of the output parasitic inductance of transistor. To validate the method, a GaN power amplifier by using the proposed topology is designed for demonstration purpose. Experimental results show that the amplifier is realized from 2.5 GHz to 3.5 GHz (33.3%) with measured drain efficiency larger than 60%, which show good agreement with the simulated results.

Keywords: class E, power amplifier, parasitic inductance, GaN

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Broadband high efficiency power amplifier (PA) have been widely discussed in the past years [1]. The switch mode class E PA is a very good candidate for high efficiency microwave PA due to its design simplicity [2]. And the class E PA with finite dc-feed inductance is one of most popular topology [3].

As the operation frequency reaches GHz range, it is essential to take into account all the transistor's parasitic parameters for high performance power amplifier design. The consideration of parasitic inductance and capacitance of transistor can not only increase the design accuracy, but also can be used to improve the performance of class E amplifier by fully consideration [4, 5].

Most of the papers focus on the output capacitance of transistor. However, as the further increase of operation frequency, the effects of parasitic inductance of transistor can not be ignored, especially for hybrid integrated circuits [6]. In this letter, the class E power amplifier with finite dc-feed inductance and series inductance network is proposed to study the effect of the transistor's parasitic inductance.

2 Theoretical analysis

The class E amplifier with finite dc-feed inductance is used in our design, which is shown in the Fig. 1. This topology has quite high load R and can give a sufficient room for broadband amplifier design. The load network consists of transistor parasitic shunt capacitance C_0, series inductance L_{series} which include the bond-wire inductance and lead inductance, finite dc-feed inductance L_0 and series reactive element jX. The series inductance L_{series} can be considered as an adjustable parameter, and the series reactive element jX can be positive (inductance) or negative (capacitance) or zero. The active device is considered to be an ideal switch.

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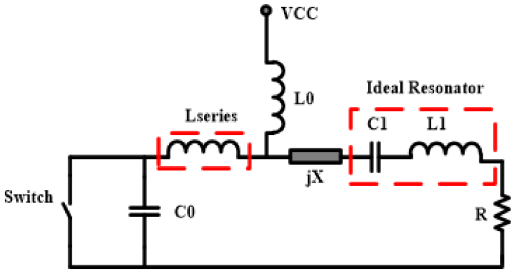
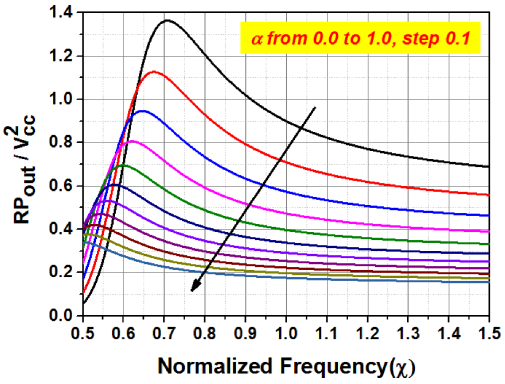


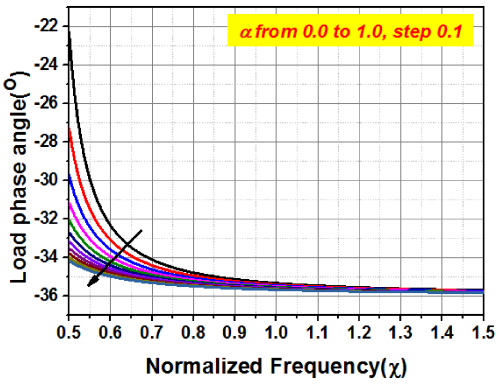
Fig. 1. Topology of the class E power amplifier with finite dc-feed inductance and series inductance network.

Let $\chi = \omega/\omega_0$ and $\alpha = L_{series}/L_0$, the normalized load RP_{out}/V_{cc}^2 versus α and χ as α is calculated and shown in Fig. 2(a), where $\omega_0 = 1/\text{sqrt}(C_0L_0)$. We can see that the normalized load RP_{out}/V_{cc}^2 has the maximum 1.3633 at $\chi = 0.709$ and $\alpha = 0$. This is the conventional topology without the consideration of parasitic inductance. And with the increasing of α, the normalized load RP_{out}/V_{cc}^2 decreases, which makes it easier to realize high efficiency matching. As a result, the series inductance L_{series} can be used one adjustable component of the load network to obtain the optimal load R.

To design broadband amplifier, it is also necessary to analyses the variation of load phase angle. The smaller variation of load phase angle, the broader frequency band can be realized. Fig. 2(b) shows load phase angle versus α and χ. It shows



(a) RP_{out}/V_{cc}^2 versus α and χ



(b) Load phase angle versus α and χ

Fig. 2. The effects of parasitic output inductance of transistor on the load network parameters of class E amplifier with the proposed topology

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that the difference of load phase angle can improve from 13.42° to 1.65° in the same frequency range ($0.5 \leq \chi \leq 1.5$) as α change from 0.0 to 1.0. This means that the proposed topology can produce a smaller total variation over a wide given frequency by fully use of the output parasitic inductance of transistor.

The output power capability C_p is also discussed here. Fig. 3 shows the calculated output power capability C_p of PA at $\alpha = 0$ and $\alpha = 1$ in frequency domain. It shows that the maximum $(C_p)_{max} = 0.1049$ when $\alpha = 0$ and $\chi = 0.6689$ and the maximum $(C_p)_{max} = 0.1049$ when $\alpha = 1$ and $\chi = 0.48$. These results show that the increase of series inductance can theoretically extend the frequency bandwidth to lower frequency without decreasing the output power capability.

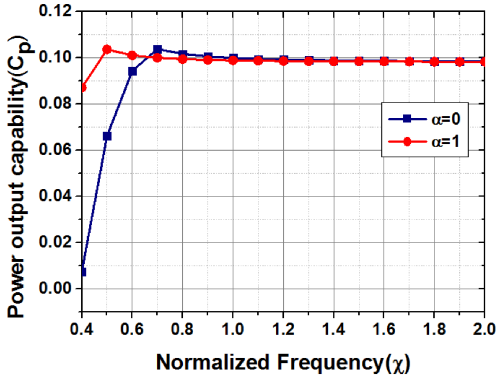

Fig. 3. Output power capability versus α and χ

3 Design of class E PA

A class E GaN PA with proposed topology is designed for demonstration purpose as shown in Fig. 4. A 0.25 µm gate length GaN HEMT with 1.25 mm total gate-width is used. In this transistor, the parasitic output capacitance C_{out} is 0.254 pF and the parasitic output inductance L_{para} is 0.15 nH [7]. The inductance L_{wire} induced by bonding wire is 0.8 nH [6]. The drain voltage $V_d = 28$ V and the center frequency $f_0 = 3.1$ GHz are selected in our design. Then, the optimal values of $\alpha = 0.58$, $\chi = 0.564$, $L_2 = 4.5$ nH and $L_3 = 9.4$ nH can be obtained from Fig. 2(a). And the value of $C_2 = 2.5$ pF can also be calculated from Fig. 2(b). The inductance L_1 and L_2 are realized by the microstrip transmission line. As shown in Fig. 8, the simulated results show that more than 60% PAE can be achieved from 2.7 GHz to 3.5 GHz and the corresponding fractional band width (FBW) is 25.8%.

In order to achieve the require transformation and provide satisfactory suppression of harmonics in the source, a two-stage cascaded low pass type transformer was implemented. Under a conjugate matching condition, to satisfy the input broadband frequency from 2.7 GHz to 3.5 GHz, the quality factor Q must be kept low, in this design, a Q of 1.5 is used. The input network is designed to match the transistor input impedance to the 50 Ω source impedance. Fig. 5(a) shows the scatter parameters of the input network, owe to the low pass character, the second harmonic and the third harmonic is suppressed, which results a faster switching operation time. In the output network, the series L_0C_0 resonant has a limited frequency response, to implement the broadband class E PA, low pass match

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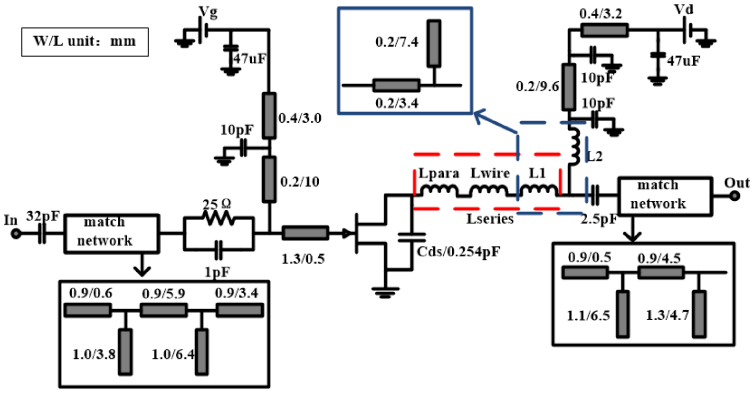
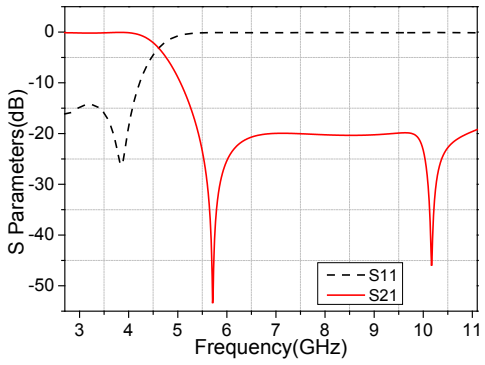
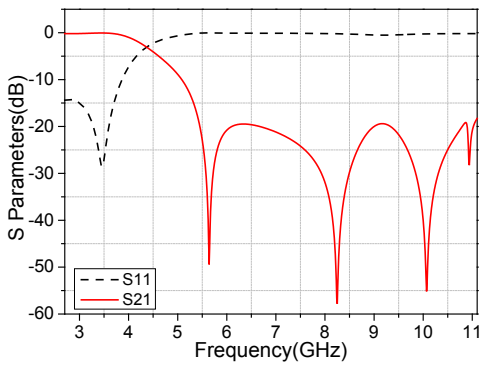


Fig. 4. Schematic of GaN class E PA with finite dc-feed inductance and series inductance network

network [9, 10] is applied to impedance matching and suppress harmonic [11]. Fig. 5(b) shows the scatter parameters of the output network, it can be seen that the second harmonic and the third harmonic is controlled.



(a) Input match network



(b) Output match network

Fig. 5. Input/output match network and harmonic suppression

4 Results and discussion

The photo of fabricated GaN class E PA is shown in Fig. 6. The input/output matching is realized by low pass filter.

Fig. 7 shows the comparison of simulated and measured drain efficiency (DE), power added efficiency (PAE), output power (Pout) and Gain versus input power at 3.1 GHz at continuous wave (CW) input signal, the maximum PAE is 63.4% when

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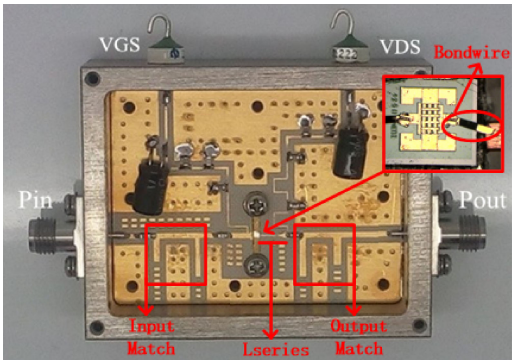

Fig. 6. Photo of fabricated GaN class E hybrid PA

the input power is 28 dBm at $V_d = 28$ V, $V_g = -2.5$ V. Very good agreement has been achieved.

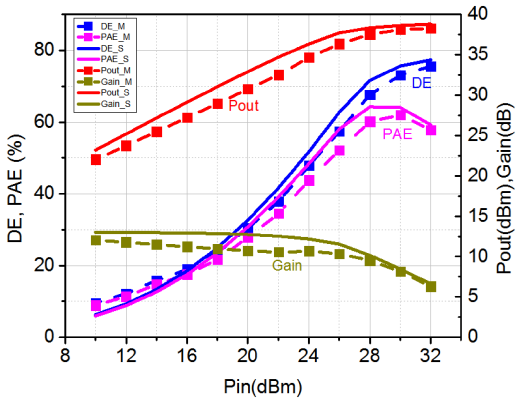

Fig. 7. Comparison of simulated and measured DE, PAE, Pout and Gain versus input power at 3.1 GHz

Fig. 8 shows the comparison of simulated and measured DE, PAE, Pout and power gain according to operating frequency at the input power of 27 dBm ($V_d = 28$ V, $V_g = -2.5$ V). It can be seen that, DE is large than 60%, the output power gain is large than 8.2 dB, and the output power is more than 35.2 dBm in the frequency range of 2.5 GHz and 3.5 GHz (33.3% (FBW)). The deviation of the simulated and measured is probably due to the larger inductance of the bold wire.

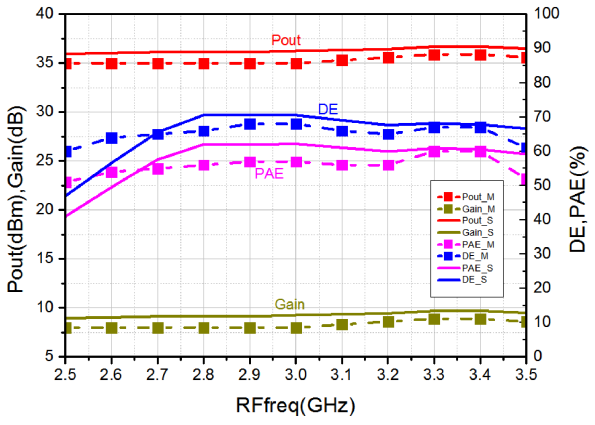

Fig. 8. Comparison of simulated and measured DE, PAE, P_{out} and Gain in 2.5~3.5 GHz

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5 Conclusion

This paper presented a class E GaN power amplifier with fully consideration of parasitic series inductance of transistor. Theoretical analytic results suggests that the proposed topology can be used to extend frequency bandwidth of class E PA. A GaN HEMT class E PA has been fabricated and the experimental data shows good agreement with the simulated results. The results of paper can be useful for class E microwave power amplifier.

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