ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.14, No.9, 1–11

An up-conversion TV receiver front-end with noise canceling body-driven pMOS common gate LNA and *LC*-loaded passive mixer

Donggu Im[1] **and Ilku Nam**[2a)]

[1] *Division of Electronics Engineering, Chonbuk National University, Jollabuk-do 561–756, Korea*

[2] *Dept. of EE and also with PNU-LG Smart Control Center, Pusan National University, Busan 609–735, Korea*

a) *nik@pusan.ac.kr*

Abstract: A low noise and highly linear up-conversion digital TV (DTV) receiver front-end, which consists of a noise canceling body-driven pMOS common gate (CG) LNA, a *LC*-loaded passive mixer, and a surface acoustic wave (SAW) driver, is implemented in a 0.18 µm CMOS process. The pMOS input stage and body-driven technique in the conventional noise canceling capacitively cross-coupled (CCC) CG LNA greatly improve noise figure (NF) over DTV frequency band without extra power consumption. The linearity of the proposed up-conversion *LC*-loaded passive mixer and modified source follower-based SAW driver is high enough to handle strong blockers without suffering from desensitization. The designed RF front-end shows a measured conversion gain of greater than 17 dB, a NF of less than 2.7 dB, and a third-order input-referred intercept point (IIP3) of greater than −2.7 dBm over DTV frequency band. The power consumption of the proposed RF front-end is 70 mW at a 1.8 V supply voltage.

Keywords: body-driven, CMOS, front-end, passive mixer, SAW driver, TV receiver, up-conversion, wideband

Classification: Integrated circuits

References

[1] J.-M. Stevenson, *et al.*: "A multi-standard analog and digital TV tuner for cable and terrestrial applications," IEEE ISSCC Dig. Tech. Papers (2007) 210 (DOI: 10.1109/ISSCC.2007.373368).

[2] G. Retz and P. Burton: "A CMOS up-conversion receiver front-end for cable and terrestrial DTV applications," IEEE ISSCC Dig. Tech. Papers (2003) 442 (DOI: 10.1109/ISSCC.2003.1234378).

[3] K. Stadius, *et al.*: "A cable-modem RF tuner," IEEE European Solid-State Circuits Conference (2003) 421 (DOI: 10.1109/ESSCIRC.2003.1257162).

[4] M. Dawkins, *et al.*: "A single-chip tuner for DVB-T," IEEE J. Solid-State Circuits **38** (2003) 1307 (DOI: 10.1109/JSSC.2003.814436).

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

[5] I. Mehr, *et al.*: "A dual-conversion tuner for multi-standard terrestrial and cable reception," IEEE Symposium on VLSI Circuits (2005) 340 (DOI: 10.1109/VLSIC.2005.1469400).
[6] I. Mehr: "Integrated TV tuner design for multi-standard terrestrial reception," IEEE Radio Frequency Integrated Circuits Symposium (2005) 75 (DOI: 10.1109/RFIC.2005.1489504).
[7] C. Ling, *et al.*: "A low-power integrated tuner for cable telephony applications," IEEE J. Solid-State Circuits **37** (2002) 1757 (DOI: 10.1109/JSSC.2002.804335).
[8] Y.-S. Youn, *et al.*: "A 1 GHz-band low distortion up-converter with a linear in dB control VGA for digital TV tuner," IEEE Radio Frequency Integrated Circuits Symposium (2001) 257 (DOI: 10.1109/RFIC.2001.936252).
[9] D. Im and I. Nam: "A wideband digital TV receiver front-end with noise and distortion cancellation," IEEE Trans. Circuits Syst. I, Reg. Papers **61** (2014) 562 (DOI: 10.1109/TCSI.2013.2278386).
[10] D. Saias, *et al.*: "A 0.12 µm CMOS DVB-T tuner," IEEE ISSCC Dig. Tech. Papers (2005) 430 (DOI: 10.1109/ISSCC.2005.1494053).
[11] G. D. J. Smit, *et al.*: "RF-noise modeling in advanced CMOS technologies," IEEE Trans. Electron Devices **61** (2014) 245 (DOI: 10.1109/TED.2013.2282960).
[12] M. El-Nozahi, *et al.*: "An inductor-less noise-cancelling broadband low noise amplifier with composite transistor pair in 90 nm CMOS technology," IEEE J. Solid-State Circuits **46** (2011) 1111 (DOI: 10.1109/JSSC.2011.2118310).
[13] Z. Liang: "Low-voltage bulk-driven amplifier design and its application in implantable biomedical sensors," Ph.D Dissertation, University of Tennessee, Knoxville (2012).
[14] A. Kumar, *et al.*: "Bulk driven circuits for low voltage applications," J. Active Passive Electron. Devices **8** (2009) 237.
[15] H. L. Kao, *et al.*: "Limiting factors of RF performance improvement as down-scaling to 65-nm node MOSFETs," Korea-Japan Micro-Wave Conference (2009).
[16] B. Razavi: *RF Microelectronics* (Prentice Hall, Upper Saddle River, NJ, 2011) 2nd ed. 960.

1 Introduction

A low noise and highly linear up-conversion receiver front-end is an essential building block for the dual (up and down) conversion digital TV (DTV) tuner because it dominates the receiver performance. With the help of the surface acoustic wave (SAW) bandpass filter (BPF), it provides more robust local oscillator (LO) harmonic rejection and interference suppression without highly sophisticated calibration process in comparison with the harmonic rejection mixer-based single conversion receiver.

The up-conversion receiver front-end usually consists of a wideband low noise amplifier (LNA) and an up-conversion mixer. In previously published works in [1, 2, 3, 4, 5, 6, 7, 8, 9], all of them adopted the Gilbert double-balanced active mixer with *LC* tank load. The impedance of *LC* tank load was matched to the termination impedance of SAW BPF. It is well known that the Gilbert active mixer provides decent gain, adequate single-sideband (SSB) noise figure (NF) in the range of 6∼12 dB, and very good port isolation. However, the third-order intercept

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

point (IP3) of the active mixer is severely limited by the input transconductance (g_m) stage. The large bias current and inductive source degeneration can improve IP3 of the mixer with low noise performance, but these are not desirable solutions because of heavy power consumption and costly chip area. In addition, the bandwidth of the inductive source degenerated mixer is not wide enough to cover DTV frequency band. In [9], the up-conversion micromixer adopting the third-order intermodulation (IM3) distortion cancellation was proposed to improve the linearity of the active mixer with low power consumption over a wide operating frequency range. The linearity improvement by the proposed linearization method was quite considerable and robust to process and temperature variations. However, because g_{m3}, the second derivative of the transconductance, is close to zero over a relatively narrow input voltage range, the distortion cancellation becomes valid up to a certain input power level. This insufficient large-signal linearity performance desensitizes the front-end circuit in the stringent RF interference environment. On the other hand, the current commutating passive mixer is a good candidate for up-conversion mixer because of very good small- and large-signal linearity, zero current consumption, and small area. However, the conversion loss of the passive mixer should be compensated by the preceding stage of LNA, and the highly linear SAW driver is required for the impedance matching with SAW BPF. Unfortunately, there is almost no study on the passive mixer-based up-conversion receiver front-end except [10], while most of previous works have focused on the receiver front-end employing the Gilbert active mixer.

Concerning a wideband LNA, various topologies such as cascoded and degenerated differential-pair LNA in [1] and [3], shunt feedback LNA in [2], [5] and [6], common gate-common source (CG-CS) balun LNA in [4], and noise canceling capacitively cross-coupled (CCC) CG LNA in [9] and [10] have been devised for DTV applications. Among them, the noise canceling LNA involving a CG amplifier and a CS amplifier like those in [9] and [10] is suitable for the passive mixer-based up-conversion receiver front-end because it can directly drive low impedance load without requiring additional inter-stage buffer. However, the noise canceling LNAs reported in [9] and [10] still suffer from higher NF than 3 dB. Especially, at low frequency around 100 MHz, the NF increases to 4.5 dB due to the $1/f$ noise of the nMOS device.

In this paper, we propose a low noise and highly linear up-conversion receiver front-end satisfying the stringent noise and linearity requirements for the DTV tuner. The proposed noise canceling CCC CG LNA with body-driven pMOS input stage greatly improves NF over DTV frequency band, especially in the VHF frequency band, without excess power consumption in comparison with conventional noise canceling LNA in [10]. This paper firstly proves that the body-driven pMOS transistor is more suitable to achieve low noise in designing LNA for DTV applications in comparison with nMOS counterpart. The *LC*-loaded up-conversion passive mixer and the SAW driver show a sufficiently high linearity and as a result meet the stringent selectivity patterns in various DTV specifications.

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

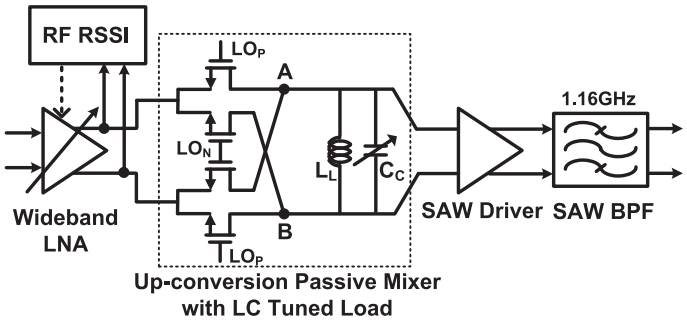

Fig. 1. Up-conversion receiver front-end employing passive mixer for the dual (up and down) conversion DTV tuner.

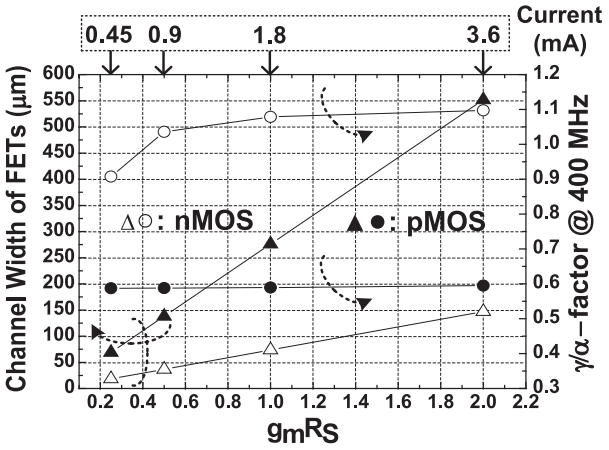

Fig. 2. Simulated γ/α-factor of nMOS and pMOS versus the value of g_mR_S in the adopted process technology. In the simulation, the channel length of all MOSFETs was 0.18 μm and the gate-to-source voltage and source-to-gate voltage of nMOS and pMOS was kept at 0.6 and 0.62 V, respectively. The source impedance R_S is 50 Ω.

2 Noise canceling body-driven pMOS CG LNA

Fig. 1 shows the block diagram of the up-conversion receiver front-end employing passive mixer for the dual conversion DTV tuner. It is composed of a wideband LNA, an up-conversion passive mixer, and a SAW driver. The proposed RF front-end converts the input signal ranging from 54 to 882 MHz to an intermediate frequency of 1.16 GHz. The RF SAW BPF is driven by the highly linear SAW driver with stable output impedance to minimize the degradation of the insertion loss and reduce the ripple in the passband by the impedance mismatch.

Fig. 2 shows the simulated γ/α-factor of nMOS and pMOS versus the value of g_mR_S at 400 MHz in the adopted process technology. Here, g_m and R_S are the transconductance and source impedance, respectively. Interestingly, the γ/α-factor of pMOS is less than two thirds of that of nMOS under the same current consumption. Also, the γ/α-factor of pMOS reported in [11, 12] is less than that of nMOS. The channel width of pMOS is much bigger than that of nMOS in order to have identical g_m under the same current consumption, and this makes it difficult for the pMOS circuit to work at high frequencies. However, over DTV frequency

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

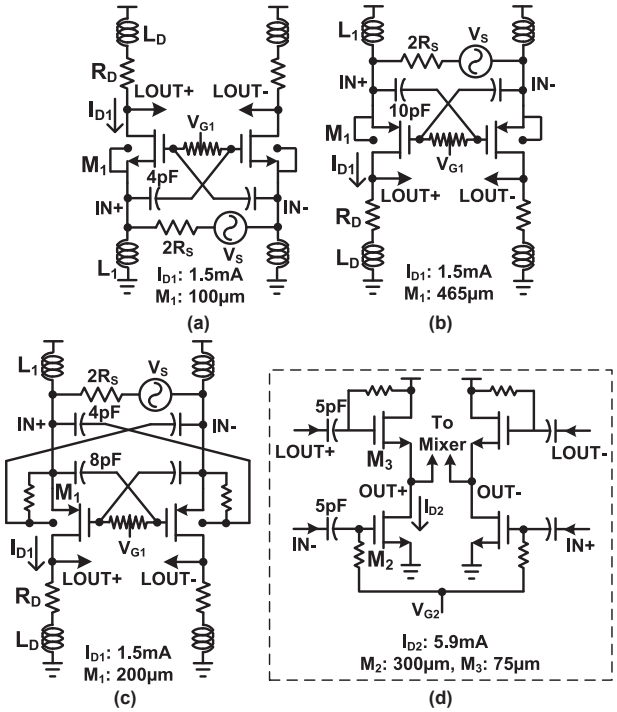

Fig. 3. Capacitively cross-coupled (CCC) common gate (CG) LNA with (a) nMOS input transistor, (b) pMOS input transistor, and (c) body-driven pMOS input transistor. Each complete LNA includes the summing stage of Fig. 3(d) for the noise cancellation. The values of L_1, L_D, R_D, and R_S in all LNAs are 200 nH, 15 nH, 600 Ω, and 25 Ω, respectively.

band below 1 GHz, the amplifier with pMOS input transistor can achieve lower NF than the amplifier with nMOS input transistor while showing reasonably high gain.

Figs. 3(a), (b), and (c) show the noise canceling CCC CG LNA with nMOS input transistor, pMOS input transistor, and body-driven pMOS input transistor, respectively. Each complete LNA includes the summing stage of Fig. 3(d) for the noise cancellation. The summing stage is capable of directly driving the up-conversion passive mixer with low input impedance while maintaining a reasonably high voltage gain of the LNA. The noise canceling CCC CG LNA with nMOS input transistor was already reported in [10]. Under the input-matched condition, their noise factors (F) are given as

$$\begin{aligned} F &= 1 + EF_{M1} + EF_{ETC} \\ &= 1 + \frac{1}{2}(\gamma_1/\alpha_1)\frac{[g_{m2}/(2g_{m1}) - g_{m3}R_D]^2}{[g_{m3}R_D + 0.5(g_{m2}/g_{m1})]^2} \\ &\quad + \frac{2}{g_{m1}}\frac{[(\gamma_2/\alpha_2)g_{m2} + (\gamma_3/\alpha_3)g_{m3} + R_D{g_{m3}}^2]}{[g_{m3}R_D + 0.5(g_{m2}/g_{m1})]^2} \end{aligned} \quad (1)$$

where the excess noise factor EF_{M1} and EF_{ETC} denote the noise contribution of the input transistor M_1 and the rest of the components (M_2, M_3, and R_D) and $g_{mn(n=1,2,3)}$ and $(\gamma/\alpha)_{n(n=1,2,3)}$ are the transconductance and γ/α-factor, respectively, of transistors M_1, M_2, and M_3. The channel thermal noise current from the input transistor M_1 is wholly canceled out at the LNA output when g_{m2} is equal to $2g_{m1}g_{m3}R_D$, but it is very difficult to meet this condition with reasonably high gain due to the

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

Table I. Design parameters of noise canceling CCC CG LNAs

	g_{m1} (mS)	g_{m2} (mS)	g_{m3} (mS)	$(\gamma_1/\alpha_1)/(\gamma_2/\alpha_2)/(\gamma_3/\alpha_3)$
Fig. 3(a)	20	72	32	1.079/1.079/1.079
Fig. 3(b)				0.589/1.079/1.079

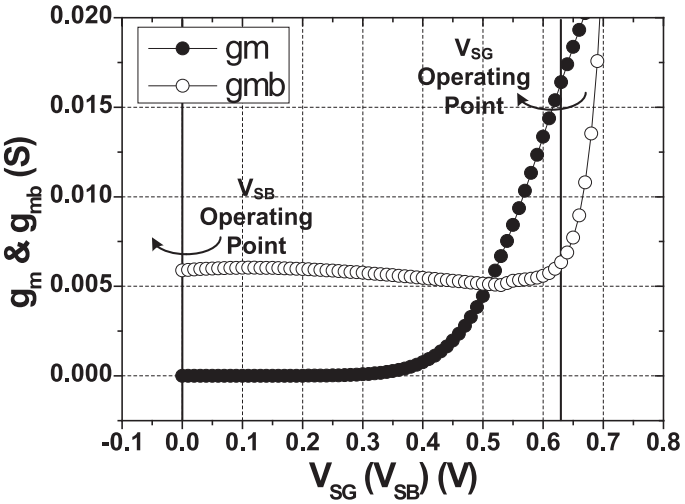

Fig. 4. Simulated g_m and bulk transconductance (g_{mb}) of pMOS transistor with the channel width of 200-μm according to the variation of source-to-gate voltage (V_{SG}) and source-to-body voltage (V_{SB}). The dc operating points of V_{SG} and V_{SB} in the proposed LNA of Fig. 3(c) are 0.63 and 0 V, respectively.

limitation of power consumption and operating bandwidth. Therefore, using the pMOS transistor with a smaller γ/α-factor as the input transconductance stage of the LNA can reduce the NF of the LNA without excess power consumption.

Table I summarizes the design parameters of the aforementioned noise canceling CCC CG LNAs under the same current consumption. The channel width of the input transistor described in Fig. 3 was chosen to meet the condition of $g_{m1} = (0.5/R_S)$ for the input-matched condition. The calculated EF_{M1} and EF_{ETC} of Fig. 3(a) are 0.369 and 0.163, respectively; those of Fig. 3(b) are 0.201 and 0.163, respectively. The calculated NF of the noise canceling CCC CG LNA with nMOS and pMOS input transistors are 1.85 and 1.35 dB, respectively. The NF of 0.5 dB can be improved without extra power consumption.

One major drawback of the noise canceling CCC CG LNA with pMOS input transistor is the bandwidth reduction due to large parasitic capacitances. Fig. 3(c) shows the proposed noise canceling CCC CG LNA with body-driven pMOS input transistor to overcome the drawback of the bandwidth reduction. The bulk transconductance g_{mb} can be derived by taking derivatives of the drain current (I_D) to body-to-source voltage (V_{BS}) and given as

$$g_{mb} \simeq \left| -\beta(V_{SG} - V_{THP0} - \gamma_p(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F}))\frac{\gamma_p}{2\sqrt{2\phi_F + V_{BS}}} \right| \simeq g_m \frac{\gamma_p}{2\sqrt{2\phi_F + V_{BS}}} \simeq g_m \eta \quad (2)$$

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

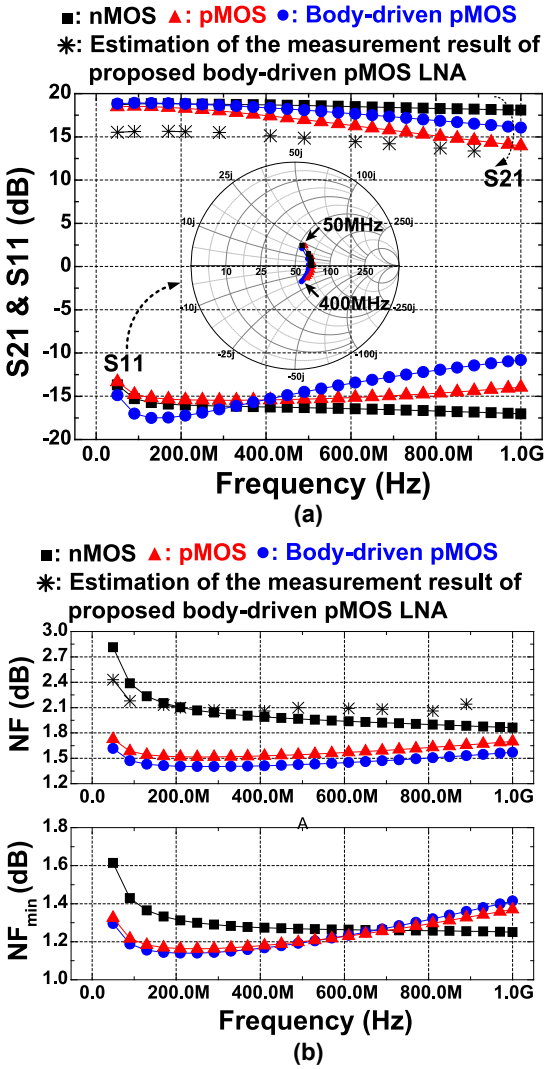

Fig. 5. Comparison of simulated (a) power gain (S_{21}) and input reflection coefficient (S_{11}) and (b) noise figure (NF) and minimum noise figure (NF_{min}) of the aforementioned noise canceling CCC CG LNAs in Fig. 3. In the simulation, the source impedance ($2R_S$) is 50 Ω. The estimation of the measurement result of the proposed body-driven pMOS LNA is added for the comparison with the simulation result.

where V_{THP0} is the threshold voltage of pMOS at zero substrate voltage, φ_F is the bulk Fermi potential, γ_P is a constant describing the substrate bias effect, and V_{SG} is the fixed source-to-gate voltage [13, 14]. Fig. 4 presents the simulated g_m and g_{mb} of pMOS transistor with the channel width of 200-μm according to the variation of source-to-gate voltage (V_{SG}) and source-to-body voltage (V_{SB}) in the adopted CMOS technology. At the dc operating points, the simulated ratio η ($= g_{mb}/g_m$) is about 0.36. By injecting the input differential signals to the body nodes of the input pMOS transistors, the effective g_m is increased by about 36 percent without extra power consumption. This reduces the channel width of pMOS input transistor for the input-matched condition and improves the bandwidth of the LNA.

Fig. 5 presents the simulated power gain (S_{21}), input reflection coefficient (S_{11}), noise figure (NF), and minimum noise figure (NF_{min}) of the aforementioned noise canceling CCC CG LNAs in Fig. 3 under the same current consumption. The

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

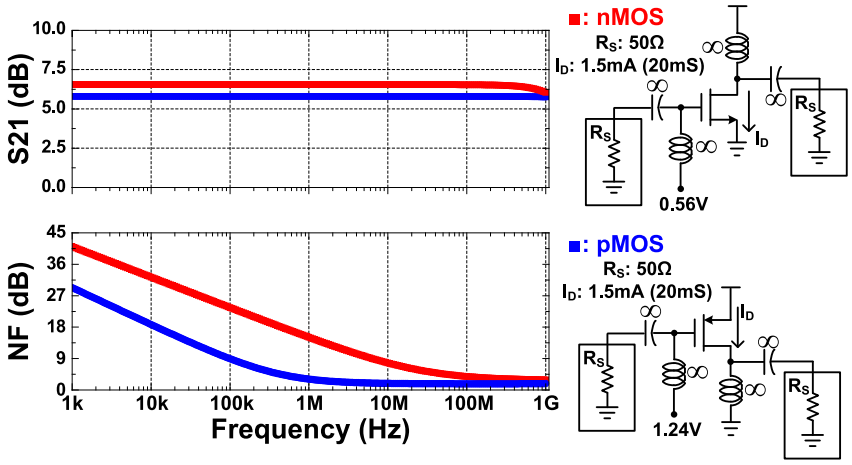

Fig. 6. Simulated $1/f$ noise of both nMOS and pMOS.

identical design parameters denoted in Fig. 3 and Table I were used for the simulation. The shunt peaking inductor L_D was added in series with the load resistor R_D to achieve wider bandwidth of the LNA. The external RF choke inductor L_1 was used for low noise and high linearity performance. In the simulation, all LNAs showed S_{11} of under -10 dB over the operating frequency. The simulated NF matched the calculated NF well. In the saturation region for MOSFETs, $\mathrm{NF_{min}}$ can be approximated as

$$\mathrm{NF_{min}} \simeq 1 + 2\frac{f}{f_t}\sqrt{\left(\frac{\gamma}{\alpha}+\frac{4}{15}\right)\left(\frac{\gamma}{\alpha}+g_m R_g\right)}, \tag{3}$$

where R_g is the dominant gate resistance and f_t is the unit-gain cutoff frequency [15]. As shown in the simulation result, $\mathrm{NF_{min}}$ of the CCC CG LNA with pMOS and body-driven pMOS input transistor is lower than that of the LNA with nMOS input transistor from 54 to 700 MHz. However, due to smaller f_t of pMOS transistor, $\mathrm{NF_{min}}$ of the proposed LNA is gradually degraded as the operating frequency increases. In case of the CG wideband amplifier, it cannot satisfy $\mathrm{NF_{min}}$ over wide frequency range because the input matching network for the optimum source reflection coefficient is not available under the restriction of wideband impedance matching. Therefore, NF itself is more important than $\mathrm{NF_{min}}$. In comparison with the CCC CG LNA with nMOS input transistor, the proposed LNA improves NF by 0.6 dB at 400 MHz under the same power consumption only by adopting the body-driven pMOS transistor as the input transconductance stage, while showing similar S_{21} and S_{11}. In conclusion, the improvement of NF comes from better noise characteristic (smaller γ/α-factor) of pMOS device. Fig. 6 shows the simulated $1/f$ noise of both nMOS and pMOS. The identical size and bias condition with those in the noise canceling CCC CG LNAs were used for the simulation. Because pMOS transistor exhibits less $1/f$ noise than nMOS transistor, the amount of NF improvement is significant at lower frequencies below 100 MHz.

3 *LC*-loaded up-conversion passive mixer and SAW driver

The simplified schematic of the double-balanced passive mixer with an on-chip *LC*-tuned load and SAW driver are presented in Figs. 1 and 7, respectively. The

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

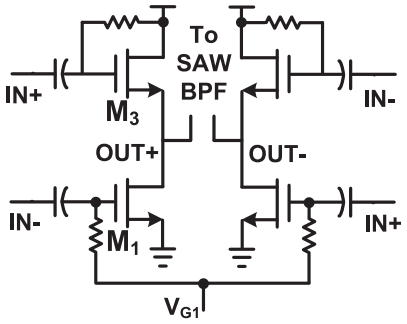

Fig. 7. Simplified schematic of SAW driver.

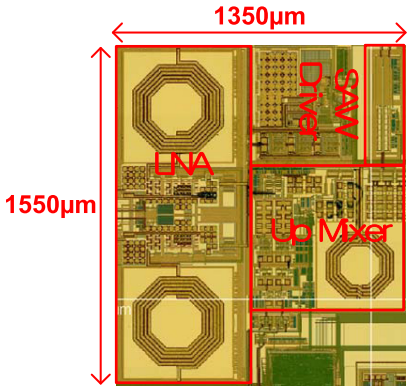

Fig. 8. Chip photograph of the proposed up-conversion receiver front-end.

up-conversion double-balanced passive mixer consists of four nMOS switching transistors, on-chip *LC*-tuned load, and three-stage inverter-based LO buffers for the generation of differential LO signals.

The bandwidth at nodes *A* and *B* should be greater than the intermediate frequency (IF) of the up-converted signal in order to minimize the degradation of the conversion gain of the passive mixer [16]. Because the on-resistance of the switching transistors and the parasitic capacitance at nodes *A* and *B* limit the bandwidth, the on-chip inductor L_L is used to cancel the parasitic capacitance at nodes *A* and *B* through the resonance. In addition, the 6-bit switched capacitor array C_C is added in order to tune the center frequency of the *LC*-load, and it is controlled through an external I2C. The out-of-band filtering and passive amplification of the *LC*-load result in a high linearity of the up-conversion front-end circuit.

The SAW driver with a differential output impedance of 100 Ω is employed as the impedance transformer to minimize the degradation of the insertion loss and reduce the ripple in the passband by the impedance mismatch with SAW BPF. The channel width of M_3 is set equal to that of M_1, and the value of g_{m3} is chosen as 20 mS for impedance matching with SAW BPF because the output impedance R_{out} of the proposed SAW driver is approximately $2/g_{m3}$.

4 Experimental results

The proposed up-conversion receiver front-end was implemented in a 0.18 μm CMOS process. Fig. 8 shows a chip photograph of the proposed up-conversion

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

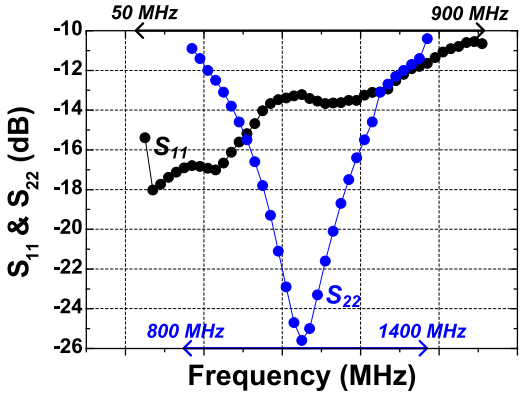

Fig. 9. Measured input and output reflection coefficients (S_{11} and S_{22}) of the proposed up-conversion receiver front-end.

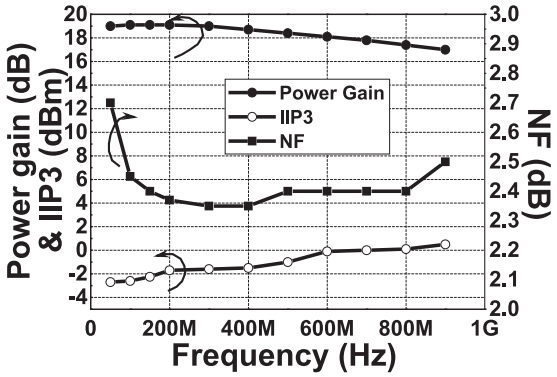

Fig. 10. Measured conversion gain, NF, and IIP3 of the proposed up-conversion receiver front-end.

receiver front-end. It consumes approximately 39 mA at a supply voltage of 1.8 V. A wideband 1:1 balun of M/A-COM's MABA-007871 was used at the input port for the differential operation during the test. The insertion loss of the input balun was de-embedded for the measurement of the conversion gain and NF of the receiver front-end. At the output port, the lumped-element *LC-CL* balun was constructed for the differential-to-single conversion.

As shown in Fig. 9, the measured S_{11} is less than −10 dB over DTV frequency band, and output impedance matching is achieved at an IF of 1160 MHz. Fig. 10 shows the measured conversion gain, NF, and IIP3 of the proposed up-conversion receiver front-end. The input frequency was swept from 54 to 882 MHz while converting a constant IF of 1160 MHz. The conversion gain of greater than 17 dB and NF of less than 2.7 dB were achieved over DTV frequency band in the measurement. Two-tone test for the intermodulation distortion (IMD) measurement was performed over DTV frequency band. The tone spacing was 6 MHz and the power level of the applied two tones was −30 dBm. The designed front-end shows the measured IIP3 of −2.7∼+0.5 dBm as shown in Fig. 10.

Because the proposed up-conversion front-end was developed in a part of the whole DTV receiver and there was no test pattern to measure the LNA only, the output of the LNA cannot be directly measured in this work. Based on the measurement data of the whole up-conversion front-end and the simulation data

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017

Table II. Measurement summary and comparison with previous works

	[2]	[3]	[9]	This Work
Frequency (MHz)	47–860	47–862	54–882	54–882
Architecture	Up-conversion receiver front-end			
Gain (dB)	20	23.5	23	17~19.1
NF (dB)	5.7	7.1	<4	<2.7
IIP3 (dBm)	−5.1	−10.5	−6.5~−4.5	−2.7~0.5
Current Consumption (mA)	39.4 @ 3.3 V	49 @ 5 V	27 @ 1.5 V	38.8 @ 1.8 V
Technology	180 nm CMOS	0.9 µm SiGe	130 nm CMOS	180 nm CMOS

of the up-conversion mixer and SAW driver, the estimation of the measurement result of the proposed body-driven pMOS LNA is done and reported in Fig. 5. There is a slight difference between estimation and simulation results due to the de-embedding error and imperfect estimation process.

Table II summarizes and compares the performance of the proposed receiver front-end against other previous works. Due to the NF improvement by the adoption of body-driven pMOS input stage in the noise canceling CCC CG LNA, the proposed up-conversion receiver front-end shows lower NF compared to previous works while having similar gain and power consumption. In addition, in terms of mixer topology, the up-conversion passive mixer followed by the proposed highly linear SAW driver leads to higher IIP3 of the front-end in comparison with previous works employing the Gilbert active mixer.

5 Conclusions

This paper firstly proves that the adoption of the body-driven pMOS input stage is more desirable for low noise in designing wideband LNA for DTV applications. The proposed noise canceling CCC CG LNA with body-driven pMOS input stage greatly improves NF over DTV frequency band, especially in the VHF frequency band, without excess power consumption. The *LC*-loaded up-conversion passive mixer followed by the highly linear SAW driver results in better IIP3 of the receiver front-end than previous designs employing the Gilbert active mixer, while maintaining other performances.

Acknowledgments

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2015R1C1A1A02037679).

DOI: 10.1587/elex.14.20170175
Received February 27, 2017
Accepted April 3, 2017
Publicized April 17, 2017
Copyedited May 10, 2017