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140 GHz power amplifier based on 0.5 µm composite collector InP DHBT

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Abstract: This paper presents a high gain, medium power amplifier for D band application based on 0.5 µm composite collector InP double hetero-junction bipolar transistor (DHBT) process. The power amplifier has four ways that combined with a T-junction power combiner. And each way has four stages HBT to provide a high gain performance. The measurement results demonstrate a peak gain of 23.6 dB at 75 GHz and at 140 GHz the gain is 21.89 dB. The saturation output power is 13.7 dBm at 140 GHz with DC power consumption 250 mW.

Keywords: InP DHBT, composite collector, power amplifier, millimeter-wave

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

As an atmospheric window in submillimeter wave band, 140 GHz is a promising frequency for imaging, radar, and communications systems [1, 2]. Power amplifier (PA) is the key component in submillimeter wave system for the output power determined the operation distance, ability of anti-interference, and communication quality. Recently, massive D-band (110∼170 GHz) PA are presented [3, 4, 5, 6, 7, 8] indicated a great attention has been paid in this field.

InP DHBT has higher breakdown voltage and a higher thermal conductivity compared with InP single heterojunction bipolar transistor (SHBT), suitable for high frequency power application. However, DHBT's high-frequency performance is degenerated by the current-blocking effect which caused by the conduction band spike between InGaAs base and InP collector layers. Several methods such as superlattice structure, step-graded doping collector, and quaternary compound (InGaAsP or InAlGaAs) are developed to deal with the current-blocking effect. In this paper we demonstrated a high performance 0.5 μm InP DHBT process with InGaAsP composite collector. The ft/fmax of 0.5×5 μm^2 device reaches 350/535 GHz. Based on this process a high gain, medium power amplifier is designed. The power amplifier's measured gain is 23.6 dB at 75 GHz and 21.89 at 140 GHz. The saturation output power at 140 GHz is 13.7 dBm with DC power consumption 250 mW.

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2 Process

The epitaxial layer of the DHBT was grown on 3 inch semi-insulating InP substrate using molecular-beam epitaxy (MBE). To deal with the current blocking effect caused by the B-C heterojunction conduction band spike an InGaAsP composite collector is used [9]. The composite collector structure consist an InGaAs setback layer, several step-graded InGaAsP layers, and a δ-doping layer. The conduction band spike is smoothed and eliminated. The doping concentration and layer thickness are optimized to achieve a good high frequency performance [10, 11, 12]. The cross-section schematic diagram of device is shown in Fig. 1 and the layer structure is listed in Table I. The width of emitter contact is 0.5 μm. Base contact width is 0.3 μm at each side. Transmission line model (TLM) measurements show a base contact resistivity of $\rho_{bc} = 3.9\,\Omega \times \mu m^2$ and base sheet resistance of $R_{sh,b} = 737\,\Omega$/square. The measured H_{21}, Mason's unilateral gain (U_{mason}) and maximum stable/available gain (MSG/MAG) for two devices are shown in Fig. 2. The extracted ft/fmax of $0.5 \times 5\,\mu m^2$ device is 350/535 GHz and $0.5 \times 7\,\mu m^2$ device is 300/400 GHz. Compared with early reported 0.5 μm InP DHBT [13, 14, 15, 16], this process have some high frequency performance improvement. The process provides three wiring metal layers and compact interconnect vias between them. The MIM capacitor with $0.26\,fF/\mu m^2$ capacitance density and 50 Ω/square TaN TFR are also available.

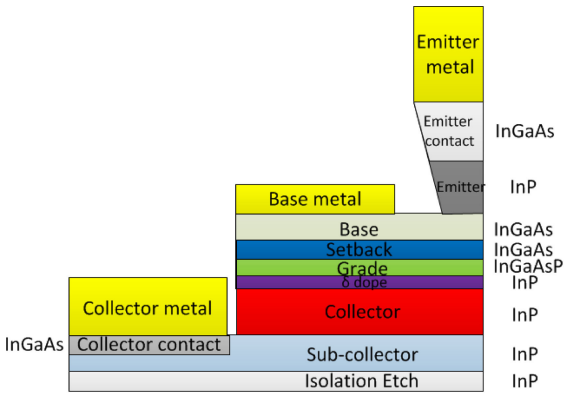

Fig. 1. Schematic diagram of device cross-section.

Table I. Layer structure of the InGaAs/InP DHBT

Layers	Material	Thickness (nm)	Dopant
Emitter Contact	InGaAs	200	Si
Emitter	InP	200	Si
Base	InGaAs	35	C
Set-back	InGaAs	30	Si
δ-doping	InP	20	Si
Collector	InP	150	Si
Collector Contact	InGaAs	50	Si
Sub-collector	InP	200	Si
Etch-stop	InGaAs	10	ud
InP substrate			S. I.

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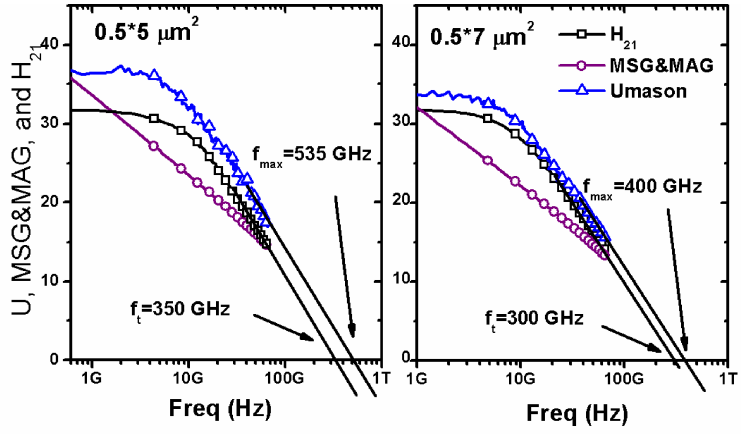

Fig. 2. The f_t and f_{max} of two devices.

3 Circuit design

3.1 Power divider

T-junction power combiner is a simple structure for power combining [17]. For the lack of isolation resistor, three ports cannot be matched simultaneously. And the isolation between two dividing port is bad. The load condition for two dividing port should be identical to avoid odd-mode oscillation. We designed a four way T-junction power combiner for the amplifier. A step impedance transformer is added to achieve a broad band width. A back to back power combiner is fabricated and measured. The micrograph is shown in Fig. 3(a) and the measured data are plotted in Fig. 3(b). The measured insertion loss is 1.53 dB at 140 GHz so the single end insertion loss will be 0.76 dB. The low frequency insertion loss increased gives a gain compression for the amplifier to provides a flat frequency response.

3.2 The amplifier

For output power consideration, we choose $0.5 \times 7\,\mu m^2$ HBT for designing. The nonlinear model is AgilentHBT model which parameters are extracted in 0.2 to 67 GHz band and fine-tuned for fitting up to G band. The amplifiers are primarily optimized for high gain and high output power with adequate input and output match. According to the linear and harmonic balance (HB) load pull simulation, input impedance $Z_s = 20 - j \times 0.5\,\Omega$ and the optimal power load impedance $Z_{Lopt} = 30.1 + j \times 45.5\,\Omega$ at 140 GHz. To achieve a sufficient amount of gain, four stages of HBT are cascaded. Inter-stage match also takes a complex conjugate matching design. A 411 fF MIM capacitor for DC-blocking is inserted between each stage. The capacitance and its parasitic effect are taken into account as a part of matching network. The DC bias is supplied through a long stub with a 1.2 pF decoupling capacitor. And a 10 Ω series resistor is utilized to suppress low-frequency oscillation. All bias lines for four stages are tied together and connected to dc-feed bar. The schematic and micrograph of the circuit are shown in Fig. 4. The total chip area is $1867 \times 2136\,\mu m^2$.

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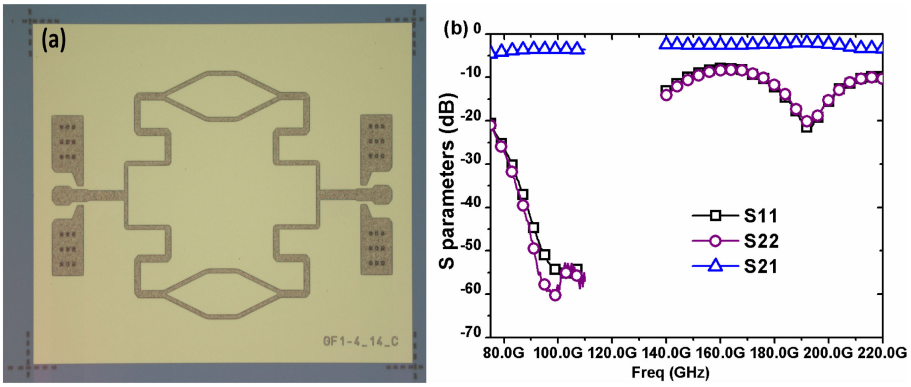

Fig. 3. (a) Micrograph of back-to-back power divider, (b) measurement s-parameters of back-to-back power divider.

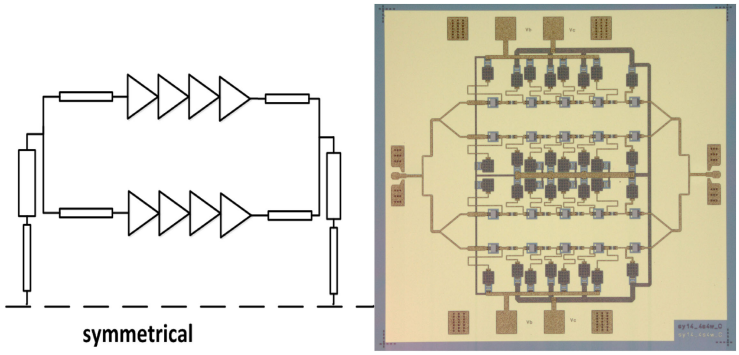

Fig. 4. Schematic and micrograph of amplifier MMIC.

4 Measurement and discussion

The amplifier MMIC is first tested with Cascade probe station, WR-10 and WR-5 waveguide frequency extenders and probes, and DC probe. The small-signal measurements are performed with $V_c = 1.5$ V, $I_c = 160$ mA and $V_b = 0.94$ V, $I_b = 6.4$ mA. At 75 GHz, the amplifier has the peak gain of 23.6 dB. At 140 GHz, the amplifier still has 21.89 dB gain. Fig. 5(a) displays the comparison of simulation and measurement. The power performances are measured with VDI power source and Erickson PM-4 powermeter. After the chain loss is carefully calibrated, 140 GHz output power are measured and plotted in Fig. 5(b), saturation output power is 13.7 dBm.

The comparison of this work and previously publication are listed in Table II. The proposed design has clear advantages in gain and has a competitive output power. This amplifier has potential for driving amplifier or medium power amplifier in D band systems.

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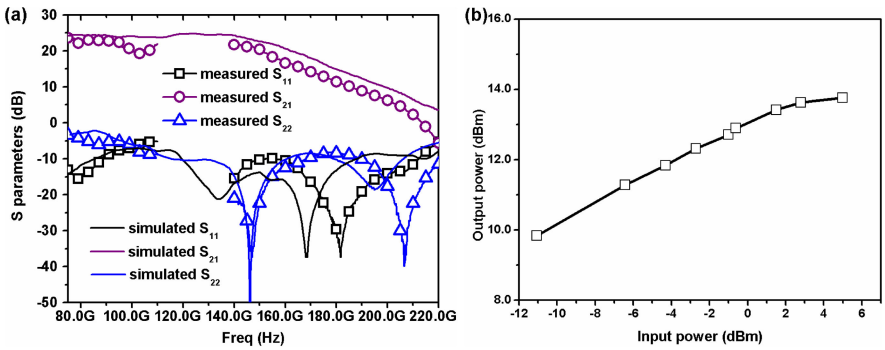

Fig. 5. Measured s parameters and 140 GHz output power.

Table II. The performance comparison

Works	Process	Topology	Gain (dB)	P_{sat}	DC (mW)
[3]	80 nm InP HEMT	3-stage CS 8-way	7	21.4	6400
[4]	0.1 μm InP HEMT	3-stage CS	>9	~11	440
[5]	90 nm SiGe	4-stage CE 8-way	15	20.8	1568
[6]	0.65 μ CMOS	4-stage CS	16	9.9	115.2
[7]	0.25 μ InP DHBT	2-stage CE	14.8	20	442
[8]	0.65 μ CMOS	4-stage CS 8-way	15–16	12.2–13.2	115.2
This work	0.5 μ InP DHBT	4-stage CE 4-way	23.6	13.7	250

5 Conclusion

A four-stages, four-ways, high gain, medium power amplifier is designed based on a high performance composite collector InP DHBT process. The measurement shows that amplifier's peak gain is 23.6 dB at 75 GHz and at 140 GHz the gain is 21.89 dB. The saturation output power is 13.7 dBm at 140 GHz with DC power consumption 250 mW. The total chip area is $1867 \times 2136\ \mu m^2$.

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