ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.14, No.12, 1–10

Analysis of the residual error due to mechanical stress in BJT-based CMOS temperature sensors

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Abstract: It is widely known that the inaccuracy of BJT-based CMOS temperature sensors is higher at high temperature range, which greatly limits their application. In this paper, the characteristic of the error after calibration is analyzed. Through the experiments, we discover that the cause of this problem is not circuit related, instead it is process related, which is the mechanical stress generated during manufacturing and packaging. Experimental results show that an accuracy of −0.5∼2 °C can be obtained for the calibrated non-epoxy sensors from −40 °C to 120 °C.

Keywords: process spread, mechanical stress, CMOS temperature sensor

Classification: Integrated circuits

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DOI: 10.1587/elex.14.20170318
Received March 30, 2017
Accepted May 24, 2017
Publicized June 12, 2017
Copyedited June 25, 2017

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1 Introduction

For BJT-based CMOS temperature sensors, the state-of-the-art design methodology guaranteeing high precision has been demonstrated to be effective for different processes and power supplies [1, 2, 3, 4, 5, 6, 7, 8]. By applying this methodology, the systematic errors caused by the non-idealities in the readout circuitry can be reduced negligibly. The random errors caused by process spread can also be minimized by calibration techniques. Therefore, theoretically the remaining error of the calibrated BJT-based sensors can be reduced below ±0.15 °C [1]. However, in reality, the remaining error is as high as several degrees Celsius, which exists especially at high temperature range. A calibrated inaccuracy of ±0.5 °C [2] and an uncalibrated inaccuracy of −2∼5 °C [9] have been published. They both have extremely large errors at high temperature range 100∼120 °C. This problem has caused people's attention because it limits the applications of the BJT-based sensors. However, until now, we have not found any publication that gives an explanation for it. To solve the problem, we do many experiments and discover one of the causes.

The rest of the paper is organized as follows. In section 2, the process-spread-induced error of V_{BE} in BJT-based sensors is analyzed. In section 3, our circuit and calibration technique which aim to compensate the PTAT error in V_{BE} is introduced briefly. In section 4, our experimental results are presented, which shows that the PTAT error in V_{BE} can be eliminated. Section 5 analyzes the remaining non-PTAT error based on the experimental results, and the paper ends with conclusions.

DOI: 10.1587/elex.14.20170318
Received March 30, 2017
Accepted May 24, 2017
Publicized June 12, 2017
Copyedited June 25, 2017

2 Process-spread-induced errors

To extract temperature information, two temperature-dependent voltages, namely ΔV_{BE} and V_{BE}, are very important in BJT-based sensors. These two voltages contain all the necessary information for the sensing temperature. ΔV_{BE} is the base-emitter voltage difference between two bipolar transistors biased at a different current ratio. It is a proportional-to-absolute-temperature (PTAT) voltage and is immune to process spread [8, 10]. But the base-emitter voltage V_{BE} is sensitive to process spread, and it can be described as follows:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right), \tag{1}$$

where k is Boltzmann constant, q is the electron charge, T is the temperature in Kelvin, I_C is the collector current, and I_S is the saturation current of the bipolar transistors. I_C is generated by the on-chip resistor R, and I_S depends on the doping variations in substrate PNP transistors. Considering the process spread in R and I_S, V_{BE} cannot be accurate on-chip. Consequently, a costly calibration is needed. If the process spread in R and I_S is assumed to be independent of temperature. It can be concluded that V_{BE} is a complementary-to-absolute-temperature voltage, and the spread of V_{BE} is a PTAT error [8, 10]. So the single-point calibration meets the calibration requirement. The single-point calibration means that the sensors only need to be calibrated at one temperature, usually at room temperature. The errors at other temperature are calibrated automatically by linear interpolation. It is preferred rather than two-point or multi-point calibration for cost consideration.

However, due to the piezojunction effect, mechanical stress causes the variations in both minority-carrier mobility and the intrinsic-carrier concentration in the base of a bipolar transistor [11]. So the process spread in I_S changes with temperature due to mechanical stress. In order to estimate the process spread in V_{BE}, the saturation current I_S needs to be examined. It can be expressed as

$$I_S = \frac{kTAn_i^2\overline{\mu_p}}{W_B N_d}, \tag{2}$$

where A is the emitter area, n_i is the intrinsic carrier concentration, $\overline{\mu_p}$ is the average diffusion constant, W_B is the base width, and N_d is the base doping concentration. A, W_B, and N_d vary with process, but their variations are independent of temperature. The spread of n_i and $\overline{\mu_p}$ are temperature dependent. Therefore, I_S can be divided into three parts:

$$I_S = I_{S0}(1 + \varepsilon_{PTAT})(1 + \varepsilon_{NONPTAT}), \tag{3}$$

where I_{S0} is process-spread-free saturation current, ε_{PTAT} is the cause of the PTAT error in V_{BE}, and $\varepsilon_{NONPTAT}$ is the cause of the non-PTAT error in V_{BE}. The non-PTAT error is the residual error after the single-point calibration. Since the PTAT error can be removed out by calibration techniques [8]. To obtain high accuracy, the study on the non-PTAT error is extremely important.

The cause of the non-PTAT error is remaining an open question. Some people [10, 11] thought that the mechanical stress may be the cause, but no one has given clear evidence. In this paper, we will demonstrate that the mechanical stress is the major contribution to the non-PTAT error based on our experiments. Mechanical

DOI: 10.1587/elex.14.20170318
Received March 30, 2017
Accepted May 24, 2017
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stress is the result of expansion or contraction of materials with different thermal expansion coefficients. It can be generated during IC fabrication or package, thus resulting in two types of stresses: the process stress induced by manufacturing and the package stress induced by packaging. Taking $\varepsilon_{PROCESS}$ is the effect of process stress and $\varepsilon_{PACKAGE}$ is the effect of package stress, I_S can be described as:

$$I_S = I_{S0}(1 + \varepsilon_{PTAT})(1 + \varepsilon_{PROCESS})(1 + \varepsilon_{PACKAGE}). \quad (4)$$

The process stress is an inherent and internal stress. It is foundry dependent and cannot be controlled by designer. While for the external package stress, the stress-induced-error can be minimized to a reasonable level by choosing particular encapsulation [11]. Reference [10] shows that ceramic or metal packages are preferred rather than plastic packages because they introduce less error.

In order to analyze the non-PTAT error, we should remove the PTAT error by a calibration technique firstly. The proposed circuits and calibration technique will be discussed in next section.

3 Proposed circuitry and method for calibration

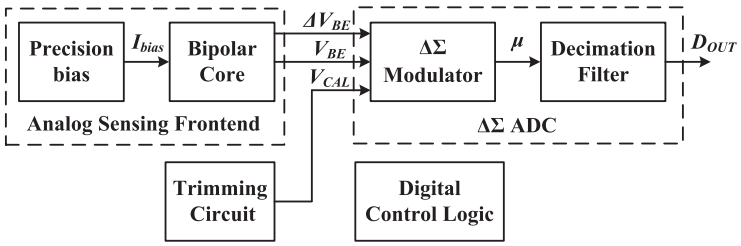

Fig. 1. Block diagram of the proposed BJT-based temperature sensor.

The block diagram of the proposed BJT-based temperature sensor is shown in Fig. 1. It contains an analog sensing frontend, a delta-sigma ADC, a trimming circuit, and a digital control logic circuit. The analog sensing frontend that contains precision bias and bipolar core generates ΔV_{BE} and V_{BE}. The delta-sigma ADC processes ΔV_{BE} and V_{BE} to obtain the digital temperature reading T. The trimming circuit provides a calibration voltage V_{CAL} to adjust V_{BE}. Digital control logic circuit provides the control signal of all the blocks. The final T can be written as:

$$T = A\mu + B = A\frac{\alpha\Delta V_{BE}}{\alpha\Delta V_{BE} + V_{BE} + V_{CAL}} + B = A\frac{V_{PTAT}}{V_{VREF} + V_{CAL}} + B, \quad (5)$$

where α is the scale factor to make V_{REF} a temperature-independent bandgap reference voltage; A and B are scale factors to transform μ into a temperature reading in degree Celsius.

Some points need to be addressed. The delta-sigma ADC contains a delta-sigma modulator (DSM) and decimation filter. A second-order cascade of integrators feedforward (CIFF) DSM with single-bit quantization is applied here and its behavioral model is shown in Fig. 2. The cascaded integrator-comb (CIC) filter is a hardware-efficient digital filter to realize decimation filter [12] and a three-order CIC filter is applied in our work.

DOI: 10.1587/elex.14.20170318
Received March 30, 2017
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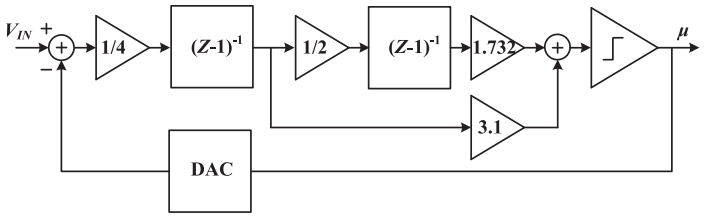

Fig. 2. Behavioral model of the single-bit second-order CIFF DSM.

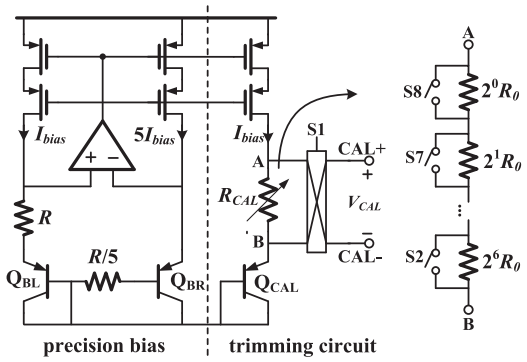

Fig. 3. Schematic of our trimming circuit.

The circuit implementation of the Fig. 1 can be found in our previous work [13]. In this paper, we will focus on the mechanical-stress-induced error. Therefore we only discuss the calibration related issues. The schematic of our trimming circuit is shown in Fig. 3. Correspondingly, an input branch for calibration is added to our DSM [13]. R_{CAL} is a trimming resistor network, which contains seven binary-weighted resistors in series. Each resistor is connected with a switch in parallel. A β-sensitive PTAT current generated by precision bias passes through R_{CAL}, and the voltage V_{CAL} across this resistor is used to compensate the spread of V_{BE}. V_{CAL} can be described as:

$$V_{CAL} = I_{bias} \cdot R_{CAL} = \frac{\beta + 1}{\beta} \frac{\Delta V_{BE}}{R} (S2 \cdot 2^6 + \cdots S7 \cdot 2^1 + S8 \cdot 2^0) R_0, \qquad (6)$$

where β is the forward current gain of the bipolar transistor. Here a β-sensitive PTAT current is used to reduce the β-induced error in bipolar core [8]. It will affect our calibration voltage V_{CAL}. We will discuss this effect in detail in section 5. S1 controls the polarity of V_{CAL}, and S2–S8 control the magnitude of V_{CAL}. V_{CAL} and V_{BE} are the inputs to the DSM simultaneously.

4 Calibration for the PTAT error

In order to verify the performance of the PTAT error calibration, we will compare the measured error of our fabricated sensors before and after calibration. Our temperature sensor is fabricated in the Global Foundries 0.18 µm CMOS technology. The chip micrograph of the fabricated sensor is shown in Fig. 4. It occupies 1 mm × 1 mm, including a frontend, a DSM, a trimming circuit, a CIC decimation filter, a bandgap reference, and a digital control logic circuit.

Six chips are randomly selected. Three of them are epoxy packaged and three are not. Fig. 5 shows the chips under test with and without epoxy package. Both

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Accepted May 24, 2017
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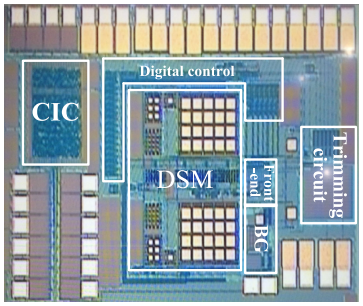

Fig. 4. The chip micrograph of our fabricated sensor.

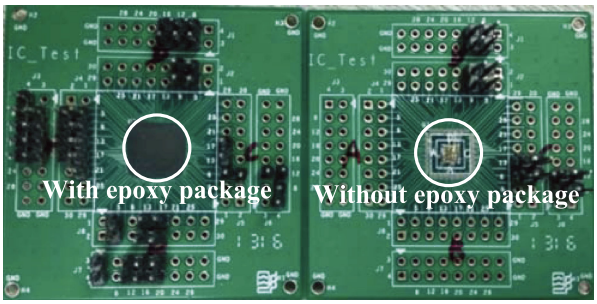

Fig. 5. Chips under test with and without epoxy package.

process stress and package stress exist in the chips with epoxy package, while only process stress exists in the chips without epoxy package. Each chip is bonded on a printed circuit board. The test boards are placed in an oven that can provide an environment of −60 °C to 150 °C. A Fluke 1551A thermometer with accuracy of ±0.05 °C is used to measure the chip temperature. Our single-point calibration procedure is applied at room temperature, which can cover 10 °C range with a step of 0.1 °C.

The PTAT error in V_{BE} can be removed by single-point calibration. The non-ideality of the circuitry is reduced by proper circuit design. But there is still a large error, especially at high temperature range. This residual error is a non-PTAT error caused by mechanical stress. In order to distinguish the difference between process stress and package stress, both epoxy and non-epoxy chips are measured from −40 °C to 120 °C in a step of 20 °C before and after calibration using the Fluke 1551A thermometer. For each temperature step, the temperature in the oven is controlled to be stable for a long time to establish thermal equilibrium between the sensors under test and the thermometer.

The measured errors of the three chips with epoxy package before and after calibration are shown in Fig. 6(a) and (b), respectively. And chips without epoxy package are shown in Fig. 7(a) and (b). The experimental results show that for chips with epoxy package, an accuracy of ±6 °C can be achieved from −40 °C to 120 °C before calibration, and −3∼6 °C can be achieved after calibration. While for chips without epoxy package, the accuracy is −2∼3 °C and −0.5∼2 °C for the uncalibrated and calibrated sensors, respectively.

According to the results shown in Fig. 6 and Fig. 7, it can be concluded that:

1. After calibration, the accuracy of all the chips is greatly improved. It means that the PTAT error in V_{BE} induced by ε_{PTAT} has been calibrated out.

DOI: 10.1587/elex.14.20170318
Received March 30, 2017
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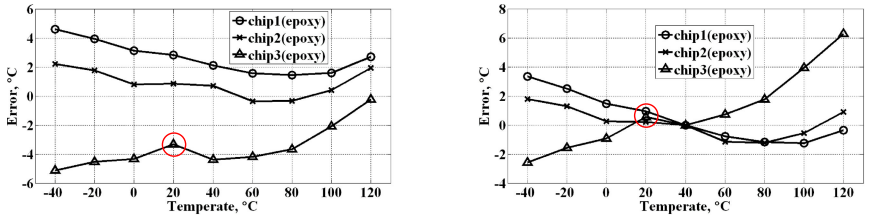
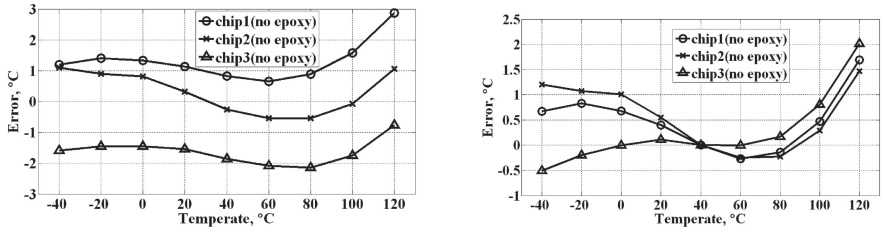


(a) (b)

Fig. 6. Measured errors of 3 chips with epoxy package before and after calibration.



(a) (b)

Fig. 7. Measured errors of 3 chips without epoxy package before and after calibration.

2. The accuracy of the non-epoxy chips is much smaller than that of the epoxy chips. This is because only process-stress-induced error is remaining in the non-epoxy chips.

3. The behavior of the errors for the non-epoxy chips is similar (Fig. 7), while that for the epoxy chips is quite different (Fig. 6). The reason is that the process stress is almost the same for the chips in the same batch. While the package stress can vary much for different packaged chips even using the same material.

By comparing the results between the chips with and without epoxy package, we can clearly see that the total error contribution of process spread consists a PTAT error induced by ε_{PTAT} and a non-PTAT error induced by $\varepsilon_{NONPTAT}$. The non-PTAT error can be mainly divided into process-stress-induced error $\varepsilon_{PROCESS}$, and package-stress-induced error $\varepsilon_{PACKAGE}$.

5 Analysis of the residual non-PTAT error

In order to study the effect of the mechanical stress, we process the data by using individual linear fitting algorithm. It means that the measured μ of each individual chip is linearly fitted by its experimental data. So certainly it will result in a minimum residual error for each chip, while the PTAT error in V_{BE} is virtually completely removed. This algorithm differs from the algorithm used in section 4, which linearly fits the average errors of all the chips. The comparison between the average and individual linear fitting algorithm is shown in Fig. 8. By applying the individual linear fitting algorithm, we can accurately analyze the residual non-PTAT error.

To find out the reason why large error is at high temperature range, we compare the measured mechanical stress between our work and the previous work [11].

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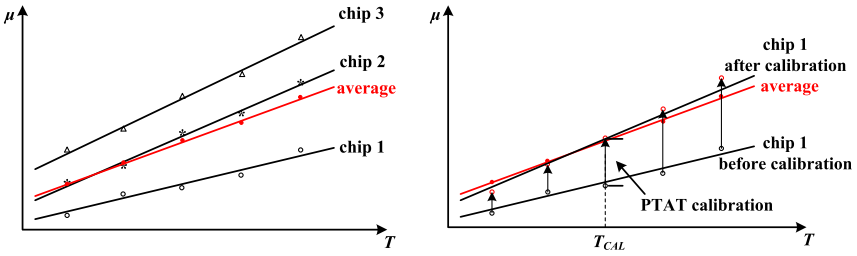
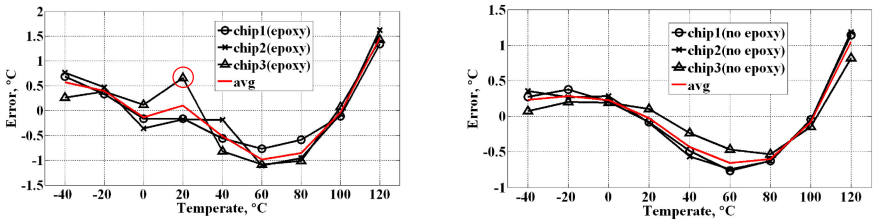


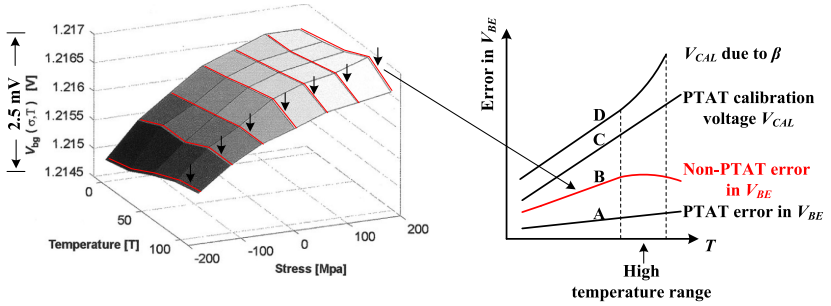
(a) (b)

Fig. 8. Comparison between the average and individual linear fitting algorithm: (a) average errors of the three chips before calibration at different temperature; (b) errors of chip 1 before and after calibration using the average errors as a reference.



(a) (b)

Fig. 9. Processed errors of 3 chips with and without epoxy package using individual linear fitting.



(a) (b)

Fig. 10. Comparison between our work and the previous work: (a) the effect of the mechanical stress proposed in [11]; (b) the effect of the mechanical stress in our work.

Although the mechanical stress cannot be measured directly, it can be evaluated by converting the mechanical stress to other parameters which can be measured. In our work, the mechanical stress is converted to the temperature errors of the chips with and without epoxy package by individual linear fitting, as shown in Fig. 9(a) and (b), respectively. For comparison, the output of bandgap reference with different temperature and different mechanical stress, which was proposed in [11], is shown in Fig. 10(a).

It is well known that the temperature errors increase dramatically at high temperature range. In our work the temperature errors increase dramatically in 100~120 °C with a maximum error of 1.5 °C and 1.2 °C for chips with and without epoxy package, respectively. As stated in [10], 1°C temperature error is equivalent

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to a 3 mV error in V_{BE}. It means a maximum error of 4.5 mV in V_{BE} in our work. For the work in [11], it can be seen, as shown in Fig. 10(a), that for typical mechanical stress, the voltage output decreases dramatically at high temperature range with a maximum error of 2.5 mV in V_{BE}.

Since the work in [11] and our work are both in CMOS technology, we may reasonably assume that the mechanical stress introduces the similar error in our work as that shown in Fig. 10(a). According to equation (5), the final T can be described as

$$D_{OUT} = A\frac{\alpha\Delta V_{BE}}{\alpha\Delta V_{BE} + V_{BE,ideal} + \Delta V_{BE,PTAT} + \Delta V_{BE,NONPTAT} - V_{CAL}} + B \quad (7)$$

where $\Delta V_{BE,PTAT}$ is the PTAT error in V_{BE}, $\Delta V_{BE,NONPTAT}$ is the non-PTAT error in V_{BE}, which is assumed to have the similar characteristic as the work in [11]. As shown in Fig. 10(b), $\Delta V_{BE,PTAT}$, $\Delta V_{BE,NONPTAT}$, and V_{CAL} are represented by curve A, B, and C, respectively. So after the PTAT calibration, the mechanical stress makes the final V_{BE} smaller and hence higher temperature error, which fits very well to our results, as shown in Fig. 9(a) and (b). It can be concluded that the residual error in our work is mainly caused by the mechanical stress, especially at high temperature range.

As stated in [10], β decreases with temperature. According to equation (6), the PTAT calibration voltage becomes larger at high temperature range due to the variation of β, which is represented by curve D in Fig. 10(b). It means the effect of the mechanical stress is getting worse by using this β-sensitive PTAT calibration voltage. This is the reason why we have a maximum error of 4.5 mV in V_{BE} which is larger than 2.5 mV in [11].

One may notice that the error of chip 3 at 20 °C, as shown in Fig. 9(a), has a singular point. It may be caused by reading error. The singular point also happens in Fig. 6 because we process the same original measured data. Anyway the average of the three curves, as shown in Fig. 9(a), is similar to that in Fig. 9(b). The reason is that the individual linear fitting algorithm seems to completely remove the PTAT error in V_{BE}, thus leaving a uniform and inherent error. As the package stress and the process stress both are mechanical stress, they should have the similar characteristic. This is another proof to demonstrate that the residual non-PTAT error is mainly caused by mechanical stress.

One may notice that both red curves in Fig. 9(a) and (b) have the minimum at 60 °C. This is maybe caused by the residual curvature existed in V_{BE}. Although we have applied the curvature correction technique, the residual curvature error is still noticeable and should be reduced by more careful consideration in our future work.

By comparing the results between our work using individual linear fitting and the previous work [11], one can clearly see that the mechanical stress results in large error at high temperature range.

6 Conclusion

The process-spread-induced error in BJT-based CMOS temperature sensor has been studied. We have demonstrated that the residual error in V_{BE} at high temperature range is mainly caused by the mechanical stress. Experimental results show that the

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temperature error is smaller for the chips without epoxy package. After one-point calibration, the error of the sensors is within −0.5∼2 °C from −40 °C to 120 °C, which is mainly caused by the mechanical stress.

Acknowledgments

This work was supported in part by Shenzhen Key Lab for RF Integrated Circuits, Shenzhen Shared Technology Service Center for Internet of Things, National key R&D plan (grant number 2016YFC0105002 and 61674162), Guangdong government funds (grant numbers 2013S046 and 2015B010104005), Shenzhen government funds (grant numbers CXZZ20150601160410510 and JCYJ20160331192843950), and Shenzhen Peacock Plan.

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