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A 6 mW 325 MS/s 8 bit SAR ADC with background offset calibration

Xiaoge Zhu[1,2], Danyu Wu[1], Lei Zhou[1], Chonghe Ma[1], Dandan Wang[1], Jian Luan[1], Yinkun Huang[1], Jin Wu[1], and Xinyu Liu[1a)]

[1] *Institute of Microelectronics of Chinese Academy of Sciences, 3 Beitucheng West Road, Chaoyang District, Beijing, China*

[2] *University of Chinese Academy of Sciences, 19 A Yuquan Road, Shijingshan District, Beijing, China*

a) *xyliu@ime.ac.cn*

Abstract: An 8-b single-channel successive approximation register (SAR) analog-to-digital converter (ADC) fabricated in 55 nm CMOS is proposed. With segmented prequantize and bypass digital-to-analog converter (DAC), the unnecessary switching of high weight capacitors are avoided. Two alternating comparators are utilized to reset the comparators completely without the sacrifice of conversion speed. A novel simple and low power background offset calibration technique is implemented. Operating at 325 MS/s, this ADC consumes 6 mW from 1.2 V supply, achieves SNDR of 43.6 dB and SFDR of 59.1 dB with 11-MHz input while occupying 0.011 mm^2.

Keywords: analog-to-digital converter (ADC), successive approximation register (SAR), segmented prequantize and bypass, alternating comparison, asynchronous timing, background offset calibration

Classification: Integrated circuits

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1 Introduction

Integration of low-power and area-efficient ADCs is a key differentiator in modern mixed-signal SoCs in both consumer and industrial applications [1, 2]. Compared to flash and pipeline ADCs, SAR ADC is a highly digitized architecture and its analog comparators can be used in circles. Technology scaling with low supply voltages in digital CMOS processes favors ADC topologies with few truly analog elements, making SAR ADCs pefectly suitable. Thus, it can achieve low power while occuping small area. A number of improvements about SAR ADC were achieved in the past few years. Segemented prequantize and bypass DAC switching [3] avoids unnecessary opposite direction switching of big capacitors as the approaches [4, 5] with less additional components (only two switches are added). Two comparators running in an alternating fashion [1] helps to reset the comparator completely and break the speed restriction of reset time when the settling time of the capacitor DAC is short enough. Asynchronous clocking [6] allows the comparision time allocated to each bit to be adjusted by the comparator itself and avoids the high-speed clock's generation and distribution. M-bit per cycle SAR ADCs [7, 8] quantize M-bits simultaneously with 2^M-1 comparators to increase conversion speed. But comparators mismatches should be resolved with calibrations and more capacitors DACs' areas cost. In this design, the most of the above-mentioned improvements are adopted and a simple single-bit/cycle SAR ADC with background offset calibration is proposed which can be further used as a sub-ADC for time-interleaved ADCs.

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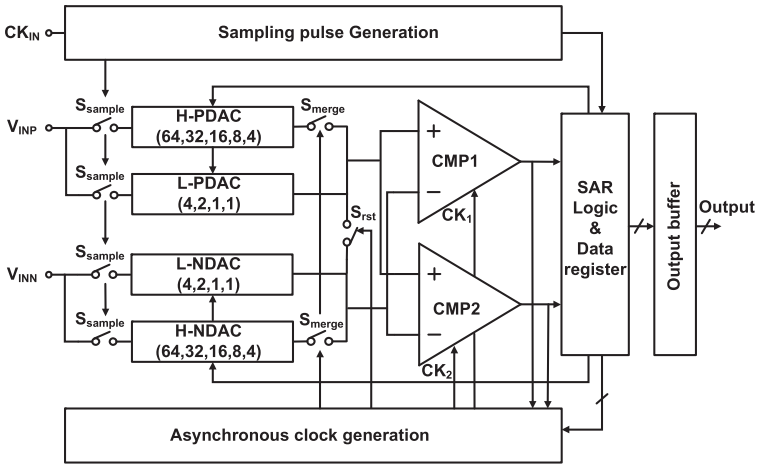
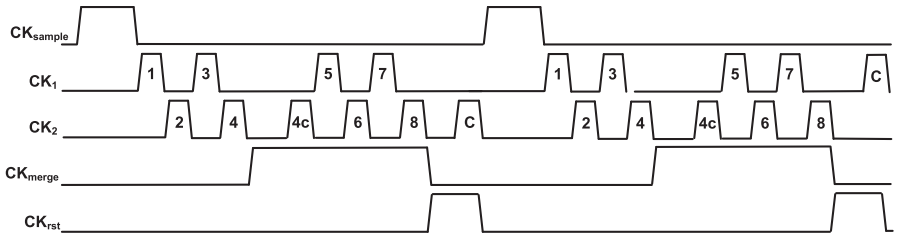
2 Proposed ADC architecture



(a) Overall ADC architecture.



(b) Timing diagram.

Fig. 1. The proposed single-channel SAR ADC.

The architecture and timing diagram of the proposed ADC operating at 325-MS/s sampling rate are illustrated in Fig. 1. Each capacitor array is split into two seperated parts (H-PDAC/L-PDAC or H-NDAC/L-NDAC) because of segemented prequantize and bypass DAC switching. To keep the commom-mode voltage relatively stable and avoid using the reference voltage V_{cm}, every capacitor, except the LSB one, is split into two identical small capacitors and connected to V_{ref} and GND, respectively [9]. The input signal is directly sampled on the top plates of the capacitor arries through bootstrapped switches when the CK_{sample} is high. The customed layout of bootstrapped switches is adopted as [10] which no cross-coupled transistors is needed to compensate for signal feed-through and less parasitics are added. Different from conventional method, only the L-PDAC and L-NDAC were connected to the inputs of comparators after sampling. The two comparators runs in an alternating fashion for first four bits. Based on the L-DACs' decisions, the capacitors of H-DACs were switched in one direction (or bypass) which avoids unnecessary switching of big capacitors. The decision results applied to big capacitors are one bit shifted to left and applied directly (when result = MSB), or bypassed and skipped (when result ≠ MSB) to H-DACs. After the forth comparison is done, the merging switches (S_{merge}) are on, the H-DACs are properly set and all capacitors in L-DACs are reset to the initial condition. A capacitor (4C) is inserted in H-DACs to provide redundancy to compensate the possible wrong decisions caused by mismatches and parasitics difference between H-DAC and

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L-DAC. In order to unchange the connecting relationships between comparators and L-DACs' capacitors, the redundante bit is also decided by CMP2. Then the ADC completes the residual lower weight 4 bits in alternating fashions like before. When all the conversions are finished, the merging switches are off and reset switch (S_{rst}) is on. Then comparators' offsets are calibrated alternately and each comparator's calibration is operated every second cycle. The SAR Logic and data register of the designed ADC has been further enhanced by register-to-DAC direct control and domino-cell based pseduo-static dynamic register as proposed in [7].

3 Circuit implementations

3.1 Segmented prequantize and bypass DAC

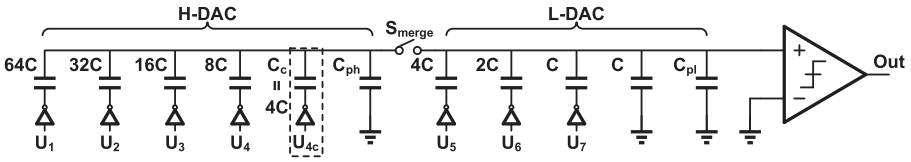

Fig. 2. The single-end version of proposed ADC.

The capacitive DAC is built with a topology that is similar to the segmented prequantize and bypass principle in [3]. The single-end version of the proposed ADC is shown in Fig. 2. In the proposed ADC architecture that S_{merge} is off initially, small capacitors are used instead of the large ones when converting the first 4-bit code. According to the first 4-bit code, the unnecessary opposite direction switching of big capacitors are avoided. It improves the conversion speed of the proposed ADC. Meanwhile, lower switching energy in conversion phase is consumpted which relaxes the design of reference buffer or reduces the size of reference decaps. Moreover, if switchings of big capacitors in H-DAC are bypassed, their mismatches will not contribute to the nonlinearity of DAC's output which benifits the ADC's linearity. When the first 4-bit are completed, the S_{merge} is on. In order to keep the linearity of the propose ADC, the weights of big capacitors in H-DAC must be consistent with those of small capacitors in L-DAC. They should have the following relationship:

$$\frac{C_H}{C_H + C_{ph} + C_c} = \frac{C_L}{C_L + C_{pl}} \tag{1}$$

That is

$$120C_{pl} = 8(C_c + C_{ph}) \tag{2}$$

Where C_{ph} and C_{pl} are the parasitic capacitance introduced to H-DAC and L-DAC. C_H is total capacitance of H-DAC except C_{ph} and C_c while C_L is total capacitance of L-DAC except C_{pl}. Considering the inaccuracy caused by process variation, parameter extraction, incomplete settling and other factors, a compensation capacitor C_c is inserted to provide redundancy. A 4C is inserted as C_c with the consideration of both power and the effectiveness of compensation. As S_{merge} connects H-DAC and L-DAC and locates in the critical path, a voltage-boosting switch is used for less settling time, which significantly reduces its on-resistance.

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3.2 Dynamic comparator with background offset calibration

Comparator is a key component of the conversion in SAR ADC. Fig. 3(a) depicts the proposed dynamic comparator, modified from the one in [11]. The double-tail latch-type voltage comparator [12] allows the speed and offset to be optimized independently which makes the design more flexible. However, the cross-coupled inverters require quite a large voltage headroom to accomodate $2|V_{th}| + 2V_{ov}$ to work in saturation which limits the achievable speed of the comparator at low supply voltage. In the proposed method, two cross-coupled pair stages in parrallel called cross-coupled latches are adopted which aid faster decision based on stronge positive feedback path but with smaller headroom limitation ($|V_{th}| + 2V_{ov}$). In [12], only after the common-mode voltage exceeds the threshold voltage of input pair of the second stage, the voltage amplification in the second stage takes over. Differently, the transconductance stage consisiting of M1–M2 translates the first stage signal to latched stage at the begining of the comparision in proposed method which accelerates the decision speed. Moreover, the transconductance stage can also be used to optimize the offset of the latched stage by seperated current tail M_t. M3–M6 are used to reset the comparators and their sizes can be minimized due to comparators' alteranting fashion which reduces the parasitic load. Based on Monte Carlo and transient noise simulations, the RMS (root-mean square) input referred offset and noise of the proposed comparator are 8 mV and 0.5 mV, respectively, with 1.2 V supply voltage and 0.9 mV common-mode voltage.

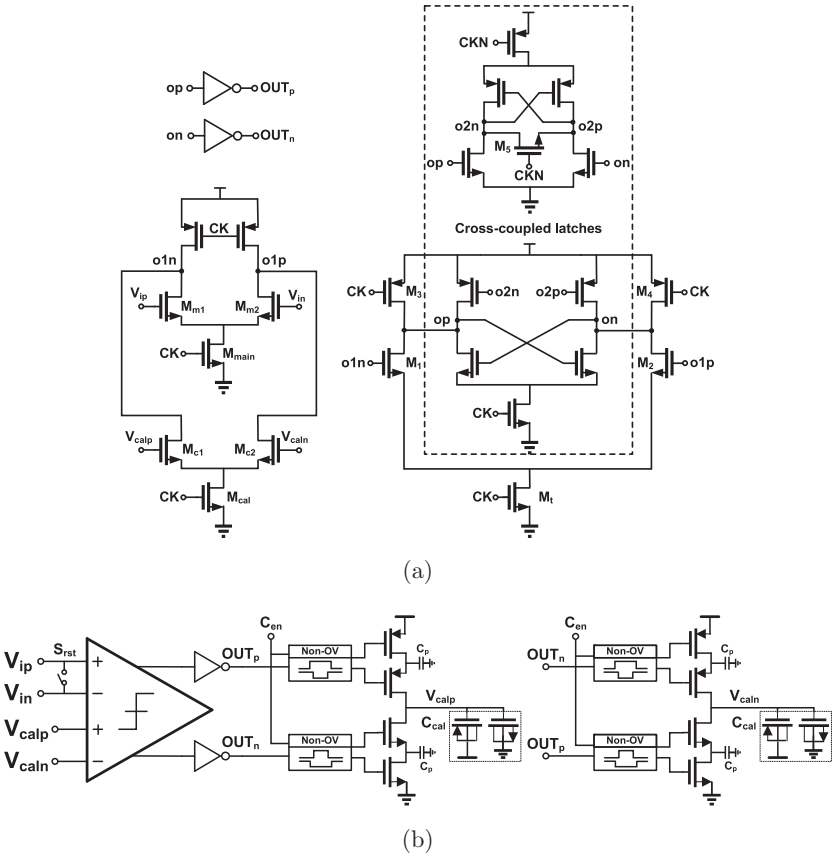

Fig. 3. (a) The proposed dynamic comparator. (b) The offset cancellation technique.

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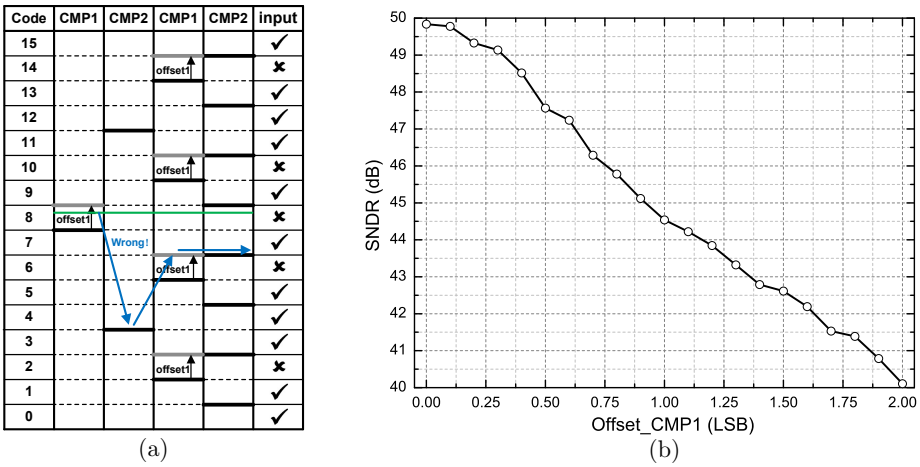

Fig. 4. (a) Non-liearity caused by offset mismatches in 4-bit SAR ADC with alternate comparators (b) SNDR verus offset mismatch

Alternate comparators relax the speed restriction of comparator's reset time. However, offset mismatch between the two comparators causes SAR ADC non-linearity, and analog calibration for the offsets must be used. Fig. 4(a) shows a 4-bit example of alternate comparators' method in which the CMP2 is ideal while the CMP1 is modeled with 1 LSB offset. Due to the offset mismatch, the input voltages within 2, 6, 8, 10 and 14 get the wrong conversion results. Besides, the behavioral simulations of the proposed ADC are operated. Fig. 4(b) illustrates the relationship between the SNDR and the offset of CMP1 while CMP2 is ideal. It is obvious that a 1 dB penalty translates the offset mismatches within 0.3 LSB.

A fast, low-power calibration circuit improved from [1] is used, shown in Fig. 3(b). A second differential pair M_{c1} and M_{c2} is introduced to calibrate the offset. It is sized 4× smaller than the main differential pair (M_{m1} and M_{m2}) to minimize its impact on comparator gain and noise. A charge-pump-based offset tracking method was used for simple and small area occupying. Depending on the decision of the comparator, charge is either added to the calibration capacitor C_{cal} or subtracted from it. The offset calibration is operated in last cycle of every convertion. The C_p is the parastic capacitors of the switches and routing. The C_{cal} is MOS capacitor consisting of a NMOS and a PMOS. Due to the nonlinearity of MOS capacitor with the voltage, the common-mode voltage of the second pair will automaticly be the proper value which is related to the size ratio of PMOS and NMOS in C_{cal} after some calibration cycles nomatter what its initial value is. Moreover, the high-density character of MOS capacitor, a compact, small layout is achieved. The ratio of the C_{cal} and the C_p was chosen to be 500:1 and the RMS input offset voltage is dramatically improved from 8 mV to 0.5 mV after calibration.

3.3 Asynchronous clock generation

The asychronous clock generation circuits in the proposed ADC is shown in Fig. 5. The pre-charged/dynamic logic is used for CK_1 and CK_2 to improve speed and power efficiency. The generations of C_{comp1} and C_{comp2} is optimized to satisfy the short settling time of capacitive DAC by reducing the number of combinational logic. Before the begining of next conversion, the comparators are reset to low and

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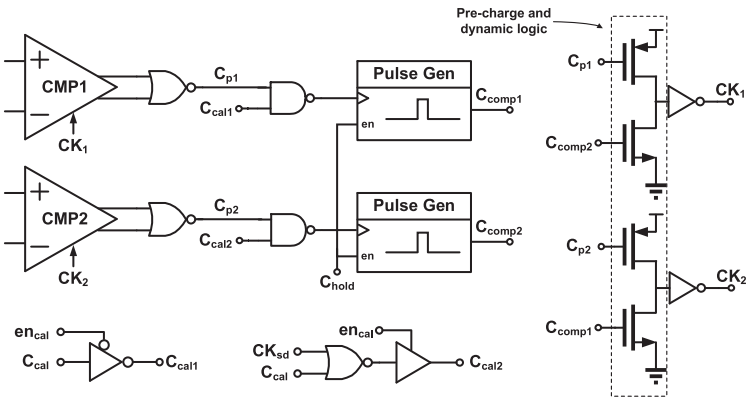
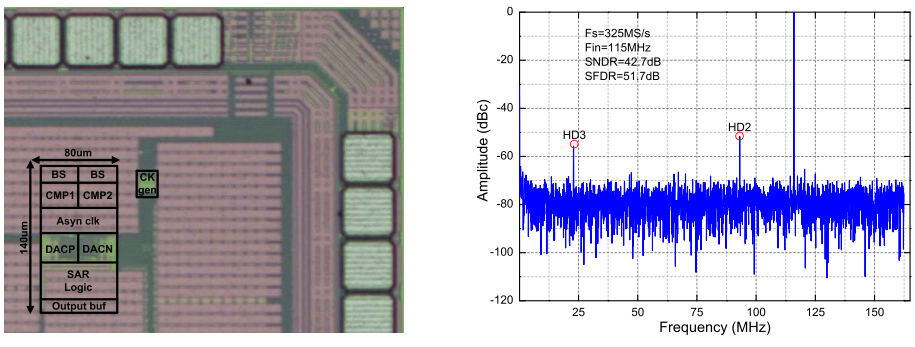


Fig. 5. Asynchronous clock generation circuits.

C_{cal} and C_{hold} are set to low and high, respectively. After sampling, the delayed sampling signal CK_{sd} triggers the pulse generator and CK_1 is enabled. Once the comparison is completed, CK_1 is disabled by C_{p1}, the comparator turns to reset state and then CK_2 is activated. Meanwhile, The C_{cal} is used to activate the clock path, whereas the the signal C_{hold} is used to disable the pulse generation. They can be used to generate the CK_2 signals when S_{merge} is on. Additionally, CK_1 and CK_2 can be generated in turn by them to activate offset calibration. The 2 divided sampling signal, en_{cal}, decides which the comparator is calibrated.

4 Measured results

The prototype ADC was fabricated in 1P9M 55 nm CMOS process with a core chip area 0.011 mm^2. The die micrograph is shown in Fig. 6(a). Fig. 6(b) shows the measured output spectrum that a 115 MHz input sine wave is sampled at 325 MS/s. The static performance of differential non-linearity (DNL) and integral non-linearity (INL) is shown in Fig. 7(a). The measured DNL and INL are +0.96/−0.96 LSB and +0.94/−0.92 LSB, respectively. Fig. 7(b) plots the SNDR and SFDR of the ADC as a function of the input frequency. The ADC maintains linearity over 6.8 bit until the input frequency is beyound 500 MHz. The total power consumption of the prototype ADC is 6 mW excluding digital output buffers from a supply voltage of 1.2 V and a figure-of-merit (FOM) of 191 fJ/covn-step is achieved.



(a) (b)

Fig. 6. (a) The die micrograph (b) Output FFT spectrum

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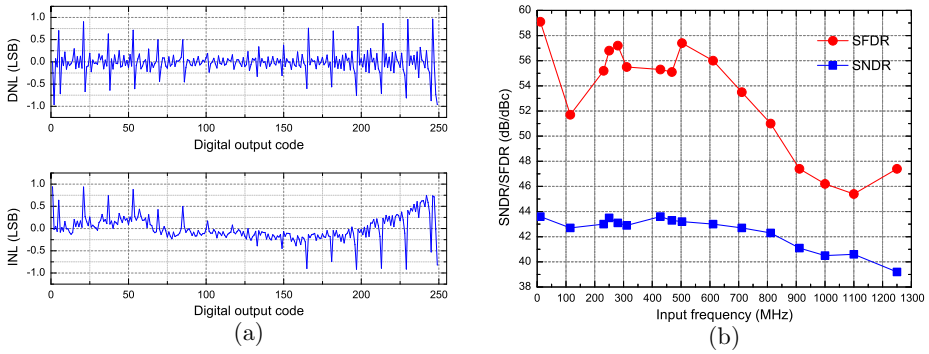

Fig. 7. (a) DNL and INL (b) SFDR and SNDR verus input frequency

5 Conclusion

This paper presents a single-channel 325 MS/s 8 bit SAR ADC fabricated in 55 nm CMOS technology. Combining the segmented prequantize and bypass DAC and alternating comparison techniques, low switching energy and high speed performances are achieved. A novel low noise, low offset and high speed comparator with background offset calibration has been also proposed. The proposed ADC achieves an ENOB over 6.8 bit up to 500 MHz input frequency at 325 MS/s with a FOM of 191 fJ/covn-step.

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