# Efficient unified semi-systolic arrays for multiplication and squaring over $\operatorname{GF}\left(2^{m}\right)$ 

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#### Abstract

In this paper, we propose a unified algorithm to concurrently perform multiplication and squaring over $G F\left(2^{m}\right)$ using the bipartite modular multiplication method and deriving common operations. Also we design efficient unified semi-systolic arrays from our proposed algorithm for fast exponentiation. The proposed arrays can be used as a core circuit for various applications. Also our architectures are well suited to VLSI implementation as well.


Keywords: finite field, Montgomery multiplication, squaring, systolic array, cryptography
Classification: Integrated circuits

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## 1 Introduction

The arithmetic operations over finite field $G F\left(2^{m}\right)$ are very important for many practical applications in error-correcting codes and cryptography [1, 2]. The multiplication is one of the basic arithmetic operations over finite fields. Modular exponentiation and inversion can be performed using a sequence of multiplications. Although many multiplier over $G F\left(2^{m}\right)$ have been proposed [3, 4, 5, 6, 7], their high space and time complexities are major limitations in various applications.

The Montgomery multiplication algorithm has been proposed for fast modular integer multiplication [8]. The Montgomery multiplication was successfully adapted to $G F\left(2^{m}\right)$ in [9]. An approach based on Montgomery multiplication which allows one to split the operand into two parts, which can be processed in parallel, is called a bipartite modular multiplication and is introduced in [10, 11]. They focused on application in the integer and mentioned the usability of their method in the finite field. Thereafter, Kim and Jeon adapted their bipartite technique to the modular multiplication in the finite fields for reducing the latency and proposed multipliers over $G F\left(2^{m}\right)[5,7]$.

The modular exponentiation is an essential part of cryptographic algorithms. It is typically performed using a series of modular squaring and multiplication based on the binary method. There are two modular exponentiation schemes: LSB (least significant bit)-first and MSB (most significant bit)-first modular exponentiation, where LSB and MSB refer to the LSB and MSB of the exponent. For fast LSB-first modular exponentiation, modular squaring and multiplication can be performed simultaneously [12, 13, 14]. Using the common operations from multiplication and squaring, Choi and Lee [6] proposed the combined systolic multiplier/squarer that computes modular squaring and multiplication concurrently instead of computing them separately for the LSB-first exponentiation.

In this paper, we propose a unified algorithm to concurrently perform multiplication and squaring over $G F\left(2^{m}\right)$ using the bipartite modular multiplication method and deriving common operations. Then we design efficient unified semisystolic arrays to concurrently compute multiplication and squaring over $G F\left(2^{m}\right)$ from our proposed algorithm for fast exponentiation.

## 2 Preliminaries

### 2.1 Montgomery multiplication

$G F\left(2^{m}\right)$ is a kind of finite field that contains $2^{m}$ different elements. This finite field is an extension of $G F(2)$ and any element over $G F\left(2^{m}\right)$ can be represented as a polynomial of degree $m-1$ over $G F(2)$. Let $x$ be a root of the polynomial, then the irreducible polynomial $G$ is represented as $G=\sum_{j=0}^{m} g_{j} x^{j}$, where $g_{j} \in G F(2)$.

Let $\alpha$ and $\beta$ be two elements of $G F\left(2^{m}\right)$, then we define $\gamma=\alpha \cdot \beta \bmod G$. Also, let $A$ and $B$ be two Montgomery residues, then they are defined as $A=$ $\alpha \cdot F \bmod G=\sum_{j=0}^{m-1} a_{j} x^{j}$ and $B=\beta \cdot F \bmod G=\sum_{j=0}^{m-1} b_{j} x^{j}$, where a Montgomery factor, $F$ and an irreducible polynomial, $G$ are relatively prime, and $\operatorname{gcd}(F, G)=1$. Then, the Montgomery multiplication algorithm over $G F\left(2^{m}\right)$ can be formulated as $P=A \cdot B \cdot F^{-1} \bmod G$, where $F^{-1}$ is the inverse of $F$ modulo $G$. Then, $P$ can be expressed as $P=(\alpha \cdot F) \cdot(\beta \cdot F) \cdot F^{-1} \bmod G=\alpha \cdot \beta \cdot F \bmod G$.

### 2.2 Bipartite modular multiplication

Kaihara and Takagi first have proposed a bipartite modular multiplication using Montgomery algorithm and then they have extended their method [10, 11]. It splits the operand multiplier into two parts that can be processed simultaneously to increasing the calculation speed. We briefly review the main idea of their method.

Let the modulus $M$ be an $n$-digit integer, where the radix of each digit is $r=2^{t}$ and let a Montgomery radix $F=r^{k}$ where $0 \leq k \leq n$. Consider the multiplier $Y$ to be split into two parts $Y_{H}$ and $Y_{L}$ so that $Y=Y_{H} R+Y_{L}$. Then, the Montgomery multiplication modulo $M$ of the integers $X$ and $Y$ can be computed as follows:

$$
\begin{aligned}
X * Y & =X Y F^{-1} \bmod M \\
& =X\left(Y_{H} F+Y_{L}\right) F^{-1} \bmod M \\
& =\left(\left(X Y_{H} \bmod M\right)+\left(X Y_{L} F^{-1} \bmod M\right)\right) \bmod M .
\end{aligned}
$$

The left term of the last equation, $X Y_{H} \bmod M$, can be calculated using the classical modular multiplication that processes the upper part of the split multiplier $Y_{H}$. The right term, $X Y_{L} F^{-1} \bmod M$, can be calculated using the Montgomery algorithm that processes the lower part of the split multiplier $Y_{L}$. Both calculations can be processed simultaneously. Since the split operands $Y_{H}$ and $Y_{L}$ are shorter in length than $Y$, the calculations $X Y_{H} \bmod M$ and $X Y_{L} F^{-1} \bmod M$ are performed faster than $X Y F^{-1} \bmod M$.

They have focused on application in the integer and mentioned the usability of their method in the finite field. Thereafter, Kim and Jeon [5, 7] adapted their bipartite technique to the modular multiplication in the finite fields for reducing the latency and proposed multipliers over $\operatorname{GF}\left(2^{m}\right)$.

### 2.3 Modular exponentiation

The exponentiation is a crucial part of modern cryptographic algorithms. The most commonly used algorithms for exponentiation are the binary methods (also called square-and-multiply methods) [15]. Its basic idea is to compute modular exponentiation by using the binary expression of exponent $E$ and the exponentiation
algorithm has the left-to-right (MSB) method and right-to-left method (LSB). The right-to-left method can be used to compute modular squaring and modular multiplication concurrently. The right-to-left binary square and multiply algorithm is represented as Algorithm 1 which computes the modular exponentiation starting from the LSB of the exponent and proceeding to the left.

Algorithm 1. LSB binary modular exponentiation algorithm in $\operatorname{GF}\left(2^{m}\right)$
Input: $M, E=\sum_{i=0}^{m-1} e_{i} 2^{i}$ (where $e^{i} \in\{0,1\}$ ), $G$
Output: $C=M^{E} \bmod G$
Step 1. $C=1$;
Step 2. $S=M$;
Step 3. for $i=0$ to $m-1$ do $\{$
Step 4. if $\left(e_{i}=1\right)$ then $C=C \times S \bmod G$;
Step 5. $S=S \times S \bmod G$;
Step 6. \}

Note that modular squaring and multiplication can be performed simultaneously in order to improve speed of exponentiation [6, 12, 13, 14]. Using the common-multiplicand method [13, 14], Choi and Lee [6] proposed the combined systolic multiplier/squarer that computes modular squaring and multiplication concurrently instead of computing them separately for the LSB-first exponentiation.

## 3 Proposed unified multiplication and squaring

In this section, we propose a unified algorithm to concurrently perform multiplication and squaring over $G F\left(2^{m}\right)$. We adopt the bipartite modular multiplication concept $[10,11,5,7]$ to decrease the latency required for calculating multiplication and squaring over finite fields. Using common-multiplicand method [6, 13, 14], we also decrease the space complexity by deriving common operations from bipartite parts.

Now, we will derive a bipartite algorithm for performing multiplication and squaring over $G F\left(2^{m}\right)$ in parallel. It is well known that $x^{m} \bmod G=\sum_{j=0}^{m-1} g_{j} x^{j}$ and $x^{-1} \bmod G=x^{m-1}+\sum_{j=1}^{m-1} g_{j} x^{j-1}$. Let $k=\lfloor m / 2\rfloor$ and $l=\lceil m / 2\rceil$. For deriving an efficient parallel architecture, we choose the Montgomery factor, $F=x^{\lfloor m / 2\rfloor}=$ $x^{k}$ as selected in [5, 7]. Then, we can derive the following formula for the Montgomery multiplication $P$ and squaring $S$ over $G F\left(2^{m}\right)$.

$$
\begin{align*}
P= & A \cdot B \cdot F^{-1} \bmod G=A \cdot B \cdot x^{-k} \bmod G \\
= & {\left[b_{0} A x^{-k}+b_{1} A x^{-k+1}+\cdots+b_{k-2} A x^{-2}+b_{k-1} A x^{-1}\right.} \\
& \left.+b_{k} A+b_{k+1} A x^{1}+\cdots+b_{m-2} A x^{-k+m-2}+b_{m-1} A x^{-k+m-1}\right] \bmod G \\
= & \sum_{i=1}^{k} b_{k-i} A x^{-i} \bmod G+\sum_{i=0}^{l-1} b_{k+i} A x^{i} \bmod G .  \tag{1}\\
S= & A \cdot A \cdot F^{-1} \bmod G=A \cdot A \cdot x^{-k} \bmod G \\
= & {\left[a_{0} A x^{-k}+a_{1} A x^{-k+1}+\cdots+a_{k-2} A x^{-2}+a_{k-1} A x^{-1}\right.} \\
& \left.+a_{k} A+a_{k+1} A x^{1}+\cdots+a_{m-2} A x^{-k+m-2}+a_{m-1} A x^{-k+m-1}\right] \bmod G
\end{align*}
$$

$$
\begin{equation*}
=\sum_{i=1}^{k} a_{k-i} A x^{-i} \bmod G+\sum_{i=0}^{l-1} a_{k+i} A x^{i} \bmod G . \tag{2}
\end{equation*}
$$

As seen in (1) and (2), the multiplication result $P$ and squaring result $S$ can be divided into two parts, respectively. One is based on the negative powers of $x$ and the other is based on the positive powers of $x$. $P$ can be denoted by $P=Q+R$, where $Q=\sum_{i=1}^{k} b_{k-i} A x^{-i} \bmod G$ and $R=\sum_{i=0}^{l-1} b_{k+i} A x^{i} \bmod G$. Similarly, $S$ can be denoted by $S=T+U$, where $T=\sum_{i=1}^{k} a_{k-i} A x^{-i} \bmod G$ and $U=$ $\sum_{i=0}^{l-1} a_{k+i} A x^{i} \bmod G$.

If Montgomery multiplication and squaring are executed concurrently, the components for the common operations can be shared and used only once for Montgomery multiplication and squaring in order to reduce the area complexity. We can derive the common operations, $A x^{-i} \bmod G$ and $A x^{i} \bmod G$, in each bipartite equation from (1) and (2).

For the derived common operations, we define $\bar{A}^{(i)}=A x^{-i} \bmod G(1 \leq i \leq k)$ and $A^{(i)}=A x^{i} \bmod G(0 \leq i \leq l-1)$. Then the equations can be expressed as $\bar{A}^{(i)}=\sum_{j=0}^{m-1} \bar{a}_{j}^{(i)} x^{j}$ and $A^{(i)}=\sum_{j=0}^{m-1} a_{j}^{(i)} x^{j}$, where $\bar{A}^{(0)}=A^{(0)}=A$. By using $x^{m} \bmod G=\sum_{j=0}^{m-1} g_{j} x^{j}$ and $x^{-1} \bmod G=x^{m-1}+\sum_{j=1}^{m-1} g_{j} x^{j-1}, \bar{A}^{(i)}$ and $A^{(i)}$ are rewritten as

$$
\begin{gather*}
\bar{A}^{(i)}=\bar{A}^{(i-1)} x^{-1} \bmod G=\sum_{j=0}^{m-1}\left(\bar{a}_{j+1}^{(i-1)}+\bar{a}_{0}^{(i-1)} g_{j+1}\right) x^{j}  \tag{3}\\
A^{(i)}=A^{(i-1)} x \bmod G=\sum_{j=0}^{m-1}\left(a_{j-1}^{(i-1)}+a_{m-1}^{(i-1)} g_{j}\right) x^{j} \tag{4}
\end{gather*}
$$

Also, using the formulas of $\bar{A}^{(i)}$ and $A^{(i)}$, the terms $Q, R, T$, and $U$ are represented by the following equations. For deriving the identical structure, we add $z \bar{A}^{(0)}$ to $Q$ and $T$, where $z=0$.

$$
\begin{gather*}
Q=\sum_{i=1}^{k} b_{k-i} A x^{-i} \bmod G=z \bar{A}^{(0)}+\sum_{i=1}^{k} b_{k-i} \bar{A}^{(i)}  \tag{5}\\
R=\sum_{i=0}^{l-1} b_{k+i} A x^{i} \bmod G=\sum_{i=0}^{l-1} b_{k+i} A^{(i)}  \tag{6}\\
T=\sum_{i=1}^{k} a_{k-i} A x^{-i} \bmod G=z \bar{A}^{(0)}+\sum_{i=0}^{k} a_{k-i} \bar{A}^{(i)}  \tag{7}\\
U=\sum_{i=0}^{l-1} a_{k+i} A x^{i} \bmod G=\sum_{i=0}^{l-1} a_{k+i} A^{(i)} . \tag{8}
\end{gather*}
$$

From (5) to (8), the recurrence equations of $Q, R, T$, and $U$ can be formulated as

$$
\left.\begin{array}{c}
Q^{(i)}= \begin{cases}Q^{(i-1)}+z \bar{A}^{(i-1)}, & \text { for } i=1 \\
Q^{(i-1)}+b_{k-i+1} \bar{A}^{(i-1)}, & \text { for } 2 \leq i \leq k+1,\end{cases} \\
R^{(i)}=R^{(i-1)}+b_{k+i-1} A^{(i-1)}, \\
\text { for } 1 \leq i \leq l,
\end{array}\right\} \begin{array}{ll}
T^{(i-1)}+z \bar{A}^{(i-1)}, & \text { for } i=1 \\
T^{(i-1)}+a_{k-i+1} \bar{A}^{(i-1)}, & \text { for } 2 \leq i \leq k+1,  \tag{12}\\
U^{(i)}=U^{(i-1)}+a_{k+i-1} A^{(i-1)}, & \text { for } 1 \leq i \leq l,
\end{array}
$$

where $Q^{(0)}=R^{(0)}=T^{(0)}=U^{(0)}=0$ and $Q^{(i)}=\sum_{j=0}^{m-1} q_{j}^{(i)} x^{j}, R^{(i)}=\sum_{j=0}^{m-1} r_{j}^{(i)} x^{j}$, $T^{(i)}=\sum_{j=0}^{m-1} t_{j}^{(i)} x^{j}$, and $U^{(i)}=\sum_{j=0}^{m-1} u_{j}^{(i)} x^{j}$ are $i$ th intermediate results.

The equations $\{(3),(9),(11)\}$ and $\{(4),(10),(12)\}$ can be simultaneously executed because there are no data dependency between computations of $\left\{\bar{A}^{(i)}, Q^{(i)}, T^{(i)}\right\}$ and $\left\{A^{(i)}, R^{(i)}, U^{(i)}\right\}$. Therefore, the results of multiplication and squaring are represented as follows:

$$
\begin{equation*}
P=Q^{(k+1)}+R^{(l)} \tag{13}
\end{equation*}
$$

and

$$
\begin{equation*}
S=T^{(k+1)}+U^{(l)} \tag{14}
\end{equation*}
$$

Then, the coefficients of $Q^{(i)}, R^{(i)}, T^{(i)}$, and $U^{(0)}$ can be computed as follows:

$$
\begin{align*}
& q_{j}^{(i)}= \begin{cases}q_{j}^{(i-1)}+z \bar{a}_{j}^{(i-1)}, & \text { for } i=1 \\
q_{j}^{(i-1)}+b_{k-i+1} \bar{a}_{j}^{(i-1)}, & \text { for } 2 \leq i \leq k+1,\end{cases}  \tag{15}\\
& r_{j}^{(i)}=r_{j}^{(i-1)}+b_{k+i-1} a_{j}^{(i-1)}, \quad \text { for } 1 \leq i \leq l,  \tag{16}\\
& t_{j}^{(i)}= \begin{cases}t_{j}^{(i-1)}+z \bar{a}_{j}^{(i-1)}, & \text { for } i=1 \\
t_{j}^{(i-1)}+a_{k-i+1} \bar{a}_{j}^{(i-1)}, & \text { for } 2 \leq i \leq k+1,\end{cases}  \tag{17}\\
& u_{j}^{(i)}=u_{j}^{(i-1)}+a_{k+i-1} a_{j}^{(i-1)}, \quad \text { for } 1 \leq i \leq l, \tag{18}
\end{align*}
$$

where $q_{j}^{(0)}=r_{j}^{(0)}=t_{j}^{(0)}=u_{j}^{(0)}=0$ and $0 \leq j \leq m-1$.


Fig. 1. (a) The semi-systolic array for computing $\{\bar{A}, Q, T\}$ (b) $\mathrm{V}_{j}^{(i)}$ cell

## 4 Proposed systolic arrays for unified multiplication and squaring

Based on the formulation used in the previous section, we present two efficient semi-systolic arrays to compute unified multiplication and squaring in this section.

The semi-systolic arrays for computing $\{\bar{A}, Q, T\}$ and $\{A, R, U\}$ is presented in Fig. 1(a) and Fig. 2(a), which are composed of $m \times(k+1) \mathrm{V}_{j}^{(i)}$ and $m \times l \mathrm{~W}_{j}^{(i)}$ cells, respectively. The circuits of cells in semi-systolic arrays are illustrated in Fig. 1(b) and Fig. 2(b), where the boxed D denotes 1-bit latch (flip-flop). Each $\mathrm{V}_{j}^{(i)}$ cell employs three 2-input AND gates, three 2-input XOR gates, and four 1-bit


Fig. 2. (a) The semi-systolic array for computing $\{A, R, U\}$ (b) $\mathrm{W}_{j}^{(i)}$ cell


Fig. 3. The module for computing $Q+R$ and $T+U$
latches in order to compute $\bar{a}_{j}^{(i)}, q_{j}^{(i)}$, and $t_{j}^{(i)}$ in (3), (15) and (17). Similarly, each $\mathrm{W}_{j}^{(i)}$ cell employs three 2-input AND gates, three 2-input XOR gates, and four 1-bit latches in order to compute $a_{j}^{(i)}, r_{j}^{(i)}$, and $u_{j}^{(i)}$ in (4), (16) and (18).

Fig. 3 shows a module for computing $Q^{(k+1)}+R^{(l)}$ and $T^{(k+1)}+U^{(l)}$ which includes $2 m 2$-input XOR gates and $2 m$ boxed $\mathrm{D}^{*}$ components, where the boxed $\mathrm{D}^{*}$ denotes 1-bit latch only if $m$ is even, otherwise it is ignored. The modules for computation of $\{\bar{A}, Q, T\}$ and $\{A, R, U\}$ takes $k+1$ and $l$ clock cycles, respectively. If $m$ is odd, $k+1=l$. Otherwise, $k=l$. Therefore, if $m$ is even, 1 -bit latches are required at input lines of $R^{(l)}$ and $U^{(l)}$ before the computation of $Q^{(k+1)}+R^{(l)}$ and $T^{(k+1)}+U^{(l)}$ in order to synchronize them.

The efficient unified architecture for Montgomery multiplication and squaring over $G F\left(2^{m}\right)$ is depicted in Fig. 4. The latency of the proposed architecture requires $0.5 m+2$ clock cycles. Each clock cycle takes delays of one 2-input AND gate, one 2-input XOR gate, and one 1-bit latch. The space complexity of this architecture requires $3 m^{2}+3 m$ 2-input AND gates, $3 m^{2}+5 m 2$-input XOR gates, and $4 m^{2}+4 m$ 1-bit latches.

The $\mathrm{V}_{j}^{(i)}$ cell calculates equations (3), (15), and (17) and the $\mathrm{W}_{j}^{(i)}$ cell calculates equations (4), (16), and (18). As we can see from Fig. 1(b) and Fig. 2(b), the $\mathrm{V}_{j}^{(i)}$ cell and the $\mathrm{W}_{j}^{(i)}$ cell perform identical function with different inputs. Therefore, one systolic array in Fig. 5 can calculate equations (3), (15), and (17) at the first round and equations (4), (16), and (18) at the second round, respectively. The Fig. 6 shows the module to compute equations (13) and (14). The Fig. 7 shows the
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Fig. 4. The proposed multiplier/squarer over $G F\left(2^{m}\right)$


Fig. 5. The semi-systolic array for computing $\{\bar{A}, Q, T\}$ and $\{A, R, U\}$


Fig. 6. The module for computing $Q+R$ and $T+U$
unified architecture for Montgomery multiplication and squaring over $G F\left(2^{m}\right)$, where $m$ is odd. When $m$ is even, it has similar structure. The space complexity of Fig. 7 is reduced by about half compared to Fig. 4.


Fig. 7. The proposed area-efficient multiplier/squarer over $G F\left(2^{m}\right)$

## 5 Complexity analysis and conclusion

As mentioned in subsection 2.3, Montgomery multiplication and squaring can be performed in parallel in order to perform fast modular exponentiation. It can be implemented by the unified multiplier/squarer or by two multipliers. Recently, Choi and Lee [6] proposed the combined systolic array for performing multiplication and squaring in parallel. Kim and Jeon [5] proposed a semi-systolic multipliers using bipartite method. Also they proposed an area-efficient semisystolic multiplier using bipartite method in [7]. A circuit comparison between the proposed and the related multipliers is given in Table I.

For a comparison of the time and area complexity, we utilize the "SAMSUNG STD 1500.13 m 1.2V CMOS Standard Cell Library". Based on this library, we estimated the time and area complexities of the proposed and the related multipliers. As discussed in detail in [6], we adopt that $A_{\text {AND2 }}=6.68, T_{\text {AND2 }}=0.094 \mathrm{~ns}$, $A_{X O R 2}=12.00, T_{X O R 2}=0.167 \mathrm{~ns}, \quad A_{L A T C H 1}=16.00$, and $T_{L A T C H 1}=0.157 \mathrm{~ns}$, where $A_{\text {GATEn }}$ denotes transistor count of an $n$-input gate and $T_{\text {GATEn }}$ denotes the propagation delay of an $n$-input gate.

All multipliers in Table I has the same cell delay of $T_{\text {AND } 2}+T_{X O R 2}+T_{\text {LATCH } 1}$. But the multiplier of Choi and Lee [6] has the latency of $3 m$ clock cycles and the latency of the others is about 0.5 m clock cycles. Compared with the multiplier of Choi and Lee, the proposed multipliers in Fig. 4 and Fig. 7 can reduce the space complexity by $44.4 \%$ and $72.1 \%$ and the AT complexity by $90.7 \%$ and $95.3 \%$, respectively. The proposed multipliers in Fig. 4 and Fig. 7 have about $40.6 \%$ greater space complexity and $40.8 \%$ greater AT complexity, compared with the multipliers in [5] and [7], respectively. But our proposed multipliers can perform multiplication and squaring in parallel for fast modular exponentiation.

In this paper, a semi-systolic architecture for Montgomery multiplication/ square for fast modular exponentiation over finite fields has been presented. We induced an efficient algorithm which is highly suitable for the design of parallel pipelined structures. We expect that our architecture can be efficiently used for

Table I. Comparison of the systolic arrays of multiplication and squaring

| Multipliers | Choi-Lee [6] | Kim-Jeon [5] | Kim-Jeon [7] | Fig. 4 | Fig. 7 |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Array type | systolic | semi-systolic | semi-systolic | semi-systolic | semi-systolic |
| Function | $A B$ and $A^{2}$ | $A B$ | $A B$ | $A B$ and $A^{2}$ | $A B$ and $A^{2}$ |
| Bipartite | X | O | O | O | O |
| Throughput | 1 | 1 | $1 / 2$ | 1 | $1 / 2$ |


| Area complexity |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{AND}_{2}$ | $3 m^{2}$ | $2 m^{2}+2 m$ | $\begin{gathered} \hline m^{2}+0.5 m \\ -0.5 \end{gathered}$ | $3 m^{2}+3 m$ | $1.5 m^{2}+1.5 m$ |
| $\mathrm{XOR}_{2}$ | $3 m^{2}$ | $2 m^{2}+3 m$ | $\begin{gathered} \hline m^{2}+1.5 m \\ -0.5 \end{gathered}$ | $3 m^{2}+5 m$ | $1.5 m^{2}+3.5 m$ |
| Latch | $10 m^{2}$ | $3 m^{2}+3 m$ | $\begin{gathered} 1.5 m^{2}+2 m \\ -0.5 \end{gathered}$ | $4 m^{2}+4 m$ | $2 m^{2}+4 m$ |
| Total transistors | $216.04 m^{2}$ | $\begin{aligned} & 85.36 m^{2} \\ & +97.36 m \end{aligned}$ | $\begin{aligned} & 42.68 m^{2} \\ & +53.34 m \\ & -17.34 m \end{aligned}$ | $\begin{gathered} 120.04 m^{2} \\ +144.04 m \end{gathered}$ | $\begin{gathered} 60.02 m^{2} \\ +116.02 m \end{gathered}$ |


| Time complexity |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Cell delay | 0.418 | 0.418 | 0.418 | 0.418 | 0.418 |
| Latency | $3 m$ | $0.5 m+0.5$ | $0.5 m+1.5$ | $0.5 m+2$ | $0.5 m+2.5$ |
| Total delay | $1.254 m$ | $0.209 m+0.209$ | $0.209 m+0.627$ | $0.209 m+0.836$ | $0.209 m+1.045$ |


| Area-Time complexity |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| AT | $270.91 m^{3}$ | $17.84 m^{3}$ | $8.92 m^{3}$ | $25.09 m^{3}$ | $12.54 m^{3}$ |  |
| complexity |  | $+38.19 m$ | $+37.90 m^{2}$ | $+130.46 m^{2}$ | $+86.97 m^{2}$ |  |
|  |  |  | $+29.82 m$ | $+120.42 m$ | $+121.24 m$ |  |
|  |  |  | -10.87 |  |  |  |

various applications including crypto coprocessor design, which demand highspeed computation, for security purposes.

## Acknowledgments

The present research was conducted by the research fund of Dankook University in 2015.

