A compact, low-power-consumption 5-Gbps OEIC receiver without equalizer fabricated in 0.18-µm CMOS technology

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Abstract: A low-cost, compact 5-Gbps fully integrated CMOS optical receiver without equalizer is fabricated in this paper in a standard 0.18- μ m CMOS technology. The measured responsivity of the DNW-strip-SMPD operating in avalanche mode is 1.4 A/W, while the bandwidth is 2.9 GHz with 11.6 V reverse bias voltage. The application for 5-Gbps very-short-reach optoelectronic integrated circuit (OEIC) receiver with a bit-error rate <10⁻¹² at incident optical power of -4 dBm has been experimentally demonstrated. The core chip area of the OEIC receiver is 0.736 mm by 0.515 mm, and it consumes 96 mW from the 1.8 V supply. Our OEIC receiver has the smallest area and the lowest power consumption in the OEIC receivers reported so far fabricated in 0.18- μ m CMOS technology.

Keywords: fully integrated, equalizer, avalanche mode, optoelectronic integrated circuit, very-short-reach

Classification: Optical systems

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1 Introduction

With the expansion of the market and communication system capacity, and the improvement of the security and reliability of information, electrical connectors are being rapidly replaced by optical fibers for their inferiority in high-frequency loss due to the skin effect and dielectric loss, and channel cross-talk noises [1]. As a feasible way to solve these problems, monolithically integrated optoelectronic integrated circuits (OEICs) have drawn more and more attention.

For short-range (<100 m) optical links over 5 Gbps, 850-nm wavelength is a potential choice by using cost-effective vertical cavity surface emitting lasers (VCSEL) and multimode fiber (MMF) [2]. In addition, as the 850-nm light can be detected by silicon, the standard CMOS-technology-compatible photodetectors (PDs) are expected for monolithic integration to enable the cost-effective implementation of the optical short-distance interconnection. However, CMOS PDs have the disadvantage of the low detection efficiency and bandwidth. This is because the penetration length in silicon at 850 nm is much larger than the typical PN junction depletion width available within CMOS technology and, consequently, the majority of incident photons are absorbed in the P-substrate region where photo-generated carriers transport as slow diffusion currents [3].







Fig. 1. The simplified block diagram of the fabricated OEIC receiver.

To improve the bandwidth of CMOS PDs, spatially-modulated PDs (SMPDs) have been reported [3, 4]. SMPDs employ differential, symmetrical structure through the difference between currents I_{light} and I_{dark} to eliminate slow diffusion current generated in the substrate. However, SMPDs suffer from low responsivity. In order to increase the responsivity, the APDs [5, 6, 7] are proposed. The responsivity can be greatly increased through its intrinsic avalanche multiplication effect. In addition, the bandwidth of the PDs can also be compensated by an external circuit, such as equalizer [8, 9], but it requires additional power, chip area and cost.

In this paper, a low-cost, compact 5-Gbps fully integrated CMOS optical receiver without equalizer is presented. Fig. 1 shows the simplified block diagram of the fabricated OEIC receiver. The receiver is composed of a Deep-N-Well-strip-SMPD (DNW-strip-SMPD), a novel dual negative feedback feed-forward common gate (DNFFCG) differential trans-impedance amplifier (TIA), a modified limiting amplifier with PMOS interleaving feedback, an offset cancellation network (OCN), and an output buffer with 50- Ω load.

2 Receiver circuit design

2.1 CMOS photodetector

The cross-section view of the DNW-SMPD is shown in Fig. 2. In order to reduce external series resistance, the P-Well region and N-Well region are completely covered with P⁺ and N⁺. As the passivation layers above the active region will reflect the incident light, the passivation layers should be removed to avoid the reduction of the responsivity. The shallow trench isolation (STI) oxide is used to increase the breakdown voltage. So a high electric field can be applied in the depletion layer, and the avalanche multiplication effect is improved. The low responsivity of SMPDs can be effectively compensated. In addition, the structure of deep N-well is used. The responsivity can be improved, because the DNW has a deeper junction depth for the lager depletion layer, so more light will be absorbed in the junction. The total active area of the DNW-strip-SMPD is $50 \times 50 \,\mu\text{m}^2$, which consists of 16 p-regions and 16 n-regions covered and uncovered with metal layers for light blocking. The distance of each p-n diode determines the operating speed and the shorter the distance, the faster the speed. Therefore, the minimum size determined by the process is employed to reduce the transit time of photo-generated carriers and improve the bandwidth. The width for P-well (W_P), N-well (W_N), and STI oxide (W_{STI}) are 1.4 µm, 0.86 µm, and 0.36 µm, respectively.







Fig. 2. The cross-section view of the DNW-SMPD.

However, the DNW-SMPD has a large parasitic capacitance, and it will affect the external bandwidth of the photodetector. Therefore, an innovative DNFFCG TIA is designed to broaden the bandwidth of the OEIC receiver, which will be introduced in the following part.

In order to solve some unstable factors caused by the high biased voltage of the PD, two methods are employed: 1) the PD is surrounded by the P⁺ guard ring connecting to the ground; 2) the NMOS transistors and the PMOS transistors of following circuit are designed in the deep N-well and N-well, respectively. It will reduce the noise and separate the unstable factors from the substrate. The schematic diagram is shown in the Fig. 3.



Fig. 3. The Integration of the SMPD and transistors in CMOS technology.

2.2 TIA

As the front-end amplifier, the TIA will determine the overall performance of the system. As the parasitic capacitance and dark current of the PD are introduced at the input of the TIA, the bandwidth and sensitivity will be affected, accordingly. It's very challenging to design TIA with high performance.

For 0.18-µm CMOS technology, some TIAs have reached a transmission rate of 10-Gps or higher [10]. However, for the OEIC system, the transmission rate of 5 Gbps is difficult to be achieved without equalizer, because the intrinsic characteristics limit the performance. In this paper, a novel DNFFCG differential TIA is proposed.

The schematic of the DNFFCG differential TIA is shown in Fig. 4. For the TIA with common-gate structure, the equivalent input resistance can be reduced by increasing the g_m , but at the same time, the power consumption is greatly increased.







Fig. 4. The Circuit schematic of the DNFFCG differential TIA.

In order to obtain a sufficiently large equivalent g_m under a small g_{m4}/g_{m9} , the gainboost technology can be employed with a local feedback stage to provide a large feedback gain. The local feedback stage consists of M₈/M₅, R₈/R₅, M₇/M₆ and R₇/R₆. Besides, two negative feedback loops are also employed to further reduce the input resistance. M₃/M₁₀, M₈/M₅, R₈/R₅, M₇/M₆ and R₇/R₆ form the first negative feedback loop. M₂/M₁, M₈/M₅ and R₈/R₅ come into being another negative feedback loop, and the present of the M₂/M₁ can decrease the equivalent resistance looking from the source of the M₈/M₅. The input resistance of DNFFCG TIA can be expressed by (1). It can be seen from the expression, the resistance can be reduced by increasing g_{m2} and g_{m3} .





Fig. 5. The equivalent small-signal model for DNFFCG TIA circuit.

To thoroughly analyze poles and zeros, an equivalent small-signal model of the DNFFCG TIA circuit is shown in Fig. 5. C_{gs3} and C_{gs4} have been de-coupled between node V_i and V_y according to Miller Theorem with the voltage transfer function from V_i to V_y firstly derived. By solving the small-signal model equations, the approximate transfer function of DNFFCG TIA can be derived:

$$Z_{T,DNFFCG} = \frac{E_3 + E_2 s + E_1 s^2}{(g_4 + C_L s)(Z_1 s^2 + Z_2 s + Z_3)(D_1 s + D_2)}$$
(2)

Where,

$$E_{1} = g_{m4}(C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})$$

$$E_{2} = g_{m4}[g_{8}(C_{gs4} + C_{gs3}) + g_{7}(C_{gs7} + C_{gs2})]$$

$$E_{3} = g_{m4}(g_{7}g_{8} + g_{m7}g_{m8})$$

$$D_{1} = C_{gs8} + C_{in} + k(C_{gs3} + C_{gs4}) = C_{in,tot}$$





$$D_{2} = (g_{m3} + g_{m4}) \left(1 + \frac{g_{m7}g_{m8}}{g_{7}g_{8}} \right) + g_{m8} + g_{m2}g_{m8} \frac{1}{g_{8}} = \frac{1}{Z_{in}}$$

$$Z_{1} = (C_{gs4} + C_{gs3})(C_{gs7} + C_{gs2})$$

$$Z_{2} \approx \frac{(g_{m4} + g_{m8} + g_{m3}) \times [g_{8}(C_{gs4} + C_{gs3}) + g_{7}(C_{gs7} + C_{gs2})] + g_{m2}g_{m8} \times (C_{gs4} + C_{gs3})}{Z_{in}}$$

$$Z_{3} = g_{7}g_{8}$$

Here, g_7 , g_8 , and g_4 are the conductance of R_7 , R_8 , and R_4 . C_L is the equivalent loading capacitance at the output node coming from the secondary circuit and k is the equivalent miller factor of C_{gs3} and C_{gs4} to simplify the analysis.

To a typical complex-pole system $H(s) = \frac{\omega_n^2}{s^2 + 2\xi_{\text{poles}}\omega_n s + \omega_n^2}$, the frequency response of the complex poles can be characterized by the damping coefficient $\xi_{\text{poles}} = Z_2/(2\sqrt{Z_1Z_3})$. In this design, there is a trade-off between the bandwidth extension, the gain overshoot, and settling time, and finally the ξ_{poles} was chosen to be 0.3. In addition, two complex zeros in the denominator should be designed carefully. The complex zeros were arranged near the dominant pole, which can also play the role of expanding the bandwidth. As the frequency response of the complex zeros are opposite with complex poles. To balance these two contrary effects, $\xi_{zeros} = E_2/(2\sqrt{E_1E_3})$ was chosen to be 0.35.

The sensitivity of the whole OEIC system is determined by the responsivity and the noise of the PD as well as the noise introduced by the subsequent circuit. And for the entire subsequent circuit, the noise of the frontend TIA is usually the dominant contributor to the input referred noise. In this design, as DNW-strip SMPD has large parasitic capacitance, the introduction of M_3/M_{10} and M_2/M_1 is needed to reduce input resistance, although it will increase the noise and deteriorate the sensitivity. The equivalent input noise current densities are increased by $6 \text{ pA}\sqrt{\text{Hz}}$ by simulation. However, in order to improve overall bandwidth, appropriate sacrifices can be acceptable without the use of the equalizer. A PD model proposed in [11] is used for simulation. The simulation result is shown in Fig. 6. The bandwidth is 5.1 GHz, while the gain is 50.3 dB Ω .

2.3 Limiting amplifer

As shown in Fig. 1, the output signal of the TIA is amplified to a digital level by a limiting amplifier, and then be delivered to the subsequent data decision and clock recovery circuit. To achieve a high gain and a wide bandwidth, the architecture with cascaded gain stages is widely used, but the severe gain peaking will arise. To solve this problem, [12] proposes an interleaving feedback technique by employing the NMOS differential pairs, and in this design, PMOS differential pairs are used as shown in Fig. 7. PMOS pairs have a better performance for the consistent of 0 and 1 level, because the shunt effect of the PMOS interstage feedback makes the 0 level higher, while the 1 level lower, thereby reducing the burden of charging and discharging. The PMOS interleaving feedback has an auxiliary pull-up effect when the signal is changed from 0 to 1 and an auxiliary pull-down effect when the signal is changed from 1 to 0, while the NMOS interleaving feedback only has the auxiliary pull-down effect when the signal is changed from 1 to 0.







Fig. 6. The simulation AC curves of the DNFFCG TIA with PD model.



Fig. 7. The schematic of the LA circuit.

2.4 Offset cancellation network and output buffer

As the multistage differential amplifiers are cascaded by DC coupling mode, any small device mismatch or asymmetric layout can lead to a serious deviation of the output DC. The DC offset cancellation circuit is needed to stabilize the operating point. Therefore, the feedback loop gain enhanced differential DC offset cancellation circuit is designed as shown in the Fig. 8. In Fig. 8, the low-pass filter is used to extract the output DC level. As the corner frequency must fall in the range of a few tens of kilohertz to eliminate the output droop, the required resistance and capacitance values must be enormous. In order to reduce the chip area, R_f and C_f are realized by PMOS transistors operating in the triode region and NMOS transistors, respectively. Amplifier A_{f1} and A_{f2} not only play the role of isolating low pass network from the output and input node, but also increase the low frequency loop gain.

In the design, an output buffer is included to drive the testing instruments. As the equivalent impedance of the output node is inherently low, the current of the buffer will be very large to maintain a sufficient output swing. Therefore, the transistor sizes of the buffer should also be large. However, it brings too much capacitive loading to the core amplifier, making it very difficult to meet the requirements of the entire system bandwidth. In order to overcome the bandwidth bottleneck, a $f_{\rm T}$ doubler circuit is employed as the output buffer, as shown in Fig. 9. Compared with the single differential amplifier, the input capacitance of the







Fig. 8. The schematic of the feedback loop gain enhanced differential DC offset cancellation circuit.



Fig. 9. The schematic of the output buffer.

 $f_{\rm T}$ doubler is reduced by half, so it can solve the contradiction between drive capacity and capacitive loading.

3 Measured results

Fig. 10(a) shows the chip photograph of the fabricated OEIC receiver. The core chip area of the receiver is about $0.736 \text{ mm} \times 0.515 \text{ mm}$. The power consumption excluding output buffer is about 96 mW with 1.8-V supply voltage. Fig. 10(b) shows the measurement setup for photo-detection frequency response and broadband optical data transmission. Light source is from an 850-nm laser diode directly modulated by an external electro-optic modulator. The modulated optical signals are transmitted through multimode fiber (MMF) and injected into the SMPD using a lensed fiber. The lensed fiber has the spot size of 50 μ m.

Fig. 11 shows the measured current–voltage (I-V) characteristics as a function of reverse bias voltage $V_{\rm PD}$. The dark current and light current will increase more rapidly after the avalanche breakdown occurs at about 11.6 V. The measured responsively of DNW-SMPD is 1.4 A/W. The parasitic capacitance of the DNW-SMPD is around 830 ff. Test result in Fig. 12 shows that the work frequency of the DNW-strip-SMPD is up to 2.9 GHz.

As shown in Fig. 13, the measured results of the trans-impedance gain and 3-dB bandwidth of the OEIC receiver are about 97.1 dB Ω and 3.52 GHz, respectively. Fig. 14 shows the measured BER performance as a function of incident optical power for 5-Gbps optical data. The measured optical sensitivity for BER of











Fig. 10. (a) The chip photograph of the fabricated OEIC receiver (b) measurement setup



Fig. 11. The current–voltage (I-V) characteristics as a function of reverse bias voltage V_{PD} .



Fig. 12. The Measured frequency response of the the DNW-SMPD.

 10^{-12} is -4 dBm. The inset in Fig. 14 shows the measured eye diagram of 5-Gbps data. Table I compares performances of our optical receiver with previously reported 850 nm CMOS OEIC receivers. As can be seen in Table I, for 5 Gbps







Fig. 13. The measured frequency response of the proposed OEIC receiver.



Fig. 14. The measured BER performance as a function of incident optical power, inset shows the eye diagram of 5-Gb/s data at output of the limiting amplifier.

Reference	[13]	[3]	[14]	[15]	This work
CMOS Technology (µm)	0.18	0.18	0.18	0.13	0.18
Core Area (mm ²)	0.72	0.76	NA	NA	0.38
Power (mW)	183	118	50	74	96
Receiver Structure	SML+TIA +EQ+LA	Meshed SML+TIA +LA (9 passive inductors)	SML+TIA +LA	SML+TIA +EQ+LA	SML+TIA +LA
Maximum Data Rate (Gbps)	5	10	2	4.5	5
Sensitivity (BER)	-3 dBm (10 ⁻¹²)	-6 dBm (10 ⁻¹¹)	-8 dBm (10 ⁻⁹)	-4 dBm (10 ⁻¹²)	-4 dBm (10 ⁻¹²)

Table I. Performance comparison of CMOS OEIC receiver





application, our OEIC receiver shows better performance than other types of receivers fabricated in standard 0.18-µm CMOS technology with smaller chip area and lower power consumption.

4 Conclusion

In this paper, a 5-Gbps OEIC receiver without equalizer fabricated in standard 0.18- μ m CMOS technology is presented. A certain amount of sensitivity and gain sacrificed in designing the TIA may be acceptable in order to broaden the bandwidth. In comparison with the OEIC receivers fabricated in a 0.18- μ m CMOS technology reported so far, our OEIC receiver has the highest performance in terms of the area, power consumption, and transmission rate. With the fabricated OEIC receiver, 5-Gbps optical data are successfully transmitted at the input optical power of $-4 \, dBm$ with BER less than 10^{-12} .

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