LETTER

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A closed-loop Sigma-Delta modulator for a tunneling magneto-resistance sensor

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Abstract: In this paper, a high-order Sigma-Delta ($\Sigma\Delta$) modulator in a standard 0.5 µm CMOS technology for a tunneling magneto-resistance sensor (TMR) is presented. The digital output is attained by the interface circuit based on a low-noise chopper front-end and a back-end forth-order Sigma-Delta modulator. The low-noise front-end detection circuit is proposed with correlated double sampling (CDS) technique to eliminate the $1/f$ noise and offset of operational amplifier. The even harmonics is eliminated by fully differential structure. The interface is fabricated in a standard 0.5 µm CMOS process and the active circuit area is about $4 \times 3\,\text{mm}^2$. The modulator chip consumes 9.6 mW from a 5 V supply and the sampling frequency is 6.4 MHz. The modulator can achieve a signal-to-noise ratio (SNR) of 121 dB, an effective number of bits 19.85 bits and a harmonic distortion of 113 dB.

Keywords: tunneling magneto-resistance sensor, interface circuit, chopper instrumentation amplifier, Sigma-Delta

Classification: Integrated circuits

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1 Introduction

Recently, magnetic sensors are widely applied in the medical, aerospace, military and automotive market [1]. The current magnetic sensor is mainly based on Hall-effect, micro-fluxgate, anisotropic magneto-resistance (AMR), giant magneto-resistance (GMR) and tunneling magneto-resistance (TMR). Compared with other sensors, TMR sensors with high sensitivity, high linearity and low hysteresis are widely applied [2, 3]. With the development of MEMS, The research on Sigma-Delta interface circuit of micro-machined tunneling magneto-resistance sensor has significant theoretical value and applied benefit [4, 5].

In this work, we propose a forth-order low-noise closed-loop ΣΔ modulator interface circuit based on a tunneling magneto-resistance sensor. The high-resolution TMR2922 sensor element from Multidimension Technologies is applied. This sensor element has a low noise floor of 0.1 nT/Hz$^{1/2}$(@10 Hz) and the forth-order electromechanical system greatly decreases the quantization noise at a relatively low sampling frequency. Tested results and discussions are shown.

2 Magnetic sensor element and interface circuit

2.1 Sensor element

The simplified equivalent model of the tunneling resistance-type magnetic sensor element is shown in Fig. 1. When the magnetization direction is in parallel state, the equivalent resistance is in low state, when the magnetization direction is in antiparallel state, the equivalent resistance is in high state. In order to achieve the higher sensitivity, the Wheastone bridge structure is used in TMR sensors. In this work, the magnetization sensor element operates in a vacuum package with high sensitivity 15 mV/Oe and high resolution less than 0.1 nT/Hz$^{1/2}$(@10 Hz).

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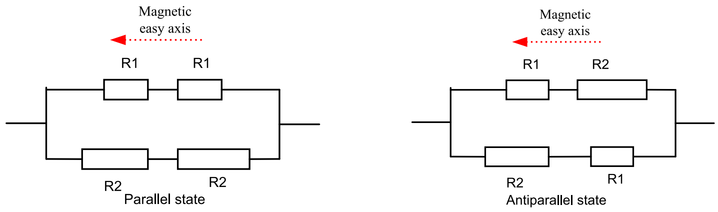

Fig. 1. The equivalent model tunneling resistance-type magnetic sensor

2.2 Interface circuit

The read-out interface circuit is consisted of a current feedback instrumentation amplifier circuit (CFIA) and a Sigma-Delta modulator. For a tunneling magneto-resistance sensor element, a current feedback instrumentation amplifier circuit is used for the preceding stage weak signal detection. The low-frequency $1/f$ noise is mainly problem [6, 7]. In order to eliminate low-frequency noise of sensors and improve the SNR of bandgap reference, the chopper stabilization technique is applied. The analog signals are converted into digital signals by ΣΔ ADC. Fig. 2 shows the whole circuit diagram of Sigma-Delta modulator.

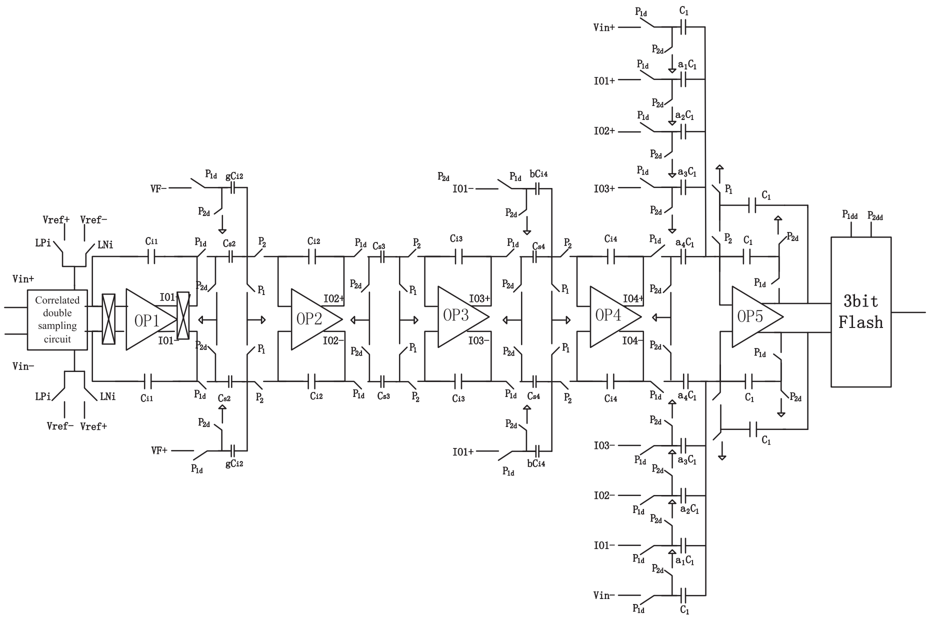

Fig. 2. The forth-order Sigma-Delta modulator circuit

The fully differential structure is applied in the first-stage integrator. The even harmonics is eliminated by fully differential structure of the first-stage integrator. The precision of integrator is affected by the gain, bandwidth and slew rate of the first-stage transconductance operational amplifier [8, 9]. The first-stage fully differential structure integrator circuit is shown in Fig. 3(a). The first-stage transconductance operational amplifier is shown in Fig. 3(b). The gain of operational amplifier is 114.5 dB. The Gain bandwidth product is 82.72 MHz; the phase margin is 83.85°; the slew rate is +66 V/us. The $1/f$ noise can be modulated to the outside of the signal bandwidth by the chopper technology.

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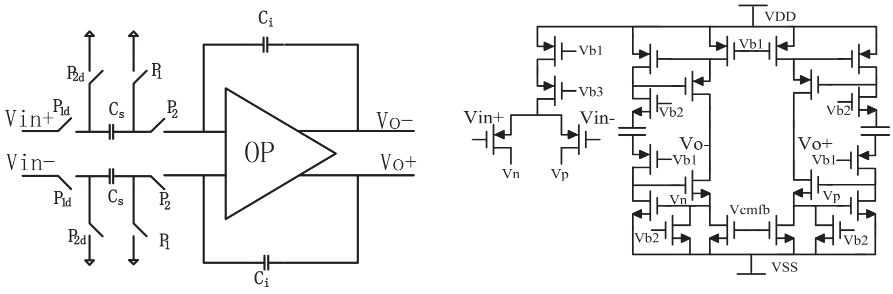
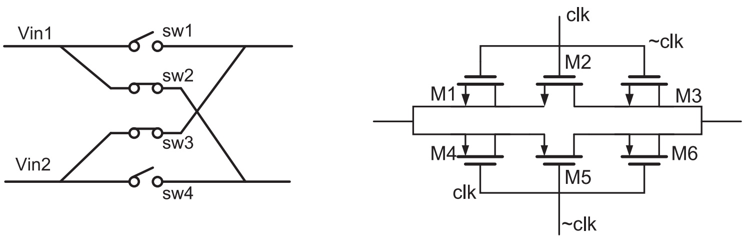


(a) (b)

Fig. 3. (a) The first-stage integrator circuit, (b) The transconductance operational amplifier

The chopper is consisted of four analog switches by the clock control. As shown in Fig. 4(a) in a clock phase, Sw2 and Sw3 are closed, Sw1 and Sw4 are open; in the next phase, Sw1 and Sw4 are closed, Sw2 and Sw3 are open. The chopper switch is composed of n MOSFET and p MOSFET transfer gate as shown in Fig. 4(b).



(a) (b)

Fig. 4. (a) The chopper structure, (b) The transfer gate switch

When the chopper is in the position of the input operational amplifier and the input common-mode voltage is the Middle potential, the transfer gate structure is usually applied in the chopper switch. As shown in Fig. 4, the analog switches (Sw1, Sw2, Sw3, Sw4) are working at the linear region, the working state:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \quad (1)$$

The input transistor gate voltage of chopper is shown as follows:

$$V_{DS}(t) = V_{OS}\exp\left(\frac{-\mu_n C_{ox}\dfrac{W}{L}(V_{GS} - V_{TH})}{C}t\right) = V_{OS}\exp\left(\frac{-1}{R_S C}t\right) \quad (2)$$

After the voltage noise of the analog switch is modulated by chopper-stabilized. The high-frequency (f_{chop}) noise is modulated to a low-frequency noise, the equivalent input voltage noise density is:

$$\bar{V}_n(f) \approx \mu_n C_{ox}\frac{W}{16\pi^2 LC_G(f - f_{chop})}\sqrt{\frac{K_f}{WLC_{OX}(f - f_{chop})}} \cdot V_{OS} \quad (3)$$

$$\frac{W}{L} = \frac{1}{16\pi\mu_n C_{ox} C_G(V_{VCC} - V_{in+} - V_{TH})f_{chop}} \quad (4)$$

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In the equation (4): The voltage noise density of analog switches and chopper stabilized amplifier's input offset voltage are related to the size of analog switches, at the same time the minimum area of the analog switch is limited. In terms of tunneling magneto-resistive sensor weak signal, the $1/f$ noise and KT/C noise are considering in ASIC design for CMOS circuits.

As shown in Fig. 5, in the Phase 1, the reference voltages +Vs and −Vs are applied to the sensor. The capacitor Cc stores the amplified voltage and the error signal V_{error} including the offset and $1/f$ noise of the amplified. The output is given by

$$\Delta V_{out1} = V_{error} - V_s \frac{\Delta R}{R} \tag{5}$$

In the Phase 2, the voltages of sensor and the capacitors are kept at −Vs and +Vs respectively. The output is expressed as

$$\Delta V_{out2} = V_{error} + V_s \frac{\Delta R}{R} \tag{6}$$

When the switch S2 is closed, the offset and low-frequency $1/f$ noise are canceled in the sampling phase. The differential output of the sampling-holding circuit is represented by

$$\Delta V_{out} = \Delta V_{out2} - \Delta V_{out1} = 2V_s \frac{\Delta R}{R} \tag{7}$$

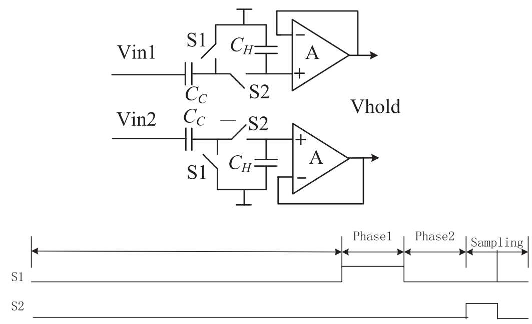

Fig. 5. The correlated double sampling circuit and timing diagram

The low-noise output signal is buffered by a three-stage folded-cascode amplifier A. The parasitic capacitors influence the magnitude of common-mode signal, but the effect on differential signal can be ignored.

3 Experimental results

Because the TMR sensor is apply in the nano-satellite. The technology indicators of the TMR sensor system: the range of measurement is $\pm 10^5$ nT, the sensor resolution is 0.1 nT(@10 Hz), The sensitivity is 15 mV/V/Oe. The signal bandwidth is 20 kHz and the sensor bandwidth is set by 25 kHz. The oversampling ratio (OSR) is 128 and the sampling frequency is 6.4 MHz.

The ΣΔ Sigma-Delta modulator interface circuit is fabricated in a standard 0.5 µm CMOS process and the PCB photograph of the tunneling magneto-resistive sensor interface chip is shown in Fig. 6(a). The 5 V supply is supported by the Agilent E3631 in the circuit. Tektronix AFG3102 function signal generator is used for supplying clock signal. Agilent 16804 A is used for collecting the digital signal. Then the digital output signal 16384-point is used to do the Fourier transform by

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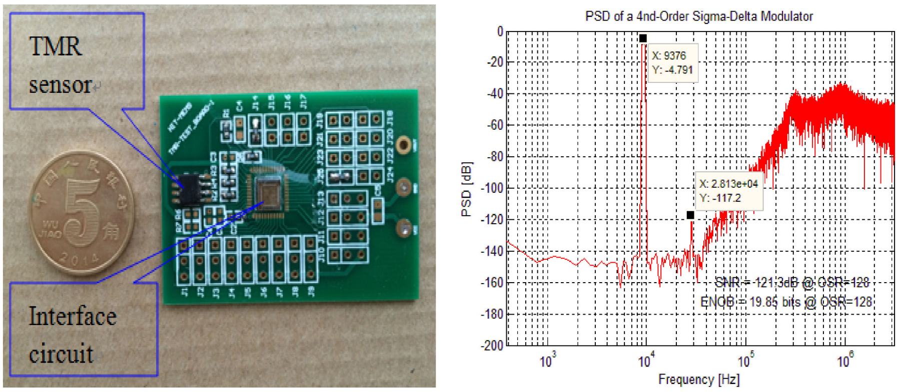

(a) (b)

Fig. 6. (a) The PCB photograph, (b) The PSD of Sigma-Delta modulator output

Matlab. The PSD analysis of the output signal is shown in Fig. 6(b). The full scale range is $\pm 10^5$ nT and the modulator has a dynamic range (DR) of 99.6 dB. The chip consumes 9.6 mW from a 5 V supply and the sampling frequency is 6.4 MHz. The signal-to-noise ratio (SNR) of the modulator can reach 121 dB; the effective number of bits is about 19.85 bits; the harmonic distortion is 113 dB.

The modulator gets a better performance than most of the reported ones in Table I. Compared with Ref. [11] although the FOM ($FOM = P/BW \times 10^{DR/20}$) of this work is smaller due to the disadvantage of technology, there is a higher DR than that in Ref. [11]. This modulator satisfies the application in digital TMR sensor.

Table I. Performance summary and comparison

Parameters	[13]	[10]	[12]	[11]	This design
Bandwidth (Hz)	11 k	0.4 k	10 k	20 k	25 k
Peak SNDR (dB)	62	104.9	-	88.7	93.7
DR (dB)	80	-	70.2	99	99.6
Supply (V)	1.8	5	0.9	3.3	5
Power (mW)	1.7	50	0.06	5.6	9.66
Process (um)	0.5	0.6	0.18	0.18	0.5
FOM	15.4	-	1.85	3.14	4.02

4 Conclusions

A high-order closed-loop Sigma-Delta modulator for a micro-machined tunneling magneto-resistance sensor is proposed in this work. In the Sigma-Delta modulator circuit the low-noise front-end detection circuit is proposed with correlated double sampling technique to eliminate the $1/f$ noise and offset of operational amplifier. The signal-to-noise ratio (SNR) of the modulator can reach 121 dB. The effective number of bits can reach about 19.85 bits; the harmonic distortion can reach 113 dB.

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