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A ECG offset cancelling readout circuit using a current mode feedback loop technique

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Abstract: This paper presents an instrumentation amplifier for ECG signals, compared with the traditional three op amp ECG read instrumentation amplifier, the circuit overcomes the disadvantage of low common mode rejection ratio due to resistance mismatch of the three operational amplifier. At the same time, the circuit uses the inverting integral amplifier as an DC offset feedback circuit to eliminate the offset voltage at the input of the amplifier. This circuit implements the class-AB control circuit to achieve high linearity output. The circuit is compact with few peripheral components. The circuit is designed and implemented by using 0.18 um CMOS Technology. The circuit test results show that the circuit can eliminate the input offset voltage of the 140 mv. And has a DC gain of 40 dB and a common mode rejection ratio (CMRR) of 120 dB at the 2 V supply voltage. THD is −64 dB, and the total input reference noise is 0.78 μVrms, the power consumption is 121.6 μW, the bandwidth is 2 kHz.

Keywords: ECG, instrumentation amplifier, DC offset suppress

Classification: Integrated circuits

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1 Introduction

With the rapid development of smart wearable devices and human health monitoring devices, higher requirements for front-end amplifier design of reading ECG signals have been put forward. The front-end amplifiers are usually operated by instrumentation amplifiers. The ECG signal contains disturbances such as baseline drift and electrode offset voltage. When the system works, the circuit amplifies

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the ECG signal and suppresses the baseline drift and electrode offset voltage, so that the rear stage ADC can obtain high quality ECG signals.

The traditional structure ECG readout circuit uses the three-op amp instrumentation amplifier as the main amplifier, while introducing the integral feedback circuit in the system as a DC offset suppression circuit (DSC) to overcome the DC offset and baseline drift [1, 2, 3, 4]. The main drawback of the three-op amp amplifier is: since the intermediate node contains the input common mode voltage, if there is an offset voltage at the input, the input of the second stage cannot eliminate the offset voltage, the output voltage contains the offset voltage amplified by the second stage amplifier. This can severely limit the CMRR and easily lead to output saturation [5]. In this paper, an instrumentation amplifier based on current feedback is proposed as the main amplifier. Current feedback uses isolation and balancing techniques to obtain high CMRR [6]. Where the isolation characteristics can isolate the input common-mode voltage and avoid common mode voltage at other nodes of the circuit [7, 8]. Based on current feedback instrument amplifier (CFIA), an integral amplifier is added to this structure, the integral amplifier is used as DSC [9]. The circuit introduces a feedback loop from the output of the main amplifier to produce a voltage that is the same as the input offset voltage in amplitude but is reversed in phase, and eliminate offset voltage in the first stage. In addition to suppressing the offset voltage in the input signals, the DSC also introduces a pole to the entire circuit transfer function so that the circuit has a high pass filtering function. The DSC can effectively filter the near-DC component, which can reduce the low frequency signal such as baseline drift in the ECG signal. The circuit structure is verified on the 0.18 um CMOS process, and the verification results show that the proposed circuit functions in accordance with the design. The circuit can be used as the front-end readout circuit of the ECG signal detection system, which provides high quality ECG signals for the post processing circuit.

2 The analysis of the proposed approach

2.1 The drawback of analysis of the three-op amp approaches

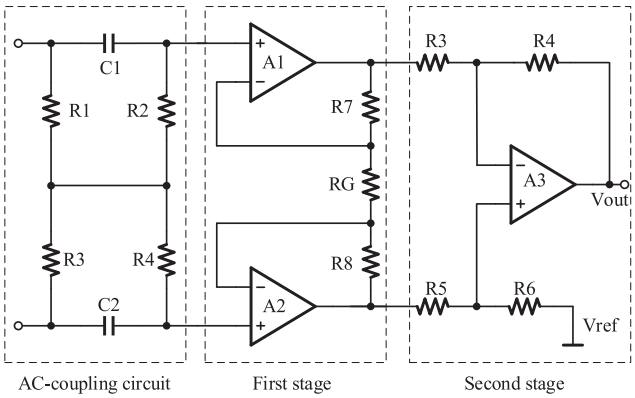

Fig. 1. The conventional three-op amp ECG readout circuit

The traditional ECG readout circuit is shown in Fig. 1. It consists of AC coupling circuit and three-op amp instrumentation amplifier [1, 2]. The ECG detection electrode contains a large DC offset voltage. If the direct access to the input of

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the three operational amplifier instrument amplifier will seriously interfere with the bias point of the amplifier, resulting in the circuit cannot work properly. So it requires an external coupling circuit to isolate the DC offset voltage in the electrode to ensure that the circuit is operating normally. The AC coupling circuit in Fig. 1 is used to isolate the electrode offset voltage. The coupling circuit provides AC coupling for the differential signal and provides a DC path for the bias current. The coupling network has no path to the ground, and in ideal cases the CMRR can be infinitely large. However, in the case of the device, the non-ideal factor and the input parasitic capacitance C_{IN} can cause a deterioration of the CMRR [10]. In order to simplify the calculation, set the resistance value and capacitance value is $R_1 = R_2 = R_3 = R_4 = R$, $C_1 = C_2 = C$, AC coupling circuit $CMRR_{AC}$ is:

$$CMRR_{AC}(s) = \frac{C}{C_{IN}} \times \frac{1 + 2RCs}{\frac{\Delta R}{R} + \frac{\Delta C_{IN}}{C_{IN}} + 2RC\left(\frac{\Delta C}{C} + \frac{\Delta C_{IN}}{C_{IN}}\right)s} \tag{1}$$

ΔR, ΔC, ΔCIN are the amount of error of R, C and CIN, respectively. Analysis of CMRR for three op amp instrumentation amplifiers [11]. It contains two-stage amplifiers, we define a CMRR for the first stage, $CMRR_F$

$$CMRR_F = \frac{1}{1/A_{d1} - 1/A_{d2} + 1/CMRR_2 - 1/CMRR_1} \tag{2}$$

$CMRR_1$ is the CMRR for the amplifier A1, $CMRR_2$ is the CMRR for the amplifier A2. A_{d1}, A_{d2} are the open-loop gain of A1 and A2 amplifiers, respectively. There are two factors that affect the CMRR of the second stage amplifier, one is the resistance matching degree, and the other is the $CMRR_3$ of the operational amplifier A3 itself. The resistance of the CMRR is:

$$CMRR_R = \frac{1}{2}\frac{2R_4R_6 + R_4R_5 + R_3R_6}{R_3R_6 - R_4R_5} \tag{3}$$

$CMRR_R$ represents the CMRR of the resistance of the second stage circuit. The CMRR of the second stage amplifier is given by:

$$\frac{1}{CMRR_S} = \frac{1}{CMRR_R} + \frac{1}{CMRR_3} \tag{4}$$

Finally, the whole circuit of the $CMRR_T$ is:

$$\frac{1}{CMRR_T} = \frac{1}{CMRR_{AC}} + \frac{1}{CMRR_F} + \frac{1}{CMRR_S} \tag{5}$$

From the above analysis, it can be seen that the non-ideal factors of AC coupling circuit, the matching of the first-stage amplifier and the parasitic capacitance of the transistor, the second-order circuit resistance matching and the amplifier performance will cause the CMRR of the whole circuit decreased.

2.2 The principle of the proposed approach

Fig. 2(a) shows a CFIA, the first stage is composed of two identical transconductance input stages, and the second stage is the transimpedance output stage. Each transconductance input stage converts the input signal voltage into current and suppresses all common mode voltages. The input transconductance Gm2 has the same internal circuit structure as the Gm1, the feedback network makes the input

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voltage of the Gm2 equal to that of the Gm1, so that the current matching between the Gm1 and the Gm2 can be realized.

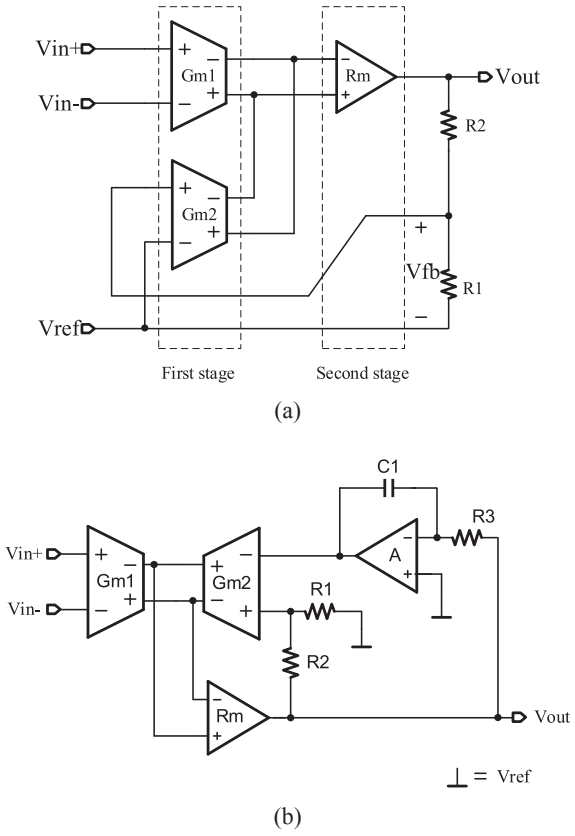

Fig. 2. (a) Current feedback instrumentation amplifier block diagram (b) The CFIA with the DSC block diagram

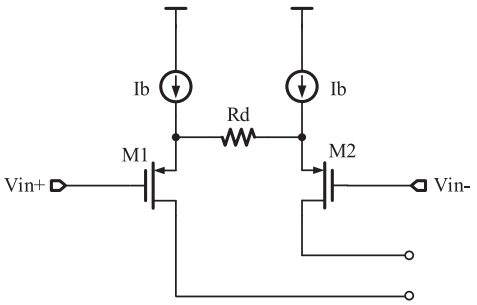

Fig. 3. The circuit diagram of the transconductance

The Gm_1 output current equal to the Gm_2 suction current. The circuit gain is:

$$Av = (Gm_1/Gm_2) \cdot (1 + R_2/R_1) \tag{6}$$

Because of the high input impedance and internal bias current source, the Gm_1 and Gm_2 can isolate the input common mode voltage and prevent the input common mode voltage from interfering with other circuits. Its variation will only cause a small change in the Gm_1 output current. The output voltage is not affected greatly, so the CMRR of the CFIA is higher [8]. Fig. 3 is the transconductance designed in this paper. It is the implementation circuit of Gm_1, Gm_2 corresponding to the part of Fig. 2(a). The CFIA of the CMRRC [12] shown in Fig. 3 is:

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$$CMRR_C = \frac{2}{3\lambda_i}\left(1 + \frac{g_{mi}R_d}{2}\right)\frac{\sqrt{W_iL_i}}{A_{VTP}} \tag{7}$$

λ_i is the channel length modulation coefficient of the input transistors. g_{mi} is the small signal transconductance of the input transistors. W_i and L_i are the gate width and the gate length of the input transistor, respectively. A_{THP} is the variation factor of the threshold voltage of the input transistor. It is a process-dependent constant. Therefore, the CFIA's CMRR is determined only by the parameters of the internal device, independent of the external device.

The traditional structure uses the AC coupling circuit to isolate the offset voltage of the electrode and enlarge the tolerance range of the input offset voltage. In this paper, the source attenuation resistor Rd is used to reduce the influence of the offset voltage on the input transistors. Setting resistance values is $R_d \gg 1/g_{mi}$, the input equivalent transconductance Gm_1, Gm_2 is:

$$Gm_{1,2} = \frac{1}{Rd + 2/g_{mi}} \approx \frac{1}{R_d} \tag{8}$$

This design increases the input offset voltage range of the input transistor, allowing the circuit to directly process the ECG signal containing the electrode offset voltage. Although the input stage has a large input offset voltage range, the electrode offset voltage will go through the circuit to amplify as the input signal for the second stage and reduce the output dynamic range, so it is necessary to suppress these disturbances on the basis of the CFIA. In this paper, the DSC is used to suppress interference. As shown in Fig. 2(b), when a DC offset voltage occurs at the input of the Gm1, the output current of Gm1 is not equal to the Gm2's inhalation current, this produces an error current. The error current is converted from the internal compensation capacitor Cm integral to the output offset voltage, which causes the common mode component of the output voltage to deviate from the reference voltage. The DSC integrates this deviation. The generated voltage is the same as the DC offset of the Gm1 input in amplitude but is reversed in phase. The current between the transconductance is matched. Therefore, the offset is eliminated.

3 The implementation of the proposed approach and circuit design

3.1 The circuit implementation

Fig. 4 is a complete circuit diagram of the CFIA designed in this paper. It is the implementation circuit of Gm_1, Gm_2 and Rm corresponding to each part of Fig. 2(a). The integral amplifier A in Fig. 2(b) is the same as the CFIA circuit, but the integral amplifier contains only one transconductance. This circuit has two high impedance points, so it is a two-stage amplifier. It contains a Class-AB output transistor that provides rail-to-rail output. In order to maintain a better linearity at larger output amplitudes, a class-AB control circuit is used to clamp the output transistor at the rail-to-rail output to maintain high linearity. The M1–M4 is the input transistor, the Rd is the source attenuation resistor, and the I_b provides current bias for the input stage. The M5–M8 and M13–M16 are the Nmos current summing circuit and the Pmos current summing circuit. The M9–M10 is a floating current

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source that provides bias for the two summing circuits. The M11–M12 and M17–M20 are the class-AB control circuits. The M11–M12 is the same structure as the floating current source, and the M17–M20 consists of two stacked diode structures. The Cm_1 and Cm_2 are the Miller compensation capacitors. The M21 and M22 are the class-AB output transistors.

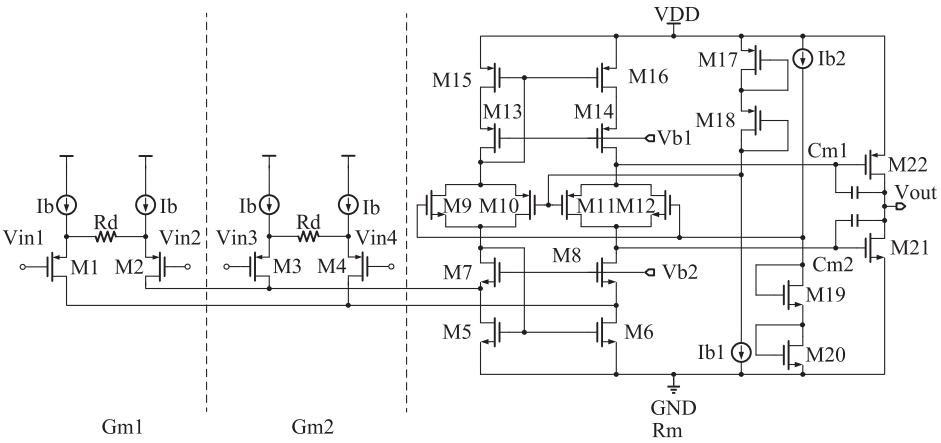

Fig. 4. The complete circuit diagram of the CFIA

3.2 ECG signals frequency response and noise analysis

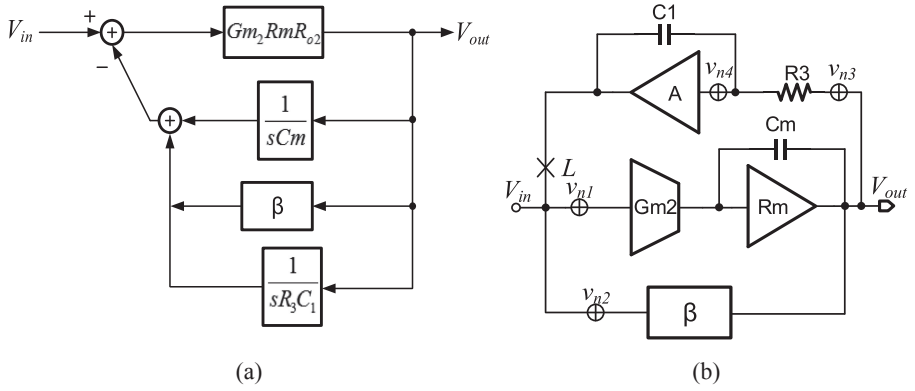

Fig. 5. (a) System signal flow diagram
(b) Equivalent diagram of frequency response and noise analysis

The DSC is added to the circuit, which brings stability and noise problems. This must be analyzed in detail. As shown in Fig. 5(a), it is a simplified signal flow diagram of the circuit. It represents the influence of the DSC and the internal capacitance on the frequency response of the circuit, and the DSC can be seen to make the amplitude frequency response of the circuit have a high pass filtering function. The following specifically calculates the frequency response and noise characteristics. As shown in Fig. 5(b), cut off the loop from node L and the input ground of the Gm_1 is grounded, and the loop gain is obtained:

$$Gain_{loop} = \frac{Gm_2RmR_{o2}}{1+sRmR_{o2}Cm} \cdot \frac{1+s\beta R_3C_1A/(1+\beta)}{(1+sR_3C_1A)/(1+\beta)}, \quad \beta = \frac{R_1}{R_1+R_2} \tag{9}$$

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A is the gain of the DSC. Rm is the gain of the transimpedance stage. β is the resistance feedback coefficient, R_{o2} is the output impedance of Rm. Cm is the CFIA internal Miller compensation capacitor. The closed-loop transfer function is:

$$A_{closed} = \frac{Gm_1}{Gm_2} \cdot \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/sR_3C_1} \tag{10}$$

Fig. 5(b) also contains sources of circuit noise, V_{n1} is the input noise of the main amplifier, and V_{n2} is the equivalent noise of the resistor network. V_{n3} and V_{n4} are the noise of the R_3 and the noise of the amplifier A respectively. So the total input reference noise of the circuit is:

$$v_{in\_noise} = v_{n1} + v_{n2} + \left(v_{n3} + \frac{v_{n4}sR_3C_1}{1 + sR_3C_1}\right) \Big/ A_{closed} \tag{11}$$

Eq. (11) shows that the noise introduced by the DSC has little effect on the noise of the whole system, and the main source of noise is in the main amplifier and the feedback loop.

3.3 Class-AB output implementation

The Rm contains a class-AB output stage circuit [13]. Fig. 6 is a simplified structural diagram. There are two transconductance linear rings, one is M17, M18, M11, M22, the other is M19, M20, M12, M21, the two loop to determine the output transistor quiescent current. Transistors M11 and M12 form a floating class-AB control circuit. Under static conditions, the class-AB control circuit M11 and M12 have the same quiescent current [14]. Thus, the quiescent current of the output transistors can be obtained:

$$I_q = \left(\frac{W}{L}\right)_{21} \Big/ \left(\frac{W}{L}\right)_{20} \cdot I_{b2} \tag{12}$$

In the dynamic state [15], the signal passes through the front stage circuits CP1 and CP2 a control signals is generated to control the gate terminal voltage of the M16 and M6, so that the current of M11 and M12 changes with the signals. The current changes in the transistors M11 and M12 change the voltage between the nodes A, B, and eventually change the gate terminal voltage of the transistors M21 and M22. When the amplitude of the signal is small, V_{AB} is:

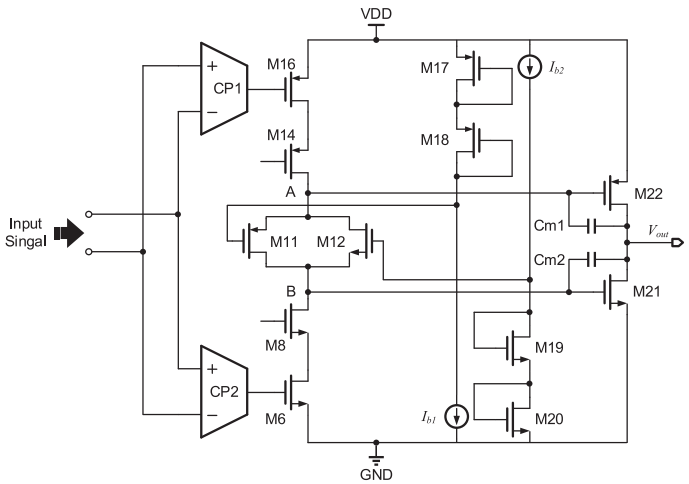

Fig. 6. Class-AB output stage diagram.

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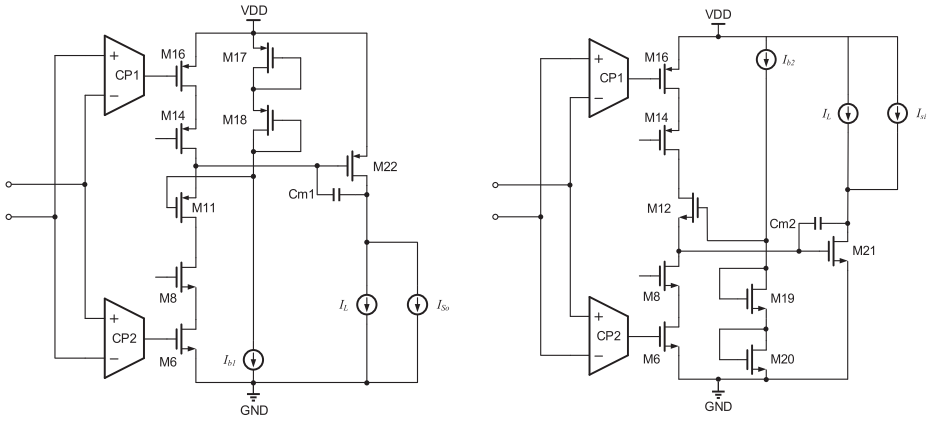
$$V_{AB} = VDD - |V_{GS22}| - V_{GS21} \tag{13}$$

V_{GS22} and V_{GS21} are the gate-source voltages of transistors M22 and M21. When the amplitude of the signal is small, the M21 and M22 operate normally and are not clamped by the class AB control circuit. The V_{GS22} and V_{GS21} are approximately equal, so V_{AB} is a constant. When the amplitude of the signal is large, assuming that the current of M11 is the same as the quiescent current of M14 and M16, M12 is turned off and the equivalent circuit is shown in Fig. 7(a). At this point, the M22 current reaches the maximum, and the M21 current is clamped to the minimum I_L. When the M17 is designed to be equal to the size of M18, M19 and M20, the minimum current is:

$$I_L = 0.34I_q \tag{14}$$

At this time, the output node delivers a larger current outward, V_{AB} decreases, and the gate voltage of the transistor M21 is clamped, and V_{AB} is:



(a) (b)

Fig. 7. (a) Circuit output current equivalent diagram
(b) Circuit extraction current equivalent diagram

$$V_{AB} = VDD - V_{GS21MIN} - |V_{GS22MAX}|, \quad V_{GS21MIN} = \sqrt{\frac{2I_L}{K(W/L)_{21}}} + V_{THP} \tag{15}$$

K is the process parameter, V_{THP} is the threshold voltage of the Pmos transistor, $(W/L)_{21}$ is the wide length ratio of M21, and the $V_{GS22MAX}$ is the gate source voltage of the transistor M22 when the current reaching the maximum. It is known from Eq. (15) that the voltage between AB nodes is reduced. Similarly, when the signal is large, the M11 can be turn off to cause the M21 current to reach the maximum, and the M22 current is clamped to the minimum, and the output node extracts the current outward, as shown in Fig. 7(b). The analysis process is the same as above.

4 Measurement results

Fig. 8(a) is the measurement results of circuit output noise, circuit noise output is about 11 μV/$\sqrt{\text{Hz}}$, the corresponding total input reference noise is 0.78 μVrms with the ECG frequency 0.1–100 Hz and the circuit gain is 40 dB. Fig. 8(b) is a

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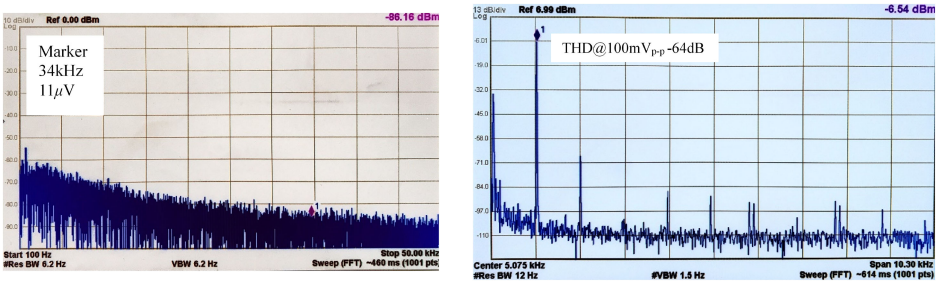
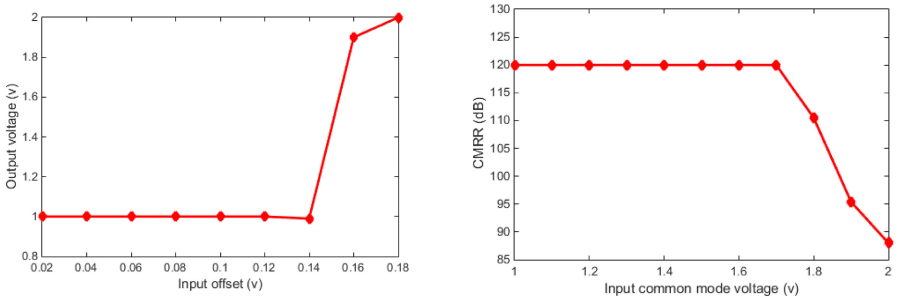
spectrogram of an output signal at 100 mVp-p THD about-64 dB with the normalized output voltage 100 mVp-p. Fig. 9(a) shows how the output common mode voltage varies with the input offset voltage, when the input offset reaches 140 mv, the output is saturated. Fig. 9(b) is a CMRR measurement result, in the circuit input common mode range, the CMRR is about 120 dB, and when the input common mode voltage exceeds 1.8 V, the CMRR begins to decrease. The proposed designs performances compared with other designs are summarized in Table I. In this work, the THD performance of the circuit is −64 dB with the output amplitude is 100 mVpp, compared with other designs, the linearity of the circuit and DC offset voltage handling capacity designed in this paper is obviously improved. And this circuit uses the CFIA, CMRR is higher than other structures. The proposed design was fabricated on a 0.18 µm standard CMOS process, the micrograph of the chip is shown in the Fig. 10. The chip area is 346 µm × 346 µm.



(a) (b)

Fig. 8. (a) Circuit output noise
(b) Circuit output spectrum analysis



(a) (b)

Fig. 9. (a) Characteristic diagram of suppression input offset voltage
(b) CMRR characteristic diagram

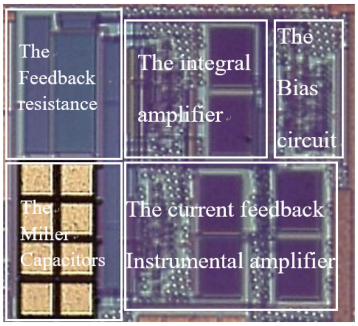


Fig. 10. The prototype of the proposed circuit on chip

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Table I. Performance comparison

	This work	[16]	[17]	[18]
Supply Voltage (V)	1.8	3	1.8	1
CMRR (dB)	120	117	-	80.04
Gain (dB)	40	20	40	38.28
Input referred noise (μVrms)	0.78	0.05 (with choping)	7.37	1.64
DC offset voltage handling capacity (mV)	±140	±50	±45	±18
Current (μA)	60.5	20	4.2	110
THD(dB)@Output voltage	−64@100 mVpp	−47@5 mVpp	-	-
Process (μm)	0.18	0.35	0.18	0.18
off chip dc decoupling component	N	Y	Y	N

5 Conclusion

This paper presents an ECG signal readout circuit, the structure avoids the traditional three op amp structure, in order to adapt to the environment in the ECG signal, the proposed circuit is introduced in the system integral feedback pole, the proposed circuit uses the integral feedback to introduce the pole in the system to form the high pass filtering function, which can eliminate the electrode offset voltage and baseline drift. The measurement results show that the circuit can eliminate the input offset voltage of 140 mv. According to the measurement results, the structure satisfies the ECG signal application environment.

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