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Design of a low-insertion-phase-shift MMIC attenuator integrated with a serial-to-parallel converter

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Abstract: This work presents a monolithic DC~4 GHz 6-bit digital attenuator with low insertion phase shift and attenuation error. Based on GaAs E/D pHEMT process, a serial-to-parallel converter is introduced to decrease the control pads of the chip. In the 16 dB attenuation bit, a switched-path-type topology is employed in order to extend the bandwidth and achieve low insertion phase shift. The attenuator has 0.5 dB resolution and 0~31.5 dB attenuation range. Measurement shows less-than-2.3 dB insertion loss at reference state, and larger-than-14 dB return loss at all states. An rms attenuation error of less-than-0.3 dB and phase-shift-variations less than 2 deg are achieved. The size of the chip is 2.0 mm × 1.7 mm.

Keywords: GaAs E/D pHEMT, serial-to-parallel converter, MMIC, attenuator

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

The attenuator is a key component in phased array radars, the performance and integration of the attenuator affects the entire system. Digital attenuators are used to balance the signals between different channels and supply amplitude conditioning. CMOS attenuators are developed for their characteristics of linearity and low power consumption compared with variable gain amplifiers. Meanwhile, poor return loss and large additive phase-shift constrain the performance of CMOS attenuators [1, 2, 3]. RF-MEMS technology is adopted in attenuator design for wide frequency range and low insertion loss of the switch. However, the switch frequency of the mechanical structure based MEMS switches is distinctly lower than transistor based switches [4, 5]. Taking above factors into consideration, GaAs pHEMT process with high frequency responses [6], and attenuator topologies with low phase shift are adopted for attenuator designs.

As a main application field, phased array system commonly consists of thousands of digital attenuators. For each attenuator, the number of control pads and bonding wires increases with the bits of the chip. For reducing system's weight and size, the combination of serial-to-parallel converter with each digital attenuator is required. After the combination, the number of input pads becomes constant regardless the number of attenuation bits [7].

This work presents a monolithic 6-bit digital attenuator with low loss and phase shift over the bandwidth from DC to 4 GHz. In the 16 dB attenuation bit, a switched-path-type topology is employed in order to extend the bandwidth and achieve low insertion phase shift. GaAs E/D pHEMT process is chosen in our design, and a serial-to-parallel converter is introduced to decrease the control pads of the chip.

2 Design principle and approach

The digital attenuator chip comprises two basic circuits, an attenuator and a serial-

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to-parallel converter. The serial-to-parallel converter consists of logic circuits to provide complementary outputs to FETs which response to serial input. The attenuator transforms the amplitude of RF signals with the control of biasing voltages supplied by the converter.

2.1 Attenuator design

The attenuator is composed by six digital bits with attenuation of 0.5, 1, 2, 4, 8, 16 dB, respectively. The combination of six digital bits provides 64 states with 0.5 dB step and a maximum attenuation of 31.5 dB. The circuit schematic diagram of proposed attenuator is shown in Fig. 1. All switch FETs are implemented in depletion mode. On-state and off-state of each FET is set when 0 V and −3.3 V gate control voltage is given respectively. The gate bias voltage is applied through a mesa-implanted resistor to prevent RF signal leakage to the digital circuit of the serial-to-parallel converter.

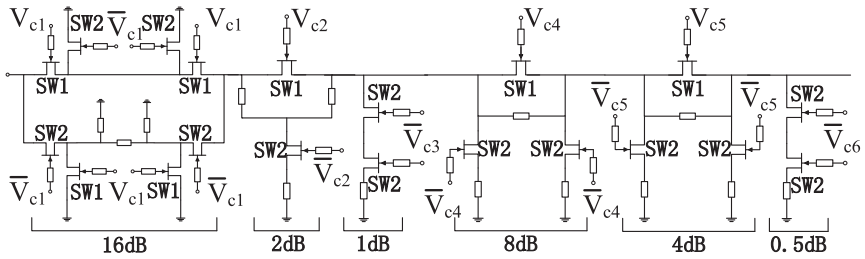

Fig. 1. Circuit configuration of the attenuator.

Simplified T-type network with series-FETs topology is applied in 0.5 dB and 1 dB bits to reduce the insertion loss at the reference state. The two off-state capacitances of the series FETs are equivalent to a smaller capacitor, which increases the isolation of the circuit.

2 dB attenuation bit employs bridge-T-type network with a switch FET (SW1) shunted with two resistors and another FET (SW2) connected to ground through a resistor. At reference state, SW1 is turned on while SW2 is pinched off. The circuit is equivalent to the structure that SW1's on-state resistor shunts with two series resistors. As on-state resistor is mainly determined by the periphery of SW1, a large-size FET is chosen to assure low insertion loss. SW2's periphery is adjusted to find the suitable off-state capacitance to minimize the phase shift between attenuation and reference state. At attenuation state, the states of two FETs are converse from reference state while attenuation is achieved by implemented resistors and SW2's on-state resistor.

4 dB and 8 dB bits adopt pi-type network to attend bigger attenuation [7]. Similarly to the bridge-T-type network, a large-size FET shunted with a resistor and the other two FETs series with a resistor to ground are set as on-state and off-state at reference state, and set conversely at attenuation state.

For the 16 dB attenuation bit, the large attenuation would bring large additive phase shift between reference and attenuation state. However, the phase-shift adjustment of FETs in bridge-T-type network or pi-type network is limited. Therefore, switched-path structure is adopted in our design. Between two SPDT

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switches, one path is constructed by a relatively long microstrip to compensate the additive phase shift, while the other path comprises a pi-type network of resistors. Two paths have a 16 dB attenuation difference. The adoption of this topology avoids the cascade of two 8 dB attenuation bits to obtain better attenuation accuracy over the entire bandwidth and prevent return loss degradation caused by cascade of same topology. In the layout design, one backside via is shared by 4 shunt switches and 2 resistors to make the circuit more compact.

2.2 Serial-to-parallel converter design

Due to the lack of p-type FETs in GaAs technology, complementary devices are not available in digital circuit design. Instead, the GaAs E/D pHEMT process is adopted for digital circuits manufacture. This process is available to have both enhancement-mode and depletion-mode devices on the same substrate. On the basis of GaAs E/D pHEMT process, the DCFL (Direct Coupled FET Logic) logic family is selected to design the digital logic circuits [8]. Depletion pHEMT works as a load to constrain the current while enhancement pHEMT works as a switch for logic function. Compared with other logic families such as SCFL, PCFL, and FFL, DCFL has simple structure and low power dissipation which is suitable for this design.

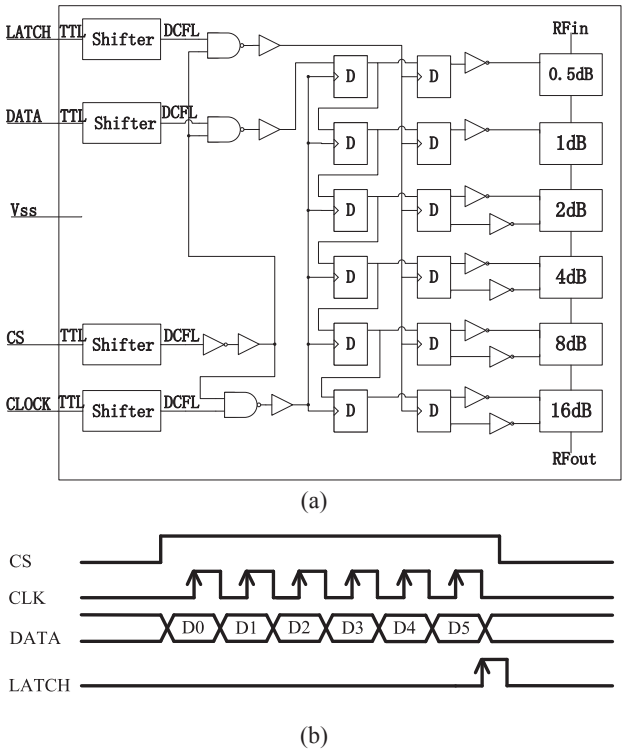

Fig. 2. (a) Digital circuit schematic diagram (b) Waveform of input signals

As Fig. 2(a) shows, the converter consists of 4 input level shifters, a 6-bit shift register, 6 hold registers and 10 output buffers. 6-bit serial data is converted into 6-bit parallel word and delivered to complementary outputs (0 V/−3.3 V) to drive each attenuation bits. The input level shifters accept TTL signals and transform them into voltage levels from +5 V/0 V to 0 V/−3.3 V. The shift register

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combined by 6 D-flip-flops converts the input data into 6 words and loads them into hold registers. Driven by LATCH signal, hold registers receive the words, and the output buffers export differential voltages to attenuator.

Fig. 2(b) shows the waveform of input signals. The chip only works when +5 V voltage level is given to CS. Input data is updated on the rising edge of CLK and hold registers receive data from the shift register on the rising edge of LATCH after 6-bit serial data.

3 Implementation and measurements

The chip is fabricated with 0.5 µm GaAs pHEMT process. Fig. 3 shows the photograph of the MMIC attenuator. The chip size is 2.0 mm × 1.7 mm. A digital

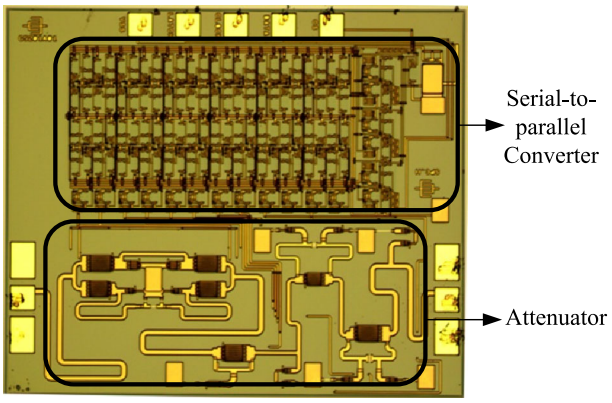

Fig. 3. Photograph of the fabricated 6-bit attenuator.

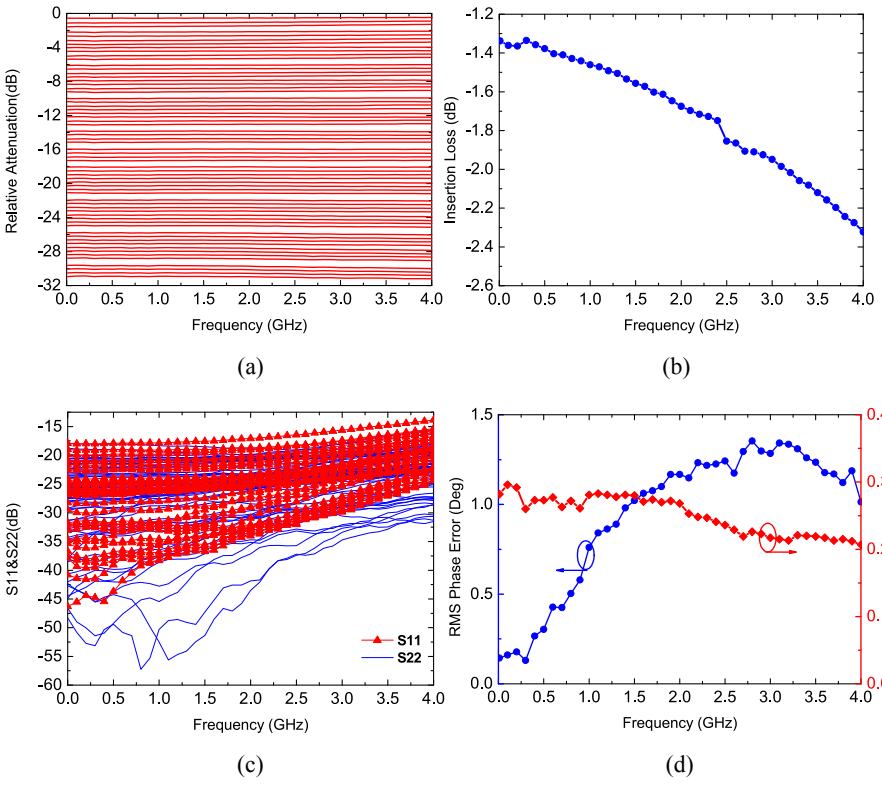

Fig. 4. (a) Relative attenuation of all states (b) Measured insertion loss (c) Measured input and output return loss of all states (d) Rms error of phase and attenuation

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waveform generator (NI-PXI) is employed to supply appropriate digital inputs with a clock signal of 10 MHz. The attenuator is tested by a vector network analyzer (Agilent PNA 5224A) using GSG co-planar microwave probes pitch on probe station.

As shown in Fig. 4(a), the fabricated 6-bit attenuator exhibits excellent flatness of relative attenuation among frequency range from DC to 4 GHz. Fig. 4(b) demonstrates the less-than-2.5 dB reference-state insertion loss in the frequency range. Fig. 4(c) shows the input and output return losses of the attenuator, which are more than 14 dB at all the 64 states. In Fig. 4(d), less-than-1 deg calculated rms phase error and less-than-0.4 dB rms attenuation error are shown. The low rms attenuation error also certifies the flatness of the relative attenuation in Fig. 4(a). Table I summarizes the performance comparison of this work with other published attenuators working in close frequency ranges. The characteristics of the attenuator including insertion loss, phase error, attenuation error, return loss are better than the previous reported attenuators. This work is also implemented with a serial-to-parallel converter, which simplifies the control methods and bonding process of the chip.

Table I. Performance comparison of relevant attenuators

Ref	Device Tech	Atten. Range (dB)	Freq (GHz)	IL (dB)	Phase error (deg)	Atten. error (dB)	Return Loss (dB)	Size (mm^2)
[1]	0.18-µm CMOS	14/4-bit	DC~2.5	<2.5	N/A	<1.5	>11.5	0.45 × 0.42
[9]	0.7-µm GaAs MESFET	31.5/6-bit	0.8~1.8	<4.5	<2.5	N/A	>15	2.35 × 7.0
[10]	0.25-µm SiGe BiCMOS	31/5-bit	0.1~4.5	<5.4	<5.3 (rms)	<0.95 (rms)	>12	1.4 × 0.6
[11]	GaAs 1-micron process	15.5/5-bit	DC~2.0	<2.3	<10	±(0.3 + 3%Att)	>13	1.14 × 0.99
[12]	GaAs pHEMT	31.5/6-bit	DC~3.8	<3	<30	±(0.35 + 5%Att)	>15	SMT 4.0 × 4.0
[13]	0.18-µm GaAs pHEMT	31.5/6-bit	4.5~6.5	N/A	<8 <3.0 (rms)	<0.6 (rms)	>14	3.76 × 4.76
This work	0.5-µm GaAs pHEMT	31.5/6-bit	DC~4	<2.3	<1.5 (rms)	±(0.2 + 2%Att) <0.8 <0.3 (rms)	>14	2.0 × 1.7

4 Conclusion

In this letter, a high-performance 6-bit attenuator integrated with a serial-to-parallel converter over bandwidth from DC to 4 GHz is reported. The implement of the serial-to-parallel converter decreases the number of control signals from 12 to 5. A switched-path-type topology is employed in the 16 dB attenuation bit to extend the bandwidth and achieve low insertion phase shift. The measurement data reveals

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that the attenuator has less-than-2.3 dB insertion loss at reference state, and larger-than-14 dB return loss at all states. An rms attenuation error of less-than-0.3 dB and phase shift variations less-than-2 deg are achieved. The measured results show low insertion loss and high attenuation accuracy of the presented monolithic attenuator.

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