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A power-delay-product efficient and SEU-tolerant latch design

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Abstract: With the increasing high requirements for digital circuits in space application, devices with smaller feature size are put into use, which have more potential suffering from Single Event Upset (SEU) under certain radiation environment. In this paper, we propose a SEU-tolerant latch with low power-delay-product (PDP) that combines a SEU-tolerant cross-coupled structure with isolation operation of flipped state. Negative feedback paths are introduced to help recover the flipped state and can be cut off to speed up the write operation at transparent mode. Furthermore, isolation of flipped state is utilized to achieve better SEU-tolerance. The simulation results with 180 nm and 40 nm CMOS technology show that the proposed latch can achieve outstanding SEU-tolerance ($Q_{critical} > 10$ fC) and a relatively low PDP of 0.0095 fs×J for 40 nm CMOS technology.

Keywords: latch, single event upset, power-delay-product

Classification: Circuits and modules for storage

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1 Introduction

With the feature sizes of devices in CMOS Technology scaling down, supply voltage and node capacitances are decreasing and digital circuits are becoming more susceptible to soft errors caused by ionizing particles [1, 2, 3, 4]. When the inside node of a latch or a flip-flop is stroke by a particle, its correct logic state may be flipped according to the amount of deposited charge. This type of soft error is called Single Event Upset (SEU), which dominates about 90% of soft-error occurrence in modern VLSI circuits and has been considered as the main threat against the reliability of digital circuits [4]. Moreover, the Window of Vulnerability (WOV) of sequential circuits is longer than combinational circuits, so latch circuits are more likely to suffer from SEU than flip-flop circuits and especially call for hardened design [5].

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All the hardening methods against SEU for latch circuits can be classified into three categories: (1) latches with interlocked feedback paths, such as Dual Interlocked Storage Cell (DICE) [6]; (2) latches capable of filtering and masking SEUs by C-Element or Triple-Modular Redundancy (TMR), such as feedback redundant SEU-tolerant latch (FERST) [7]; (3) latches strengthening capacitance of sensitive nodes [9] by increasing transistor sizes, such as Schmitt Trigger latch (ST) [8]. The performance of these hardened methods need to be evaluated in terms of SEU-tolerant ability and area, speed, power as well.

In this paper, we propose a novel SEU-tolerant latch design. It achieves superior SEU-tolerance with even lower power-delay-product (PDP) when compared to some similar designs. Simulations under 180 nm and 40 nm CMOS technology are carried out for performance evaluation.

This paper is organized as follows: Section 2 will give a brief description of some previous designs. Section 3 shows the proposed latch design and the simulation results of the proposed design and comparison with previous designs are shown in Sections 4. Section 5 comes to the conclusion of the paper.

2 Previous designs

As shown Fig. 1, this is a conventional latch. The transmission gate TG1, inverter INV1 and INV2 forms the main transferring path. The transmission gate TG2, inverter INV1 and INV3 forms the feedback loop to latch the stored value. The structure of this latch is simple but it is unhardened, thus it is highly susceptible to SEU.

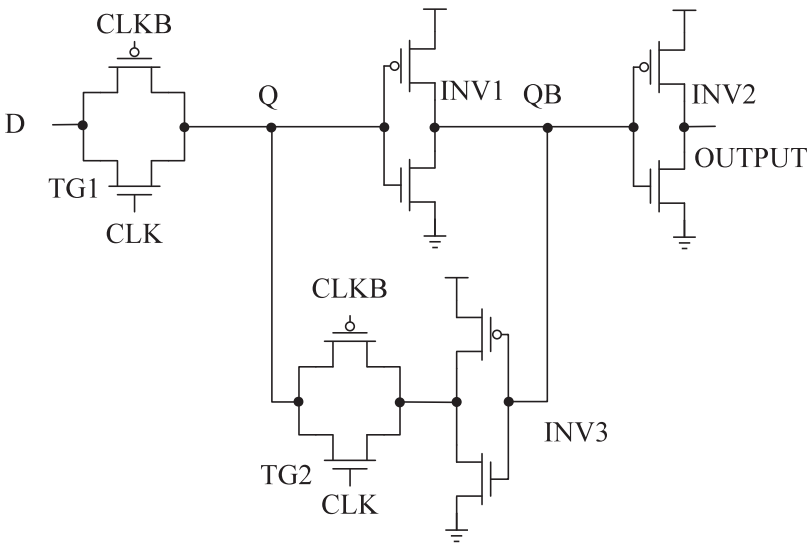

Fig. 1. Conventional latch [10]

DICE latch, illustrated in Fig. 2 is a well-known SEU-tolerant latch for its superior soft-error tolerance. It has a relatively high critical charge when compared with conventional latch. DICE latch is composed of two cross-coupled latches. They interlock with each other to form a steady state. When one of the four logic values flips caused by injected particle, other three nodes are able to help it recover to its normal state.

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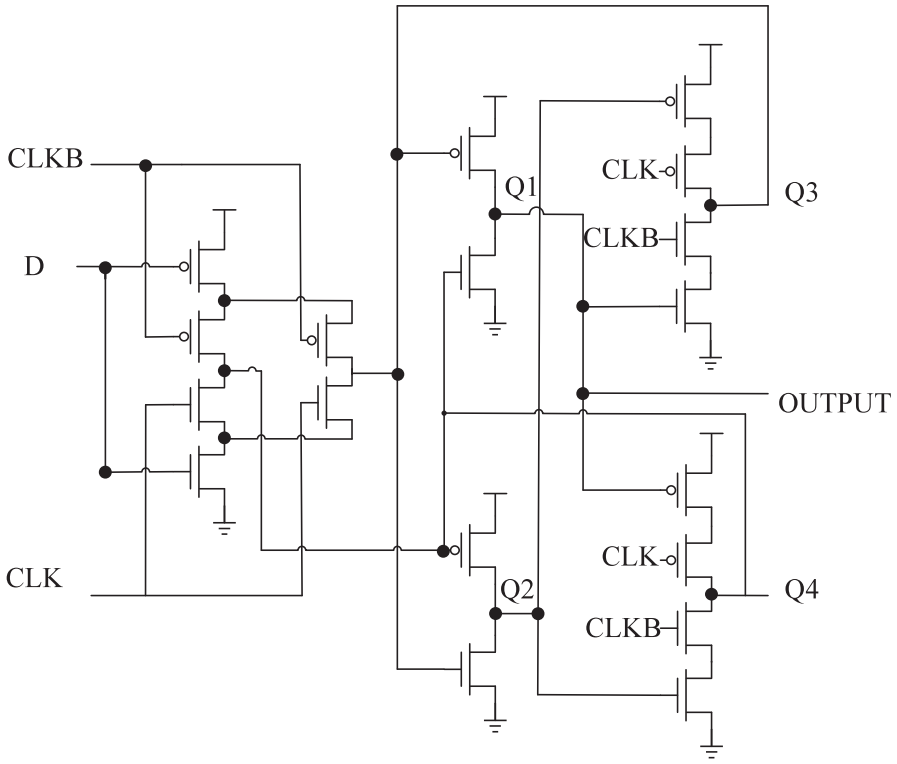

Fig. 2. DICE latch [11]

However, DICE latch [12] still needs to pay heavy hardware overhead to achieve superior SEU-tolerance since its transistor size should be increased to meet the demand for soft error resistance.

Fig. 3 shows the schematic of FERST latch, which consists of two parallel latches and three C-elements [14], with the help of which SEU can be masked. Although FERST latch has superior SEU tolerance for all internal nodes, its output node still has potential to be affected by SEU if the particle energy is high enough.

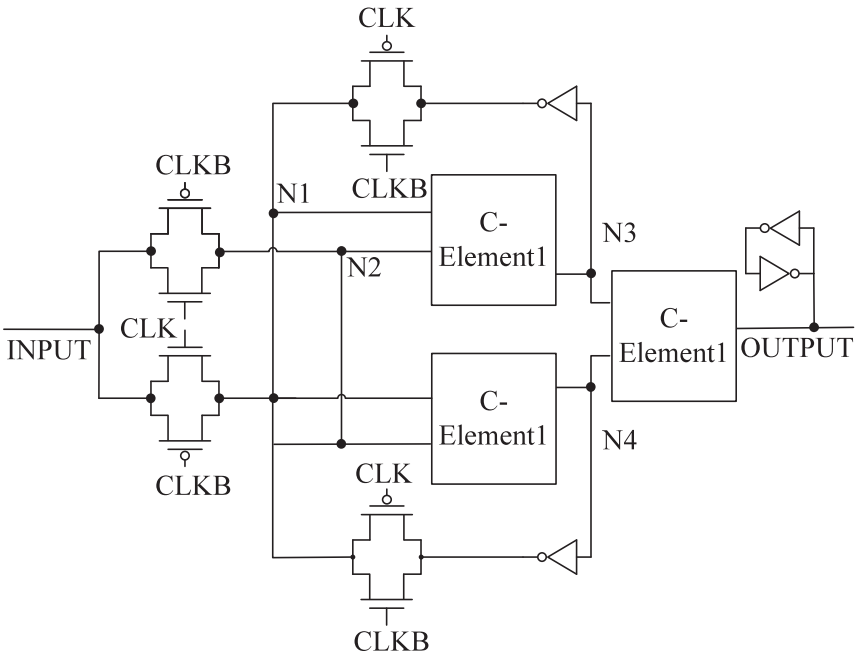

Fig. 3. FERST latch [13]

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Moreover, its drawbacks include large power-delay-product (PDP) and heavy hardware overhead.

Generally speaking, the performance and hardware overhead are still need to be improved for aforementioned hardened latch designs. In this paper we propose a hardened latch design that can achieve the same SEU-tolerance as FERST latch and DICE latch with lower PDP. Simulation experiments under 180 nm and 40 nm CMOS process are carried out for performance evaluation, which will be discussed in next sections.

3 Proposed hardened latch

As shown in Fig. 4, the proposed latch utilizes two cross-coupled structures [15] that cross couple to form negative feedback paths. Redundant transistors (MP1, MP2, MN1, MN2) are controlled by storage nodes. When the latch works at transparent mode, feedback paths are cut off to speed up write operation. When the latch works at latching mode, the flip state caused by SEU can be isolated or recovered through the negative feedback.

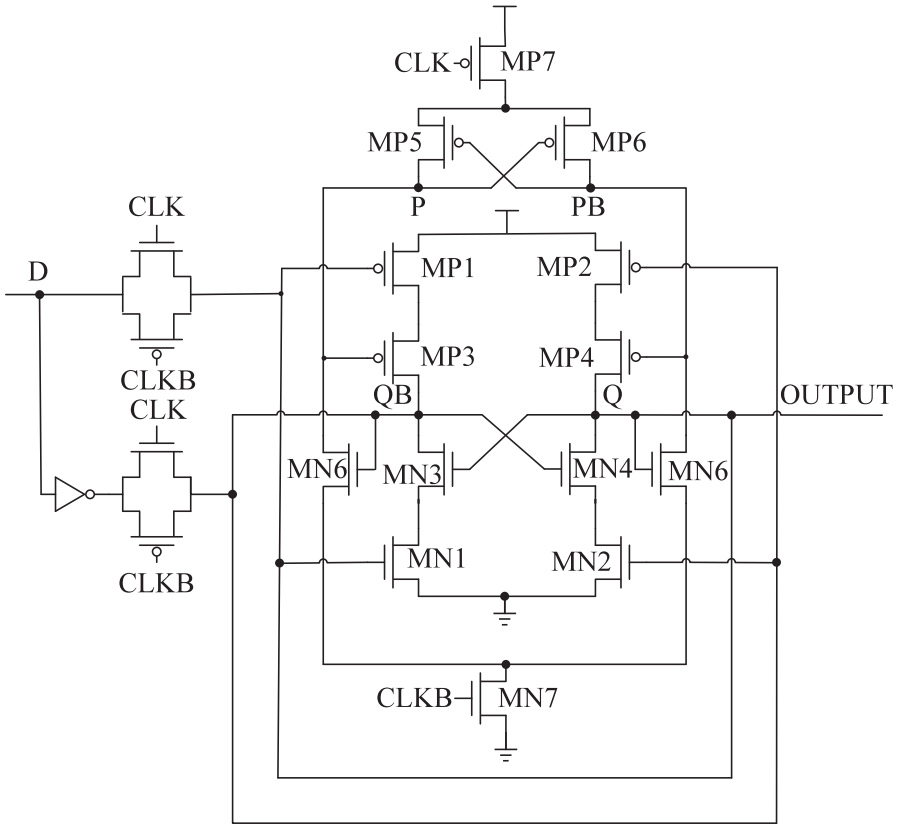

Fig. 4. Proposed latch

The detailed operation of proposed latch is illustrated as below. When CLK = 1 and CLKB = 0, latch goes into transparent mode. Transmission gates are turn on and the same and inverse phase of input D are respectively transferred to node Q and QB. As mentioned above, the negative feedback has an opposite effect on storage Q and QB during write operation. Four transistors (MN1, MN2, MP1, and MP2) are added to cut off the negative feedback. Assume that input D = "1", Q is

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supposed to be set to "1" and QB is to "0". If the precious logic state of P is "0", MP3 is on that tends to charge node QB and hinders its pull-down processing. However, MP1 is added and turned off to stop the pull-up procedure of node QB and MN1 is turn on to speed up the pull-down procedure of node QB. Moreover, as to save power, MN7 and MP7 controlled by clock signal are added to cut off the current flowing paths of node P and PB at transparent mode. The logic values of node P and PB will be updated at the beginning of latching mode.

When CLK = "0" and CLKB = "1", latch turns into latching mode. After the logic values of node P and PB have updated, the negative feedback design for SEU-tolerance is constructed. The steady logic states of nodes Q, QB, P, PB are "1" "0" "1" "0" or "0" "1" "0" "1". For different types of flips that occur at four sensitive nodes, their SEU-tolerant mechanism is illustrated in detail.

Case1–A SEU from logic "1" to logic "0" occurs at node Q or QB. Nodes Q and QB are both connected to the gate of NMOS transistors (MN3, MN6, MN4, and MN5), so this flip can be isolated and stopped from affecting other nodes. Then the flip will be recovered by the negative feedback. MP1 and MP2 are ignored because of the isolation of MP3 and MP4, which are under control of node P and PB.

Case2–A SEU from logic "0" to logic "1" occurs at node P or PB. In the same way as Case 1, nodes P and PB are only connected to the gate of PMOS transistors (MP3, MP6, MP4, MP5), so this flip can be isolated and the flip can be recovered. For Case1 and Case2, the critical charge can be considered as ∞.

Case3–A SEU from logic "1" to logic "0" occurs at node P or PB. Assume that node P flips from logic "1" to "0". Thus node P and PB are both at logic "0" in the same time and MP5 and MP6 become on. Meanwhile, Q = "1" and QB = "0", MN5 is off and MN6 is on. Nodes P and PB compete to be logic "1" while the pull-down path of P is cut off and that of PB is turn on. As a result, node P prevails and recovers to its normal state "1". The critical charge of this case is more than 100 fC through simulation.

Case4–A SEU from logic "0" to logic "1" occurs at node Q or QB. Assume that node Q flips from logic "0" to "1". In the same way as Case 3, with the help of node P, MP3 is on and constantly charge node QB, so it has a higher ability to keep logic "1". On the contrary, node Q recovers to its normal state "0". The critical charge of this case is more than 10 fC through simulation.

4 Comparison of simulation results and performance

Simulations are carried out using Cadence Spectre on a 180 nm and 40 nm CMOS process with 1.1 V supply voltage at 100 MHz frequency. No capacitive load is added acquiescently. For fair comparison, transistors in different circuits are all at minimum size. The impact of injected particles can be described by a double exponential current pulse which is shown as follows [16]:

$$i(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}), \quad (1)$$

where Q is the amount of charge deposited as a result of the ion strike, τ_α is the collection time constant for the junction and τ_β is the ion track establishment

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constant. It has been extensively reported that particle strikes typically lead to current pulses with various durations [17] and Eq. (1) can be expressed as:

$$Q = I_0 \int_0^{\infty} (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})\, dt = I_0 \times (\tau_\alpha - \tau_\beta) \tag{2}$$

Here, we set $\tau_\alpha = 45$ ps and $\tau_\beta = 145$ ps. The parameter we select to evaluate the SEU-tolerance is the critical charge, defined as the minimum charge that makes the state flip [18]. The critical charge required for a soft-error of each node can be figured out by iteratively increasing the injected charge by a small amount.

Fig. 5 shows a recovery process of flip from logic "1" to "0" occur at node P. The injected charge is 100 fC and the logic value of node P recovers to its normal state within 1.2 ns even through the voltage fluctuation at node P is over 1.047 V. As illustrated in Fig. 6, node Q is able to recover to its normal state within 0.3 ns when 10 fC charge is injected and flip from "0" to "1" occurs.

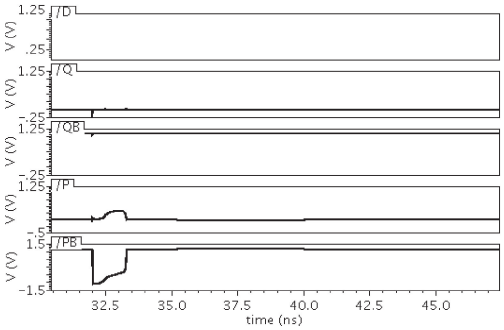

Fig. 5. Recovery procedure of flip from "1" to "0" occurs at node PB

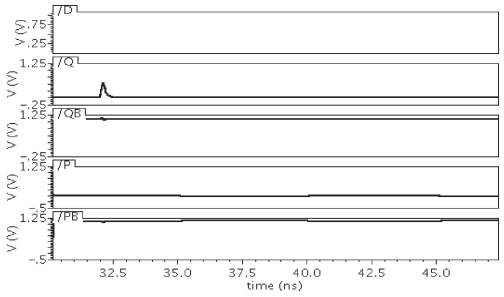

Fig. 6. Recovery procedure of flip from "0" to "1" occurs at node Q

For conventional latch, its critical charge is only 0.2 fC. The critical charge of our hardened is 10 fC, 50 times of that of conventional latch. FERST latch maintains a critical charge of 10 fC and DICE latch is 20 fC. We compare the performance of proposed latch with that of other hardened latches. The comparison results for transistor count, critical charge, power, delay, and power-delay-product are listed in Table I and Table II. The input voltage remains stable and the hyperbolic function of the current source is connected to the sensitive node, and the flip state achieves. The PDP [19] penalty can be calculated as Eq. (3). Results show that the proposed latch has a relatively small transistor count and a much bigger critical charge than other three latches, while it consumes the minimum delay and modest power dissipation. So it has lower PDP than other two hardened latches.

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Table I. Performance comparison in 180 nm process

Latches	Conventional Latch	FERST Latch	DICE Latch	Proposed Latch
Transistors Count	10	28	18	20
Critical Charge (fC)	5	40	100	>1000
Dynamic Power (uW)	0.185	3.415	1.318	1.345
Static Power (nW)	200.1	295.5	455.2	262.7
Delay CLK-Q (ps)	126.4	359.9	146.2	38.8
PDP (fs∗J)	0.0233	1.229	0.193	0.0525
PDP Penalty	0	51.75	7.28	1.253

Table II. Performance comparison in 40 nm process

Latches	Conventional Latch	FERST Latch	DICE Latch	Proposed Latch
Transistors Count	10	28	18	20
Critical Charge (fC)	0.2	10	20	10
Dynamic Power (nW)	45.68	346.72	300.86	157.3
Static Power (nW)	189.2	229.7	783.3	232.8
Delay CLK-Q (ps)	97.9	135.4	76.9	23.3
PDP (fs∗J)	0.0045	0.0469	0.0231	0.0035
PDP Penalty	0	9.42	4.13	0.178

$$\text{PDP\_}penalty = \frac{PDP(Hardened\_Latch) - PDP(Conventional\_Latch)}{PDP(Conventional\_Latch)} \quad (3)$$

When feature size decreases to 40 nm, the advantage of critical charge of proposed latch disappears though it is still at the same order of magnitude as FERST latch and DICE latch. It is because that all transistors in the simulation are set at minimum sizes and the critical charge can greatly magnify if some of the transistor sizes are increased. However, the proposed latch still maintains outstanding performance. Measured by PDP, FERST latch is 13 times of the proposed latch and DICE latch is 6 times. Therefore, the new hardened latch design achieves a lower PDP with superior SEU-tolerance when compared with similar latch designs.

For a detailed comparison, the relative cost in terms of transistors count, power, delay and PDP of the precious latches over the proposed latch are calculated in Fig. 7. As shown in Fig. 7, the proposed latch on average achieves 76.2% reduction in terms of delay and 66.5% reduction in terms of PDP.

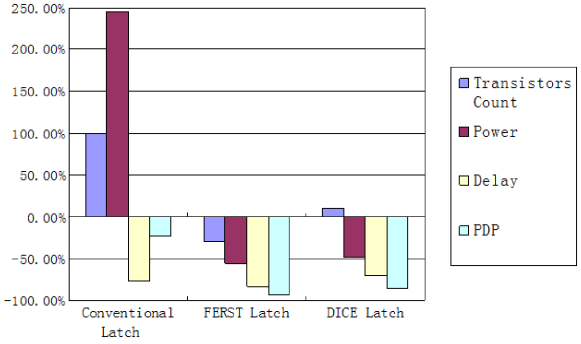

Fig. 7. Relative performance improvement of precious latches against proposed latch in 40 nm process

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5 Conclusion

In this paper, we propose a robust SEU-tolerance latch design with low PDP. It utilizes the SEU-tolerant mechanism of cross-coupled structures and flip-isolation of mechanism to realize high SEU immunity. Simulation results show the proposed latch has superior SEU-tolerance as some similar latch designs, while consumes less delay and power consumption. The proposed latch performs with 7.5% lower PDP than FERST latch and 15.2% than DICE latch. It can be convinced that the proposed SEU-tolerant latch design has large potential to be used in high-speed low-power hardened digital circuits.

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