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Fully-integrated linear CMOS power amplifier with proportional series combining transformer for S-Band applications

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Abstract: A novel proportional series combining transformer using for power amplifier (PA) is presented. Compared with balanced series combining structures, the high efficiency range is extended by sophisticated power adjusting and impedance tuning. As a proof-of-concept, a 2.5 V dual-channel PA with the proposed transformer was implemented in standard 0.18-µm CMOS process. The fabricated PA achieved a saturated output power (P_{sat}) of 28 dBm and a maximum linear output power ($P_{1\text{-}dB}$) of 26.8 dBm with the power added efficiency (PAE) of 33.5% and 31%, respectively. With power mode control, the high efficiency range exceeded 8.2 dB. The PA satisfied EVM requirements of LTE 2.3 GHz 20 MHz/64-QAM signal and WLAN 802.11g signal, respectively.

Keywords: power amplifier, transformer, power combiner, proportional, power mode control

Classification: Integrated circuits

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1 Introduction

Radio frequency (RF) link demands power amplifiers (PAs) that are lower bill of materials, higher average efficiency, better linearity and a smaller form factor. It is worth noting that CMOS PAs, as low cost solution, still are good candidates for portable wireless applications [1, 2, 3]. It is certain that CMOS PAs need adopt kinds of techniques to overcome its high parasitic loss and low breakdown voltage [4]. Considering that PAs operate on power back-off region most of the time, the high-efficiency range is necessary to be extended, thus the high average efficiency and long battery life can be acquired. Various technologies have been proposed on average efficiency improvement, such as envelope tracking techniques, Doherty power amplification, balanced transformer power combining and so on [5, 6, 7, 8].

However, the limited dynamic range and systematic complexity are always challenges for envelop tracking techniques [5]. Doherty power amplification exhibits high efficiency over a wide range of output power, but the $\lambda/4$ transmission lines are usually difficult to be integrated in a single die [9]. Transformer power combining technique can dynamically modulate the load by channel switching, hence it is able to keep the high efficiency at back-off region. There have been efforts to realize transformer power combining PA in CMOS process, with the power combiners adopting balanced structures [7, 8, 10, 11]. Nevertheless, the high-efficiency range of a balanced structure is not fully developed due to its even-distributed power channels and rough power adjustment.

In this paper, a novel proportional series combining transformer (P-SCT) topology is proposed, the high-efficiency range is further extended by sophisticated power adjusting and impedance tuning. As a proof-of-concept, a S-Band fully-

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integrated dual-channel power amplifier based on P-SCT will be implemented in standard 0.18-μm CMOS process without external components.

This paper is organized as follows: In section 2, the P-SCT structure is analyzed and compared with conventional balanced combining structure. The detailed PA circuit design, measured results and conclusion are given in section 3, 4 and 5, respectively.

2 Proportional series combining transformer design

The P-SCT structure is shown in Fig. 1. It is a combination of multi-channel (N ≥ 2) proportional transformer units.

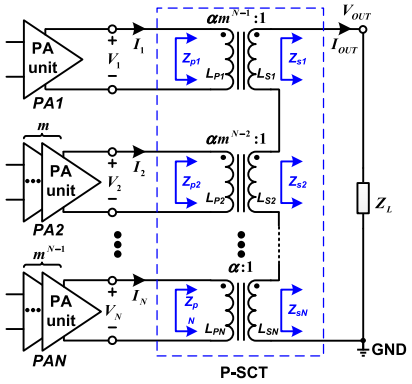

Fig. 1. N-channel proportional series combining transformer (P-SCT) structure.

The self-inductances of the primary and secondary windings of each transformer unit correspond to the geometric sequences, given as (1) and (2),

$$\sqrt{\frac{L_{P1}}{L_{S1}}} : \sqrt{\frac{L_{P2}}{L_{S2}}} : \cdots : \sqrt{\frac{L_{PN}}{L_{SN}}} = \alpha m^{N-1} : \alpha m^{N-2} : \cdots : \alpha \tag{1}$$

$$L_{S1} : L_{S2} : \cdots : L_{SN} = 1 : m : \cdots : m^{N-1} \tag{2}$$

where m, or $1/m$ ($m > 1$) is the common ratio of above geometric sequences, and α ($\alpha > 1$) is the adjustable coefficient for turn ratios, used for adjusting the output power level. The magnetic coupling coefficient k of each transformer unit is regard as ideal for simplicity, thus all mutual inductances of these units are equal, which can be derived as (3),

$$M = \frac{m-1}{m^N - 1} \cdot \alpha m^{N-1} L \tag{3}$$

the corresponding Z-Matrix of proposed P-SCT structure can be expressed as (4).

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \\ V_{out} \end{bmatrix} = \begin{bmatrix} j\omega M\alpha m^{N-1} & 0 & \cdots & 0 & -j\omega M \\ 0 & j\omega M\alpha m^{N-2} & \cdots & 0 & -j\omega M \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & j\omega M\alpha & -j\omega M \\ j\omega M & j\omega M & \cdots & j\omega M & -j\omega L \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \\ I_{out} \end{bmatrix} \tag{4}$$

According to the Z-Matrix, the input and output impedance of each transformer unit are calculated as (5) and (6).

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$$\begin{cases} Z_{p1} = \omega M\alpha(1+j)m^{N-1} \\ Z_{p2} = \omega M\alpha(1+j)m^{N-2} \\ \vdots \\ Z_{pN} = \omega M\alpha(1+j) \end{cases} \tag{5}$$

$$\begin{cases} Z_{s1} = \omega M\alpha^{-1}(1-j)m^{1-N} \\ Z_{s2} = \omega M\alpha^{-1}(1-j)m^{2-N} \\ \vdots \\ Z_{sN} = \omega M\alpha^{-1}(1-j) \end{cases} \tag{6}$$

As a result, the input impedance of each transformer unit varies by the same proportion as the power stage output impedance, and the load impedance of each transformer unit is in accordance with the secondary self inductances, respectively.

$$Z_{p1} : Z_{p2} : \cdots : Z_{pN} = m^{N-1} : m^{N-2} : \cdots : 1 \tag{7}$$

$$Z_{s1} : Z_{s2} : \cdots : Z_{sN} = 1 : m : \cdots : m^{N-1} \tag{8}$$

According to [12], the passive efficiency of a transformer can be maximized when the load impedance meets equation (9) approximately.

$$Z_{sN} = \frac{\omega L_{sN}}{\sqrt{\frac{1}{Q_s^2} + \frac{Q_p}{Q_s} \cdot k^2}} - j \cdot \omega L_{sN} \approx \omega L_{sN} - j\omega L_{sN} \tag{9}$$

Based on (7)~(9), the proposed P-SCT structure exhibits a multi-channel proportional input and load impedance, therefore, all power units and transformer units can achieve η_{max} at the same time.

The maximum output power can be calculated as (10) when all power channels are switched on and reach the maximum efficiency. Similarly, the minimum output power can be calculated as (11) when only the first power channel is switched on and reaches the maximum efficiency.

$$P_{OUT,MAX} = \frac{V_{DD}^2}{2Z_L} \cdot \frac{(m^N-1)^2}{\alpha^2 m^{2N-2}(m-1)^2} \tag{10}$$

$$P_{OUT,MIN} = P_{OUT,MAX} \cdot \frac{(m-1)^2}{(m^N-1)^2} \tag{11}$$

The peak output power range, which means the ratio of the high to low saturated output power is related to channel number (N) and proportion (m) according to (10) and (11). As a comparison, the balanced combining structure is able to provide a power ratio of N^2 [7]. Obviously, the high efficiency range of proposed P-SCT structure is extended compared to conventional balanced structure. Moreover, the proposed N-channel PA can be designed to operate in $2^N - 1$ power modes, more than the balanced structure PA with only with N power modes. Fig. 2 shows the efficiency comparison of dual-channel PAs with the balanced and proportional ideal power combining transformers.

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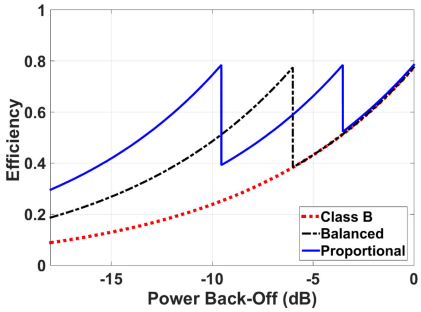
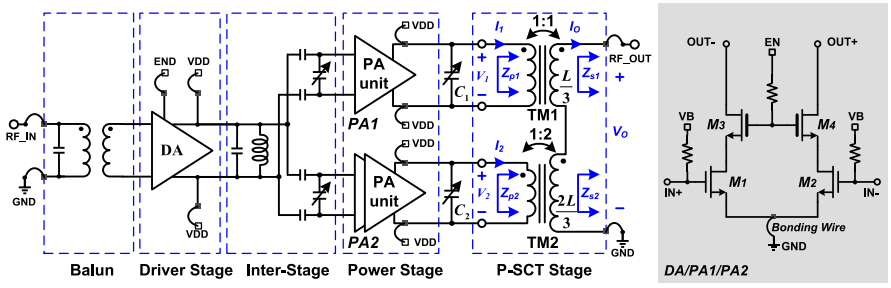


Fig. 2. Back-off efficiency of proposed dual-channel proportional structure with m = 2, N = 2, in comparison with the balanced structure and conventional class-B PA.

3 Implementation of dual-channel PA with P-SCT structure

3.1 Schematic of dual-channel PA with P-SCT

To validate the theoretical analysis, a dual-channel dual-stage CMOS power amplifier with the proposed P-SCT structure ($N = 2$, $m = 2$ and $\alpha = 0.5$) is designed, depicted in Fig. 3(a). Two parallel power channels are combined by the P-SCT stage at the output. The driver and power stage are pseudo differential amplifiers with cascode topology, shown in Fig. 3(b). In addition, the common gate stage of all amplifiers are thick-oxide transistors used for further distributing the voltage stress. The VDD bonding wires which serve for power feeding for driver and power stage are included in the matching networks. Because of the bonding wire effects in the matching networks, optimal load trajectory were a little shifted from original trajectory for both driver and power stage. Meanwhile, the efficiency performance is little improved due to low parasitic series impedance of bonding wires. Device sizes of each transistor for driver and power stage are summarized in Table I. The P-SCT stage is a combination of a 1:1 transformer (TM1) and a 1:2 transformer (TM2).



(a) (b)

Fig. 3. (a) Simplified dual-channel PA schematic with P-SCT (b) the pseudo differential cascode configuration

Table I. Summary of device sizes

	Common Source (M_1, M_2)		Common Gate (M_3, M_4)	
	W/L (μm/μm)	NO. of fingers*	W/L (μm/μm)	NO. of fingers*
DA	840/0.18	168	900/0.34	180
PA1	1680/0.18	336	2160/0.34	432
PA2	3360/0.18	672	4320/0.34	864

*Unit finger-width is 5 μm

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The single-ended external signal is turned to differential internal signal by an on-chip passive balun. All input, output and inter matching network are realized with passive inductors and capacitors without external components.

3.2 P-SCT based output passive network design

A dual-channel P-SCT based output passive network is proposed, and the 3D EM structure is depicted in Fig. 4.

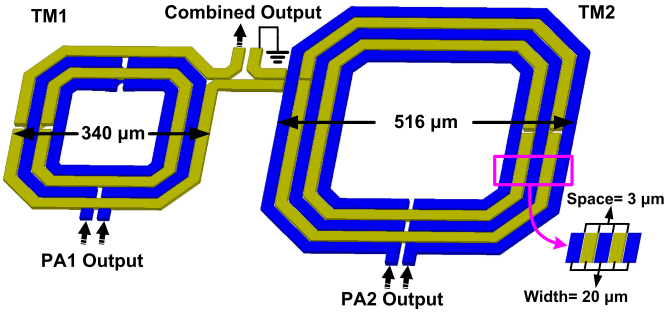

Fig. 4. Implementation of proposed dual-channel P-SCT

The turn ratio of a transformer can be defined as follow [13],

$$n = \sqrt{\frac{L_s}{L_p}} \tag{12}$$

where L_p and L_s are the self-inductances of the primary and secondary winding, respectively. The planar transformer units are constructed from inter-wound metal conductors. The primary winding of TM2 adopts three metal lines in parallel, therefore a better magnetic coupling coefficient can be acquired. In order to acquire accurate turn ratio and inductances, all transformers were modeled and analyzed in Ansoft HFSS software. Simulated results are listed in Table II.

Table II. Performance of TM1 and TM2 at 2.4 GHz

Transformers	Primary Self-Inductance	Secondary Self-Inductance	Magnetic Coupling Coefficient	Turn Ratio
TM1	1.29 nH	1.52 nH	0.75	1 : 1.09
TM2	0.67 nH	2.95 nH	0.81	1 : 2.13

The equivalent circuit model of proposed dual-channel P-SCT are presented in Fig. 5. Note that the proportion m and the adjustable coefficient of turn ratio α are set to 2 and 0.5, respectively. The magnetic coupling coefficient of both transformer units are set to be equal ($k_{TM1} = k_{TM2} = k = 0.8$) for simplification.

The transformer efficiency is the ratio of power dissipated in load resistance R_L and the total power dissipated in r_{p1}, r_{p2}, r_s and R_L, shown in (12).

$$\eta = \frac{R_L}{R_L + r_s + \dfrac{[(\omega L_s - 1/\omega C_L)^2 + (r_s + R_L)^2](4{r_{p2}}^2 + \omega^2 {L_p}^2)}{n^2 k^2 \omega^2 {L_p}^2[(2r_{p1} + 2r_{p2})^2 + 9\omega^2 {L_p}^2]}\left(r_{p1} + \dfrac{4{r_{p1}}^2 + 4\omega^2 {L_p}^2}{4{r_{p2}}^2 + \omega^2 {L_p}^2} r_{p2}\right)} \tag{13}$$

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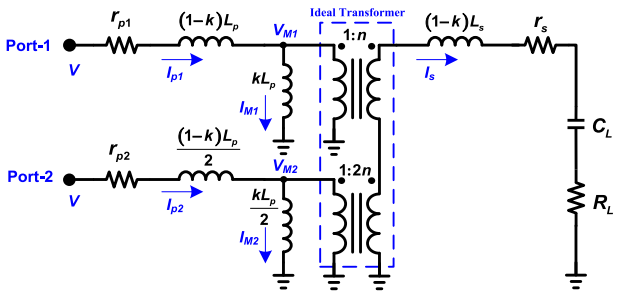

Fig. 5. Equivalent circuit model of proposed dual-channel P-SCT

A maximum efficiency can be acquired when the series capacitor C_L resonate L_s at the frequency of interest. The load termination is set to 50 Ω, which is pulled to 45–60j Ω by bond wires and on-chip shunt capacitor at the frequency of 2.4 GHz. The equivalent series devices C_L and R_L are assigned to 1.1 pF and 45 Ω, respectively. Without considering input and output terminal reflection, the simulated power transform efficiency of the proposed dual-channel P-SCT against frequency is plotted in Fig. 6.

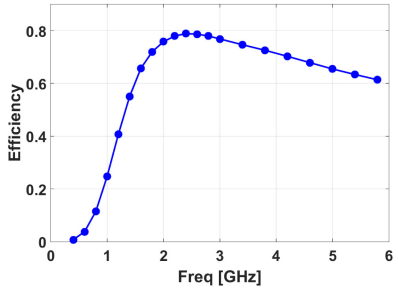

Fig. 6. Simulated transformer efficiency versus frequency

3.3 Power mode control

The power channels can be turn on and off independently by gate bias controlling. Through power channel switching, the PA can be set to operate in three power modes: $I_1 \neq 0$, $I_2 = 0$ in low power mode (LP), $I_1 = 0$, $I_2 \neq 0$ in medium power mode (MP) and $I_1 \neq 0$, $I_2 \neq 0$ in high power mode (HP), shown in Fig. 7.

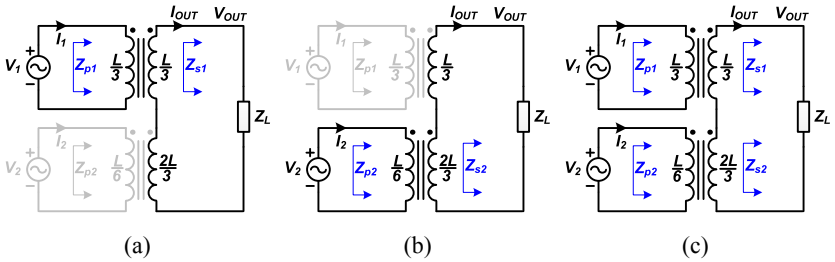

Fig. 7. (a) Low power, (b) medium power and (c) high power mode

According to equation (3)~(6), the input and load impedance of each transformer unit are calculated in different power modes and summarized in Table III.

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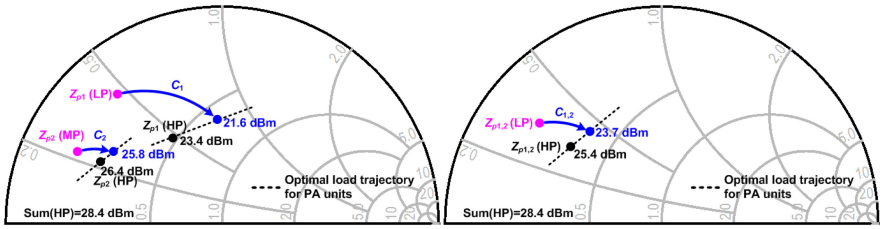
Table III. Summary of port impedance in different power modes

	HP($I_1 \neq 0, I_2 \neq 0$)	MP($I_1 = 0, I_2 \neq 0$)	LP($I_1 \neq 0, I_2 = 0$)
Z_{p1}	$\omega L(1+j)/3$	$+\infty$	$\omega L(1/3+j)/3$
Z_{p2}	$\omega L(1+j)/6$	$\omega L(2/3+j)/6$	$+\infty$
Z_{s1}	$\omega L(1-j)/3$	—	$\omega L(1-j/3)$
Z_{s2}	$2\omega L(1-j)/3$	$\omega L(1-j2/3)$	—

In order to maximize the efficiency of the entire PA in high power mode, the input impedance of TM1 and TM2 should be realized conjugate matching with the output impedance of PA1 and PA2 at the operation frequency, respectively. The input impedances vary with different power modes, to be specific, the real part of Z_{p1} deceases by 2/3 in low power mode. and the real part of Z_{p2} deceases by 1/3 in medium power mode. Therefore, when operating at power back-off, the dislocated input impedance is needed to be pulled back to the optimal load trajectory of each PA unit by using tunable capacitors. The trajectories of impedance tuning for the proposed proportional structure and the conventional balanced structure are shown in Fig. 8.



(a) (b)

Fig. 8. Conjugate matching realization between power stage and transformer units for (a) proposed P-SCT structure and (b) conventional balanced structure

Z_{p1}(LP) is pulled to a proper impedance value of $28 + 27\text{j}\,\Omega$, with the shunt capacitor of 1.8 pF. Similarly, Z_{p2}(MP) is pulled to $14 + 13.5\text{j}\,\Omega$, with the shunt capacitor of 2 pF. Simulation results show that the output power of PA1 is 21.6 dBm in LP, the output power of PA2 is 25.8 dBm in MP, and the total output power of 28.4 dBm in HP. The high to low power ratio is 6.8 dB, which is further extended than the conventional balanced structure with a power ratio of 4.7 dB.

4 Measurement results

The fully-integrated PA was implemented in 0.18-µm CMOS process, shown in Fig. 9. Total die area is $2.3 * 1.3\,\text{mm}^2$. In order to realize a small size and low parasitic effects, the chip is bonded to Quad Flat No-lead (QFN) package with 50 Ω input and output terminations. With $V_{DD} = 2.5$ V, the common source gate bias setting for driver stage is a combination of 0.5 V and 0.7 V in order to get good linearity. The common source gate bias of PA1 and PA2 are both set to 0.55 V for class AB linear operation.

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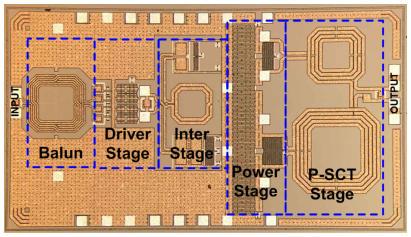
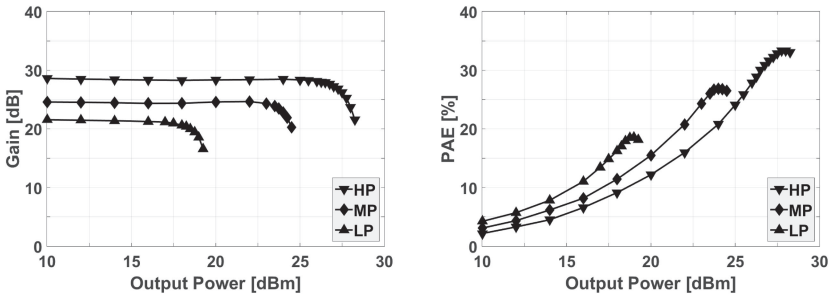


Fig. 9. Die photograph of the PA

Measurement results of power gain and PAE against output power are shown in Fig. 10(a) and (b), respectively. The maximum linear output power are 18.6 dBm with PAE of 16.8% in LP, 23.5 dBm with PAE of 25% in MP, 26.8 dBm with PAE of 31% in HP, respectively. The saturated output power is 28 dBm with PAE of 33.5%. On account of the difference of P-SCT energy delivery efficiency in HP and LP, the power ratio of HP to LP is enlarged to 8.2 dB.



(a) (b)

Fig. 10. (a) Power gain and (b) PAE against output power

To evaluate the EVM performance for different modulations, LTE 2.3 GHz 20 MHz Band-width 64-QAM signal and 802.11g WLAN 54 Mbps 64-QAM OFDM signals at 2.4 GHz are applied. The EVM limit for LTE and WLAN signals are both −25 dB. The measured EVM results given in Fig. 11, demonstrate that the PA acquires an EVM value of −27 dB with PAE of 21% at the maximum linear output power which is 22 dBm for WLAN signal, and a EVM value of −29.5 dB with PAE of 21.4% at the maximum linear output power which is 24 dBm for LTE signal, respectively. The implemented power amplifier satisfied the EVM mask for these two modulated signals under the maximum linear output power requirements.

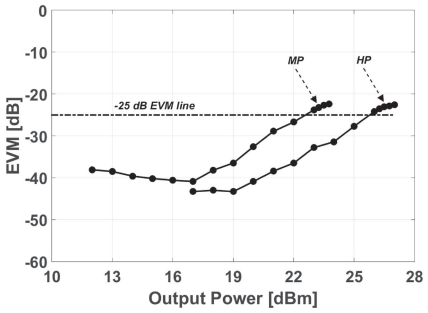


Fig. 11. Measured EVM for 802.11g WLAN 54 Mbps 64-QAM OFDM signal and LTE 2.3 GHz 20 MHz/64-QAM signal

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Table IV. Comparisons with previously reported CMOS PAs

Ref.	Process [nm]	Supply [V]	Freq. [GHz]	$P_{1\text{-dB}}$ [dBm]	PAE@ $P_{1\text{-dB}}$ and Back-offs from $P_{1\text{-dB}}$ [%]	Power Combiners
[2]	180	3.3	2.5	20/22.3/26[†]	13/15/22.5[†]	Balanced PCT[△]
[3]	180	3.3	2.4	31.5	26.5/10.5 (−8 dB Back-off)	Balanced PSCT[▽]
[8]	180	3.3	2.4	27	33[‡]/10[‡] (−6 dB Back-off)	Balanced PCT[△]
[10]	90	3.3	2.4	27.7	25/8 (−8 dB Back-off)	Balanced SCT
[11]	65	3.3[∂]	2.5	23.7/26.7/28.2[†⋄]	13.1/18/21[†⋄]	Balanced SCT
This work	180	2.5	2.3/2.4	18.6/23.5/26.8[†]	16.8/25/31[†]	Proportional SCT

[†]With power mode control, [‡]Peak drain efficiency, [⋄]Saturated output power, [∂]Envelope modulated supply, [△]Parallel combining transformer, [▽]Parallel series combining transformer

The performance of the designed PA is summarized and compared to previously reported power combining CMOS PAs with the balanced structure in Table IV. Comparing with references with ([2], [11]) or without ([3], [8], [10]) power mode control, the PAE at back-offs from $P_{1\text{-dB}}$ is distinctly improved. Reference [8] exhibits high peak drain efficiency, but the linear efficiency was not so good and the drain efficiency decreased sharply at back-off region. Generally, the proposed PA provides a favorable performance on high efficiency range of output power.

5 Conclusion

A fully-integrated CMOS PA with the proposed P-SCT structure for S-Band applications is achieved. The back-off efficiency is distinctly improved by using a proportional power combiner. The maximum linear output power ($P_{1\text{-dB}}$ @HP) is 26.8 dBm with PAE of 31%. When the PA operates in low power mode, at 8.2 dB power back-off ($P_{1\text{-dB}}$ @LP), the PAE is 16.8%. Compared with traditional balanced structure, the linear high efficiency power range is expanded. Moreover, this sophisticated power adjusting method can be applied to multi-channel and any proportion power amplifier design.

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