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An equivalent lumped circuit model for on-chip helical transformers

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Abstract: This paper presents a compact equivalent lumped circuit model for on-chip helical transformers. From fundamental model, a simple coupled *RL* loop is added to account for the skin and proximity effect, and a series *RLC* branch is added to account for the parasitic coupling effects between inductors. Several helical transformers with various design configurations were fabricated using a standard 0.18 µm 1P6M CMOS process. It's demonstrated that the proposed model shows good accuracy over two times self-resonance frequency, which is essential for the design of high-speed and radio-frequency circuit.

Keywords: on-chip helical transformer, equivalent lumped circuit model, standard CMOS process

Classification: Electron devices, circuits and modules

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1 Introduction

On-chip transformers, or coupled inductors, are often used for the design of high-speed and radio-frequency circuit blocks, such as voltage-controlled oscillator, high-bandwidth amplifier, impedance matching, and so forth. Usually, the planar inductors are employed due to their relatively higher quality factor. However, the multilayer inductors, or stacked inductors, show higher inductance density, which means they occupy less area for the same inductance. As the integrated circuits technologies advance, more metal layers are available for the design of multilayer inductors, and make it possible that the devices can be more compact. As one of the most important work, the modeling of planner transformers drew much research effort [1, 2]. However, because of their complexity and diversity, the modeling of multilayer transformers is not that easy. In [3], a lumped model was proposed for stacked transformer, which may not applicable to the other multilayer transformers. In [4], a distributed model was proposed for symmetric multilayer transformers. Though physical and universal to some extent, it's not convenient for practical design due to too many parameters needed.

Helical inductor, as the simplest multilayer inductor, has only one turn on each layer, and then the number of turns equals to the number of layer used. A helical transformer consists of two coupled helical inductors. Fig. 1a shows the 3D-view of helical transformer. For multilayer inductors, because the space between metal layers is small, and the turn width is always large, the parasitic capacitance seems significant. However, according to the analysis in [5], it can be verified that the equivalent capacitance across the two terminals of helical inductor is actually small, and if more layers are stacked, the final equivalent capacitance gets even smaller. This is why the helical inductor possesses high self-resonance frequency f_{SR} along with high inductance density. The helical transformer will also have this benefit. In this paper, we discuss the modeling of helical transformer. A compact equivalent lumped circuit model for helical transformer is given, which shows good agreement with the measurement results.

2 Device structure and circuit model

We designed the helical transformers in a standard 0.18 um CMOS process, which provides 6 metal layers. As shown in Fig. 1a, the inner and outer inductors are placed in concentric style. The inner inductor uses six metal layers, from M1 to M6, while the outer inductor uses four metal layers, from M2 to M5, to facilitate the routing of lead wires for the inner inductor.

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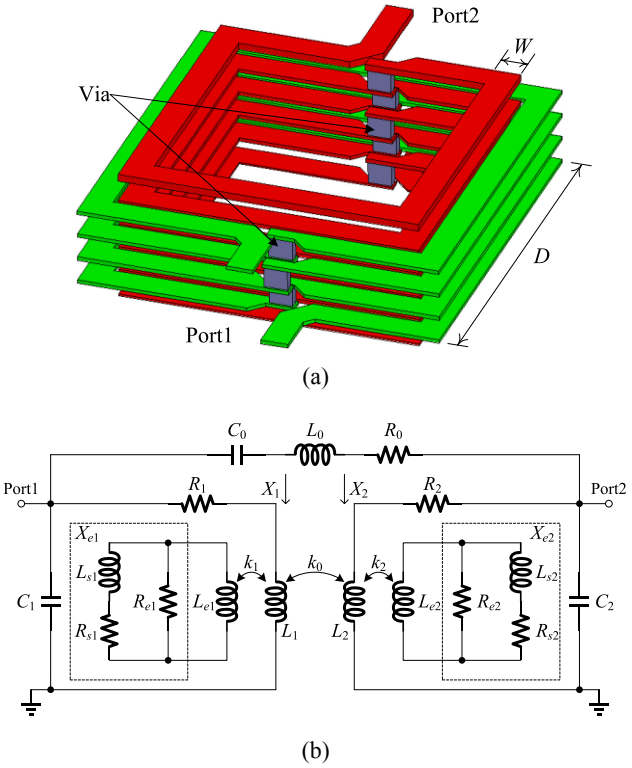

Fig. 1. (a) 3-D view (D: outer diameter, W: turn width) and (b) proposed equivalent lumped circuit model of helical transformer. The lower terminals of both two inductors are grounded.

Fig. 1b shows the proposed equivalent lumped circuit model for helical transformer. L_1, R_1, C_1, L_2, R_2, C_2 and k_0 constitute the fundamental model of the transformer [6]. L_1, R_1 can be viewed as dc inductance and dc resistance of the outer inductor, respectively. C_1 represents the equivalent parasitic capacitance across the two terminals of the inductor, as defined in [5]. L_2, R_2 and C_2 represent the corresponding parameters of the inner inductor. k_0 is the coupling coefficient between the outer and the inner inductors. In reality, the inductance and the resistance are frequency dependent due to the skin and the proximity effects. Therefore, a circuit model with the capability to mimic the frequency behavior of the actual inductor is required. In previous papers, a *RL* ladder structure is proved to be an effective way to capture the frequency behavior of inductor, and also transformer [2, 3]. However, as for a *RL* ladder, there is no explicit component that can be viewed as dc inductance, and each inductance component is larger than dc inductance. Thus, when considering the coupling coefficient k_0, one will very likely obtain a deviated value, which is usually misleading. To make it more physical and meaningful, we employ a coupled *RL* loop structure as shown in the figure. The final extraction results will reveal that the extracted k_0 approach the theoretical values.

According to [7], the eddy current in metal path contributes an important part of the aforementioned frequency dependence. As shown in [7], the electro-magnetic field B will penetrate through the metal path and excite eddy current loop, which is always crowed along the path edges. Hence, a *RL* loop, including the loop resistance and inductance R_{e1} and L_{e1}, models this loop, and k_1 models the

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interaction between the main inductance and the loop. Actually, an additional branch, including R_{s1} and L_{s1}, is also necessary to capture the frequency dependence of the loop resistance. L_{e2}, R_{e2}, L_{s2} and R_{s2} represent the corresponding parameters of the inner inductor. A more complicated high-order RL loop was discussed in [2]. However, it's found that the RL loop here is accurate enough for the modeling of helical transformer.

Another important part is the parasitic coupling between the inner and the outer inductors. In most previous circuit models, only the parasitic capacitance had been taken into consideration [2, 3]. However, due to the distributed nature of the coupling effect, the capacitor-only scheme cannot ensure model accuracy at higher frequencies. In [8], an improved scheme was proposed to account for this distributive parasitic coupling effect for planer transformer. A series RLC branch instead of a single capacitor was used. It's believed that this improved scheme is also applicable to helical transformer. Thus, a series RLC branch, including C_0, L_0 and R_0, is employed as shown in the proposed model.

For a helical inductor, the quality factor of the lower terminal is usually very small due to large parasitic terminal-to-substrate capacitance. Hence, the lower terminals of the inner and the outer inductors are most likely connected to ground in practical circuit design. As a result, the lowest metal actually works like a shielding for the upper metal layers from the substrate, and the substrate network is unnecessary and not considered in the proposed model.

3 Measurement and model extraction

Three square helical transformers were fabricated. Fig. 2 shows the chip photo of each device and corresponding design parameters, the outer diameter D and turn width W. The spacing between the inner and the outer inductors is fixed at 2 µm. Because the lower terminal of each port is grounded, the helical transformer is actually a two-port device. Hence, the two-port scattering parameters (S-parameter) are measured on the probe station. After measurement and de-embedding [9], a fitting process was applied to extract model parameters. Generally, it is important to make an appropriate initial guess for each model parameter in order to reach a reasonable and accurate fitting result.

As stated above, L_1 and L_2 are viewed as the dc inductance, so the classical Greenhouse's method is effective to make an initial guess [10]. And actually, the mutual inductance, hence the coupling coefficient k_0, can also be estimated by the Greenhouse's method. R_1 and R_2 are viewed as dc resistance and easy to be obtained with the square resistances of the metal. For C_1 and C_2, the analytical method in [5] is proved to be accurate for stacked inductors, including helical inductors. For the coupled RL loop, according to the circuit model in Fig. 1b, the impedance X_1 (X_2) from the upper terminal of L_1 (L_2) without considering the effect of k_0 can be expressed as

$$X_{1,2} = j\omega L_{1,2} + \frac{\omega^2 k_{1,2}^2 L_{1,2}}{X_{e1,e2}/L_{e1,e2} + j\omega} \tag{1}$$

where X_{e1} (X_{e2}) is the impedance of the dashed box and ω is the angular frequency. From the equation, it can be found that X_{e1} (X_{e2}) and L_{e1} (L_{e2}) are correlated. That

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is to say, only one parameter is independent and needs to be determined. Hence, we can fix L_{e1} and L_{e2}, and let X_{e1} and X_{e2} go through the fitting process. In this paper, we choose 1 nH for L_{e1} and L_{e2}. For C_0, L_0 and R_0, though the equations in [8] are proposed for planer transformer, they are still feasible qualitative estimations for helical transformer.

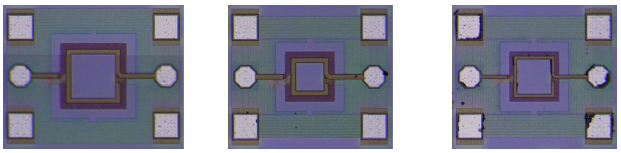

Fig. 2. Chip photos of the devices with various design parameters (unit: μm). The spacing between the inner and the outer inductors is 2 μm.

Table I. Extracted model parameters of fabricated transformers

	T1	T2	T3
R_1	12.37 Ω	9.216 Ω	14.42 Ω
L_1	6.661 nH	4.400 nH	5.167 nH
C_1	136.6 fF	101.3 fF	76.56 fF
L_{e1}	1 nH	1 nH	1 nH
R_{e1}	21.87 Ω	24.84 Ω	28.94 Ω
R_{s1}	35.51 Ω	34.68 Ω	50.17
L_{s1}	2.998 nH	2.590 nH	4.186 nH
k_1	0.460	0.500	0.422
R_2	14.93 Ω	10.08 Ω	17.27 Ω
L_2	10.97 nH	6.267 nH	8.484 nH
C_2	86.90 fF	59.47 fF	50.74 fF
L_{e2}	1 nH	1 nH	1 nH
R_{e2}	66.48 Ω	147.8 Ω	99.29 Ω
R_{s2}	61.56 Ω	57.14 Ω	105.2 Ω
L_{s2}	2.696 nH	2.375 nH	4.021 nH
k_2	0.433	0.497	0.421
C_0	50.37 fF	40.32 fF	35.69 fF
L_0	1.393 nH	0.6396 nH	1.002 nH
R_0	17.85 Ω	12.52 Ω	21.93 Ω
k_0	0.566	0.517	0.586

With proper initial guess, the final fitting process converges fast. Table I lists the extracted parameters of all three devices. It's worth noting that the initial calculated k_0 for the three devices are 0.583, 0.522 and 0.602, respectively, which are close to the final extracted values. Fig. 3 shows the measured data and the final fitted curves of all three devices. The port inductance and quality factor are calculated as:

$$L_{p1} = imag(Z11)/\omega, \quad L_{p2} = imag(Z22)/\omega \tag{2a}$$

$$Q_{p1} = imag(Z11)/real(Z11), \quad Q_{p2} = imag(Z22)/real(Z22) \tag{2b}$$

where the subscript of "p1" and "p2" indicate Port1 and Port2, respectively, and $Z11$ and $Z22$ are impedance parameters (Z-parameter) of the transformer. It's

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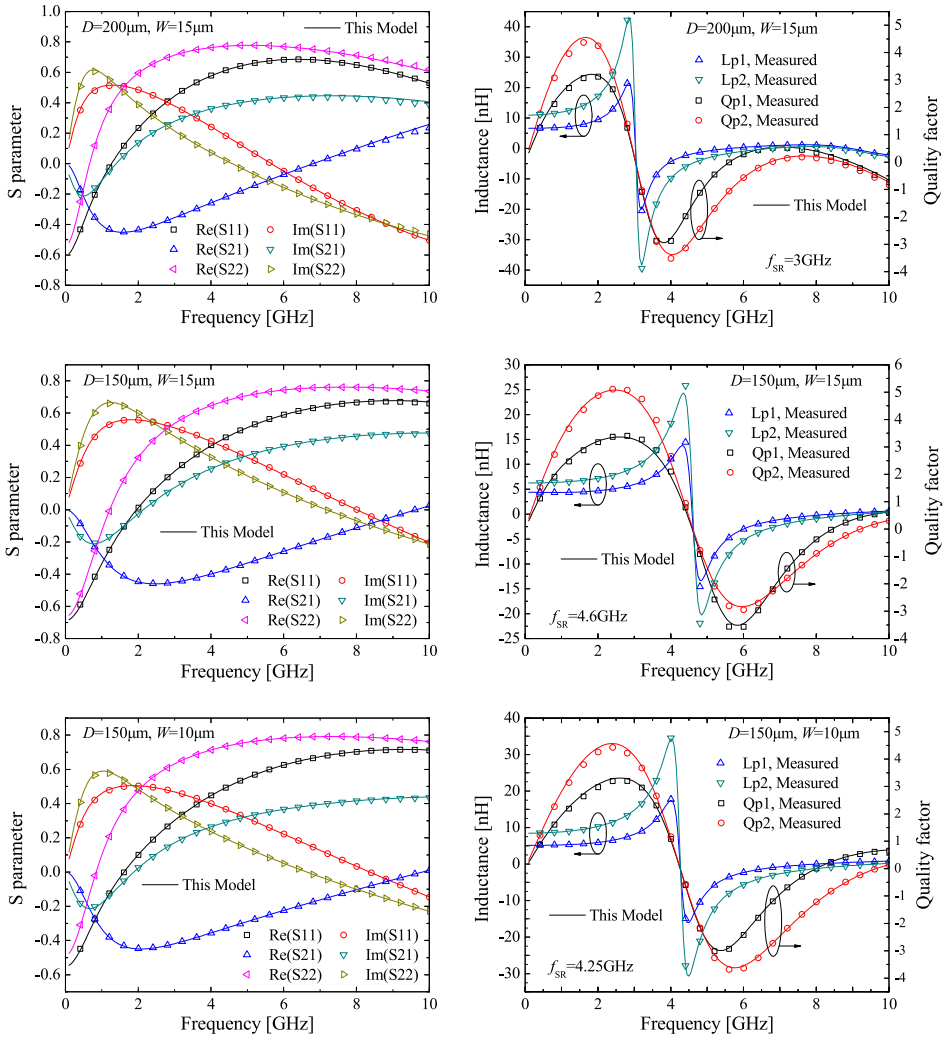

Fig. 3. Measured and fitted scattering parameters, port inductance and quality factor of (a) T1, (b) T2 and (c) T3. The subscript of "p1" and "p2" represent Port1 and Port2, respectively.

shown that the proposed model fits measured data very well. Moreover, it can be found that the model is effective for over two times self-resonance frequency.

4 Conclusion

A compact equivalent lumped circuit model for on-chip helical transformers is proposed. A simple coupled *RL* loop for the skin and proximity effect and a series *RLC* branch for the parasitic coupling effects between inductors are added into the fundamental model. Based on the measurement results, it has been verified that the proposed model is accurate for over two times self-resonance frequency, which makes it suitable for the design of high-speed and radio-frequency circuits.

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