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A low power accelerometer system with hybrid signal output

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Abstract: A low power micromechanical capacitive accelerometer system is presented with hybrid signal output in this paper. Correlated-double-sample (CDS) technique is utilized in the front end circuit to ensure low noise output signal. The accelerometer system provides direct digital output, and analog output is also available. The chip is implemented in a standard 0.35 µm CMOS process with a power dissipation of 19 mW from a single 5 V supply. The digital output signal achieved a noise floor of 2 µg/$\sqrt{\text{Hz}}$, and the precision of analog output signal is 3.75 µg/$\sqrt{\text{Hz}}$.

Keywords: accelerometer, hybrid signal output, CDS

Classification: Integrated circuits

References

[1] L. Aaltonen and K. Halonen: "Continuous-time interface for a micromachined capacitive accelerometer with NEA of 4 µg and bandwidth of 300 Hz," Sens. Actuators A: Phys. **154** (2009) 46 (DOI: 10.1016/j.sna.2009.07.011).

[2] H. L. Xu, *et al.*: "A closed-loop ΣΔ interface for a high-Q micromechanical capacitive accelerometer with 200 ng/$\sqrt{\text{Hz}}$ input noise density," IEEE J. Solid-State Circuits **50** (2015) 2101 (DOI: 10.1109/JSSC.2015.2428278).

[3] M. Yücetaş, *et al.*: "A high-resolution accelerometer with electrostatic damping and improved supply sensitivity," IEEE J. Solid-State Circuits **47** (2012) 1721 (DOI: 10.1109/JSSC.2012.2191675).

[4] H. Xu, *et al.*: "A high-order closed-loop ΣΔ interface for micro-machined accelerometer sensor," Analog Integr. Circuits Signal Process. **82** (2015) 401 (DOI: 10.1007/s10470-014-0436-4).

[5] H. Xu, *et al.*: "Harmonic distortion analysis for switched-capacitor electro-mechanical Sigma-Delta modulators," IEEE Sensors J. **15** (2015) 4826 (DOI: 10.1109/JSEN.2015.2427391).

[6] B. V. Amini, *et al.*: "A 4.5-mW closed-loop ΣΔ micro-gravity CMOS SOI accelerometer," IEEE J. Solid-State Circuits **41** (2006) 2983 (DOI: 10.1109/JSSC.2006.884864).

[7] M. A. Lemkin: "Micro accelerometer design with digital feedback control," Ph.D. Dissertation, Univ. California, Berkeley, CA, USA (1997).

[8] K. C.-H. Chao, *et al.*: "A higher order topology for interpolative modulators for oversampling A/D converters," IEEE Trans. Circuits Syst. **37** (1990) 309 (DOI: 10.1109/31.52724).

[9] R. Schreier and G. C. Temes: *Understanding Delta-Sigma Data Converter* (IEEE Press, New York, 2005).

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Publicized January 9, 2018
Copyedited February 25, 2018

[10] B. C. Kuo and F. Golnaraghi: *Automatic Control System* (John Wiley & Sons, Inc, 2003) 397.
[11] L. Aaltonen and K. Halonen: "Integrated high-voltage PID controller," Baltic Electronics Conference (2008) 125 (DOI: 10.1109/BEC.2008.4657494).

1 Introduction

Capacitive accelerometers, often operating in a closed loop, have the characters of good linearity and resolution and a high signal bandwidth, and gain increasing popularity [1, 2]. In order to achieve low-noise performance, a low-noise sensor element with high quality factor (Q) is needed to be incorporated in a high-order sigma-delta loop. This could obtain direct digital output signal, but it will complicate the design due to the stability issue. A high-Q sensor element increases the settling time, which requires an electronic damping by electrostatic feedback force [3]. Meanwhile, a high-Q sensor element in a high-order loop needs heavy phase compensation to maintain a stable system. To simplify the design, a low-Q sensor element with 1 $\mu g/\sqrt{Hz}$ noise floor can be applied, which meets most of the high performance applications [4].

Despite sigma-delta interface circuits for capacitive accelerometers provide direct digital output and are insensitive to process variation, they face the truth that noise folding effects, residual motion and high clock frequency sampling will limit the overall performance of the sensor. Therefore, continuous-time readout is also popular in some applications. Usually a high precision ADC is used to convert the analog output signal to the digital domain using the same reference voltage as the interface to eliminate the supply dependence of the output [3].

In order to achieve a high performance accelerometer system with relative low power dissipation, a hybrid interface circuit with continuous-time readout and sigma-delta closed-loop is designed to get the above-mentioned advantages of both topologies.

2 Sensing element and system

Fig. 1 shows the overall blocks with detailed front-end charge sensing amplifier and correlated-double-sampling. The equivalent half-bridge model of the bulk micromachined accelerometer in Fig. 1 consists of variable capacitors C_{S1} and C_{S2}. The sensitive capacitance C_f is 10 pF, and C_c and C_H is both 5 pF. A larger sampling capacitor will increase the phase shift. Equation (1) presents the acceleration-to-displacement transfer function of mechanical sensing element.

$$H_{ms}(s) = \frac{x(s)}{a_{in}(s)} = \frac{1}{s^2 + \frac{b}{m}s + \frac{k}{m}} \tag{1}$$

where b, k and m are the damping coefficient, the spring constant and the proof mass, respectively. The function can be transferred to equation (2) in low frequency.

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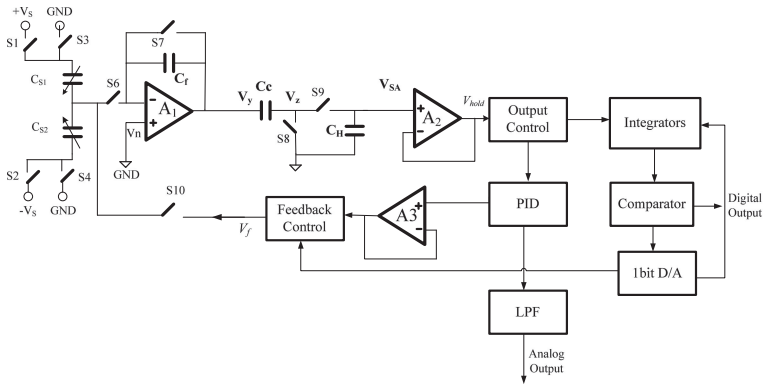

Fig. 1. The overall blocks with detailed front-end charge sensing amplifier and correlated-double-sampling

$$\frac{x}{a_{in}} = \frac{1}{w_0^2} \tag{2}$$

where $w_o = \sqrt{\frac{k}{m}}$. Therefore, the low frequency acceleration can be linearly converted to the change of the variable capacitors C_{S1} and C_{S2}. To avoid the stability issue of the high-order digital path, a low-Q sensor element with 1 μg/$\sqrt{}$Hz noise floor is applied, and it is not necessary to insert a phase compensator into the high-order loop. Fig. 2 gives the main timing schematic of the front end circuit. Due to the correlated-double-sampling (firstly s8 turns on to sample the low frequency noise, then s8 turns off and s9 turns on, and the low frequency noise and signal are both sampled), the low frequency noise Vn can be eliminated, and the high-precision signal V_{SA} is achieved as shown in (3) [5, 6, 7].

$$V_{SA} = V_z - V_y = V_S \frac{C_{S1} - C_{S2}}{C_f} \tag{3}$$

The sampled and hold signal V_{SA} is chosen by the output control block to select the signal path. The analog output signal path consists of a proportional-integral-derivative controller (PID controller), a low pass filter (LPF) and a hold amplifier A3. The digital output signal path includes the integrators, comparator and 1 bit DAC. The analog output signal path feedback and digital output signal path feedback is chosen by the feedback control.

3 Main block circuits

Fig. 3 shows a third order sigma-delta modulator in the digital path, and the distributed feedback capacitor is not shared with the sampling capacitor to achieve small distributed feedback factor [8]. The sampling capacitance C_{s1} of the first integrator is 1 pF, and other sampling capacitances are scaled down due to the front-end gain to shape the noise and linearity, therefore, the power dissipation and chip area decreases [9]. The operational amplifier of the first integrator is a gain-boosting topology to enhance the low-frequency direct current (DC) gain, and the second and third integrators have a differential single-stage folded-cascode topology. P1 and P2 are non-overlap clocks, which are also given in Fig. 3. The quantizer in Fig. 3 consists of a dynamic comparator and a latch. The output bit stream signal Vd is converted to analog feedback signal V_f by the 1 bit DAC. The modulator consumes a power of 2 mW.

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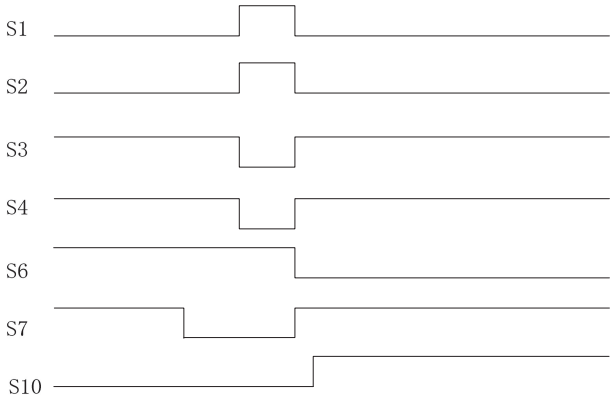

Fig. 2. Main timing schematic of the front end

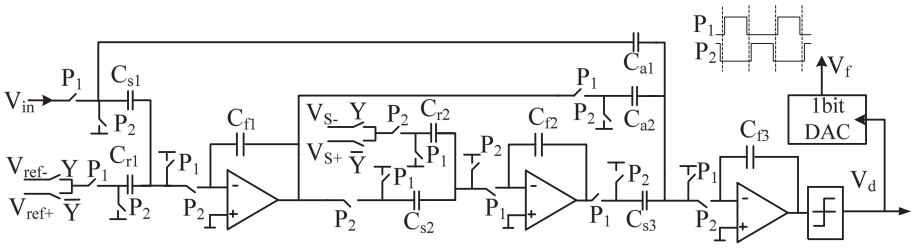

Fig. 3. Sigma-delta modulator in the digital path

The PID controller for the analog feedback loop is illustrated in Fig. 4. The PID controller is effective especially for a vacuum-packaged sensor element.

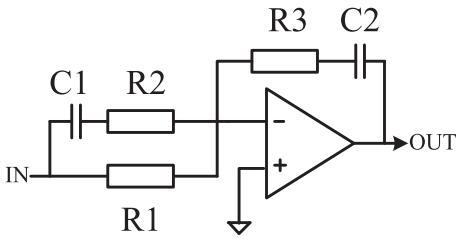

Fig. 4. PID controller for the analog feedback loop

The transfer function of the PID controller is shown in (4) [10], and $K_p = -R_3/R_2$, $K_D = -1/R_2C_2$, $K_1 = -1/C_1R_3$. For a PD controller, $K_1 = 0$ [11].

$$H(S) = K_p + K_D s + \frac{K_1}{S} \tag{4}$$

The PID controller introduces a zero point located in the $-K_D/K_P$ in the closed-loop transfer function, which compensates the damping ratio of the analog closed-loop system and improves the stability of the system with a low damping sensor element. The static power dissipation of the PID is less than 1 mW. The output of PID is filtered by a passive LPF, which provides high-precision analog output signal. The PID output is also buffered by an OPA with a high DC gain to drive the sensor element.

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4 Measurement results

The low power interface circuit for the accelerometer system was fabricated in a standard 0.5 µm CMOS process. Fig. 5 shows the chip micrograph with active circuit area measured $2.5 \times 3\,\text{mm}^2$. A low-Q capacitive bulk micromachined accelerometer with Brown noise near $1\,\mu\text{g}/\sqrt{\text{Hz}}$ is wire-bonded to the chip. The system including analog and digital loop is powered by a single 5 V supply. The sampling clock is 125 kHz, which is divided from an on-chip oscillator with 1 MHz frequency. The whole power dissipation is 19 mW.

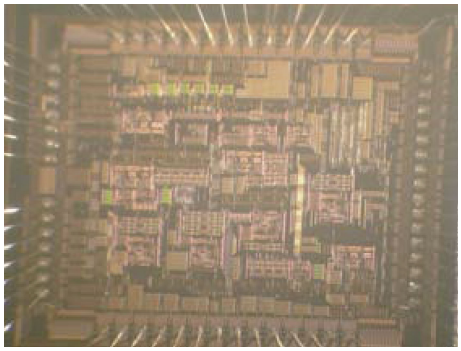

Fig. 5. Chip micrograph

The closed-loop sensitivity is 1.2 V/g by performing the system on a dividing head. The PSD result of the analog output is given in Fig. 6. The measured low frequency noise below 100 Hz is lower than $-105\,\text{dB}/\sqrt{\text{Hz}}$, which results in an equivalent $3.75\,\mu\text{g}/\sqrt{\text{Hz}}$ low frequency floor. The digital output is captured by Agilent Logic Analyzer 16804A and processed in Matlab program. A 65536-point bit stream is calculated and shown in Fig. 7. The low frequency noise is eliminated by the CDS technique, and a low noise floor of $-120\,\text{dB}/\sqrt{\text{Hz}}$ is achieved. The equivalent input acceleration noise is about $2\,\mu\text{g}/\sqrt{\text{Hz}}$ below 1 kHz bandwidth.

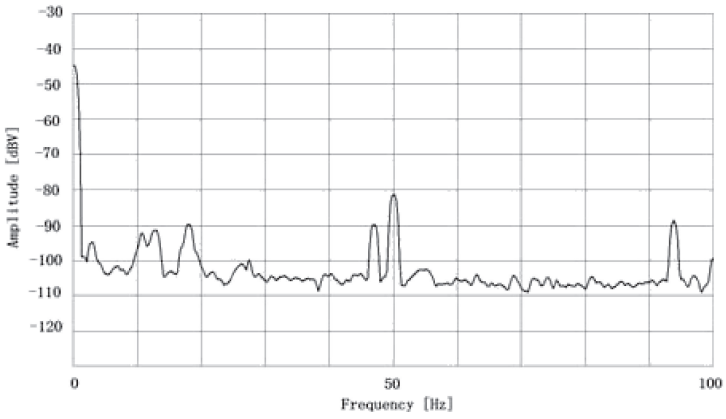

Fig. 6. PSD result of the analog output

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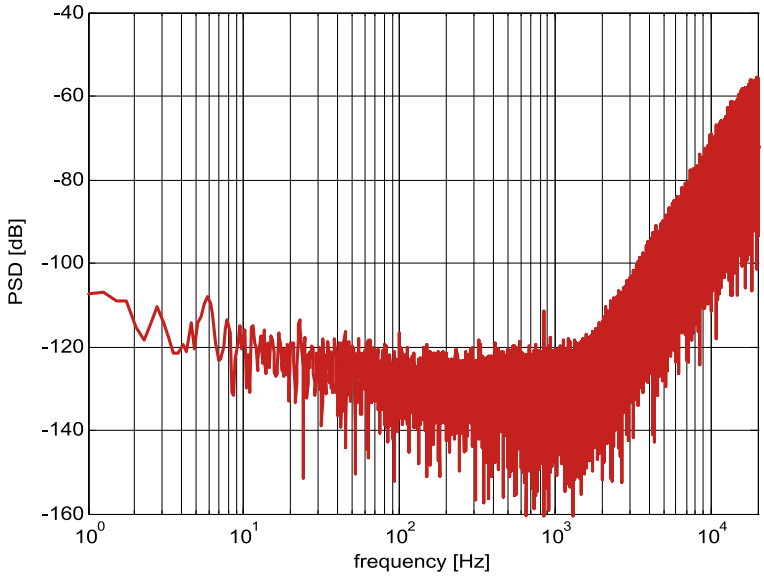

Fig. 7. Measured PSD of the closed-loop digital micromachined accelerometer

5 Conclusion

This work achieved a hybrid system with analog and digital output signal for a capacitive accelerometer by dissipating a power of only 19 mW. The measured closed-loop sensitivity of the loop is 1.2 V/g. An equivalent 3.75 $\mu g/\sqrt{Hz}$ low frequency floor is achieved for the analog loop and 2 $\mu g/\sqrt{Hz}$ for the digital loop with a 1 kHz bandwidth.

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