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# Electronic UWB tunable true-time delay line for timed array antennas

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**Abstract:** This study presents a silicon-based ultra-wideband (UWB) true-time delay line for timed array antennas. The proposed circuit uses the novel active switches to mitigate performance deterioration from on-off switching. The proportional-to-absolute-temperature (PTAT) biasing circuit and scaling technique are adopted to improve the gain stability against the PVT variation at the different delay settings. The experimental prototype is fabricated in a 0.13 µm SiGe BiCMOS process, and exhibits a maximal relative delay of 35 ps with an average of 5 ps over a frequency range of 14–34 GHz. The chip occupies an area of 0.62 $mm^2$, and the measured average input 1-dB compression point is 13 dBm.

**Keywords:** ultra-wideband (UWB), true-time delay line, timed array

**Classification:** Microwave and millimeter-wave devices, circuits, and modules

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## 1 Introduction

In communication systems, a true-time delay line (TTDL) has wide applications, such as wideband beamforming, delay-locked loops and equalizers [1, 2, 3]. For timed array receivers, the TTDL not only mitigates the beam squinting, but also provides a constant delay response to enhance signal-to-noise ratio (SNR).

Various techniques including passive and active methods have been used to realize the TTDLs. Even if the MEMS-based (Micro-Electro-Mechanical System) TTDL and the photonic TTDL provide favorable delay performance, they are not suitable for integrated and low-cost systems due to the bulky size and complex process [4]. The active solutions based on RC or $g_m$-C filters can be accomplished in a small chip area; however, it requires a calibration technique to improve the delay accuracy at low-GHz frequencies [5].

This work employs RF interconnect line replacing lumped inductor with low inductance and relative high quality factor as basic delay element for high frequency applications. This proposed TTDL uses the novel active switches, PTAT (proportional-to-absolute-temperature) biasing and scaling technology to optimize the performance. Compared to the conventional TTDL using transmission line, it provides a small DV over a large frequency range with picosecond-delay resolution in a compact chip area.

## 2 True-time delay line circuit design

The circuit architecture of the proposed variable TTD is shown in Fig. 1, which adopts a trombone structure using RF interconnect line (IL) and capacitor as the basic delay element. The structure increases the operating frequencies within a certain DV and reduces the high-frequency loss due to low inductance with


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relatively high quality factor. The delay time is adjusted through activating one of the eight active switches ($S_1$ to $S_8$) to change signal path. The minimal relative delay time, i.e. delay resolution, is achieved by the two sections of IL and $C_P$. That is expressed as

$$T_D = 2\sqrt{LC_P} \tag{1}$$

where $L$ is the inductance of IL. The two sections composed of $IL_9$, $C_{d1}$ and $IL_9$, $C_d$ are placed at the input and output terminals of $S_8$ to accomplish the load matching. For reducing DV, the resistances $R_{d1}$ and $R_{d2}$ are equal to load impedance to realize the impedance matching. The impedance of the delay line is calculated as

$$Z(\omega) = \sqrt{\frac{L}{C_P}} \cdot \sqrt{1 - \frac{LC_P\omega^2}{4}} = Z_0 \cdot \sqrt{1 - \frac{LC_P\omega^2}{4}} \tag{2}$$

where $Z_0 = \sqrt{L/C_P}$ is the characteristic impedance of the delay line [6].

The power supply VDD is connected to $R_{d1}$ and $R_{d2}$ instead of placing at the output terminal of a certain active switch in [7]. Compared to Ref. [7], this proposed structure cancels a choke inductor and avoids impedance inconsistency caused by the choke inductor, which can reduce the chip area and improve the delay flatness. It exists a trade-off among delay resolution, impedance matching, bandwidth and chip area; thus, the device sizes need to be calculated prior to designing.

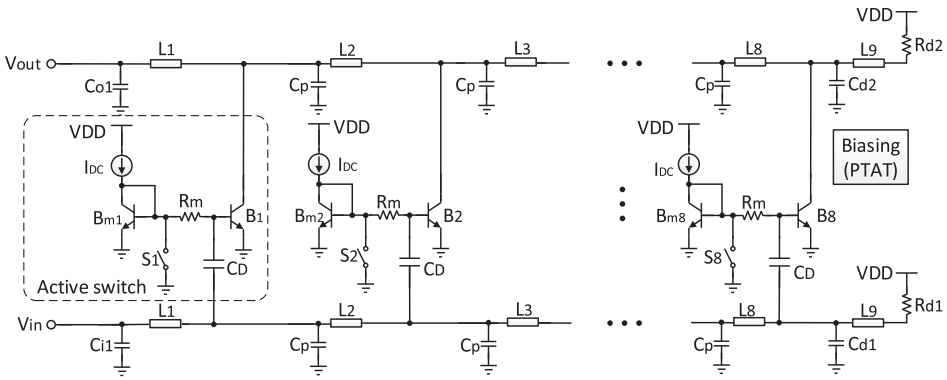


**Fig. 1.** Proposed 3-bit trombone true-time delay line circuit

## 2.1 Active switch

The proposed active switch consists of a transistor amplifier, current biasing, MOS switch and DC-blocking capacitor as shown in Fig. 1. The switches ($S_1$–$S_8$) are applied to control the base biasing currents of amplifiers ($B_1$–$B_8$). Differing from [8, 9], the switching amplifier removes the cascode topology used as on-off switching operation. Alternatively, the proposed active switch places switches to control the bias current and adds the DC-blocking capacitors at the input terminal. The modification has three advantages: first, this structure eliminates one collect-emitter voltage drop; second, the change reduces the parasitic capacitors and improves the effective frequency range; and third, the cancellation of the switch at the signal path reduces the on-off parasitic capacitance variation that is benefit for delay flatness.


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At the input terminal, the DC-blocking capacitor can absorb the the on-off capacitance variation, which is advantageous to the impedance matching and delay flatness in on-off switching operation. Assuming the difference of on-off capacitance is $\Delta C_o = |C_{on} - C_{off}|$ at the input terminal without DC-blocking capacitor, $C_{on}$ and $C_{off}$ are parasitic capacitances at the on and off states, respectively, and the DC-blocking capacitance is $C_D$. Thus for the proposed structure, the variation of the on-off capacitance is given by

$$\Delta C_{proposed} = \left| \frac{C_{on} \cdot C_D}{C_{on} + C_D} - \frac{C_{off} \cdot C_D}{C_{off} + C_D} \right| = \left| \frac{C_D^2 \cdot \Delta C_o}{(C_{on} + C_D) \cdot (C_{off} + C_D)} \right| \quad (3)$$

$$\Delta C_{proposed} < \Delta C_o = |C_{on} - C_{off}| \quad (4)$$

Fig. 2 shows the proposed circuit is less capacitance variation than those at the input and output terminal of [7] as the inequality (4) describes.

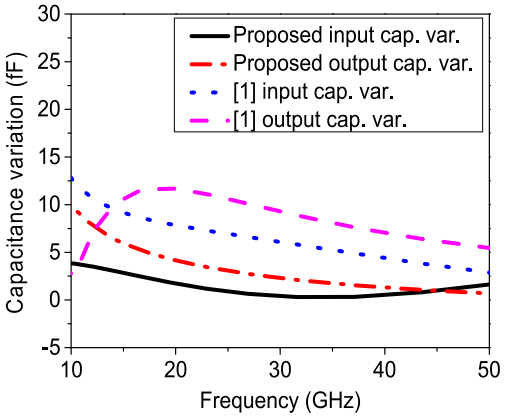


**Fig. 2.** Comparison of the input and output capacitance variation between the proposed and conventional structure

## 2.2 Gain immune to process, voltage and temperature (PVT) variation

The proposed delay line employs PTAT as the biasing circuit to achieve a stable gain against temperature and supply variation. Fig. 3(a) and (b) shows the proposed PTAT biasing circuit and the op-amp used in the PTAT. The cascode current mirror composed of $M_1$–$M_4$ is used to improve the power supply rejection (PSR) by mitigating the channel-length modulation [10]. Equation (5) gives the formulas derivation, which explains the gain $A_{v0}$ of the delay line is irrelative with temperature using PTAT biasing.

$$A_{v0} = g_m \cdot R_o = \frac{I_{PTAT}}{V_T} \cdot R_o = \frac{\Delta V_{BE}}{V_T \cdot R_1} \cdot R_o = \frac{\ln n}{R_1} \cdot R_o \quad (5)$$

where $V_T$, $n$, $g_m$ and $R_o$ are thermal voltage, the emitter area ratio of $B_2$ to $B_1$, transconductance of active switch and output impedance of the delay line, respectively. Obviously, the gain $A_{v0}$ in Eq. (5) is irrelative with PVT. The loop gain and PSR at DC are respectively given by


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$$A_{\text{loop}}(0) = g_{\text{m3,4}}(R_{\text{Y}} - R_{\text{X}})A_1 \tag{6}$$

$$\text{PSR} = \frac{i_{\text{PTAT}}}{v_{\text{dd}}} = \frac{1 - A_{\text{vdd}}}{A_1(R_{\text{Y}} - R_{\text{X}}) + \dfrac{1}{g_{\text{m1,2}}}} \tag{7}$$

where $R_{\text{X}}$, $R_{\text{Y}}$ and $A_{\text{vdd}}$ mean the output impedance of node X, Y and supply-to-output gain of $A_1$. Equations (6) and (7) explain that a large open-loop gain $A_1$ leads to a higher loop gain and a lower PSR, which mean that the delay line has less gain fluctuation from temperature and supply variation [11]. The op-amp $A_1$ adopts a two-stage current mirror amplifier as shown in Fig. 3(b). Based on Equation (7), $A_{\text{vdd}}$ approximately equals to unity that can reduce PSR. Fig. 4 shows that the simulated S21 of the delay line with and without PTAT biasing circuit for different PVT in the longest delay state at 16 GHz. The comparison shows that the gain deviation without PTAT is larger than that with PTAT, and the proposed technique can provide the gain stability against PVT variation for the delay line circuit.

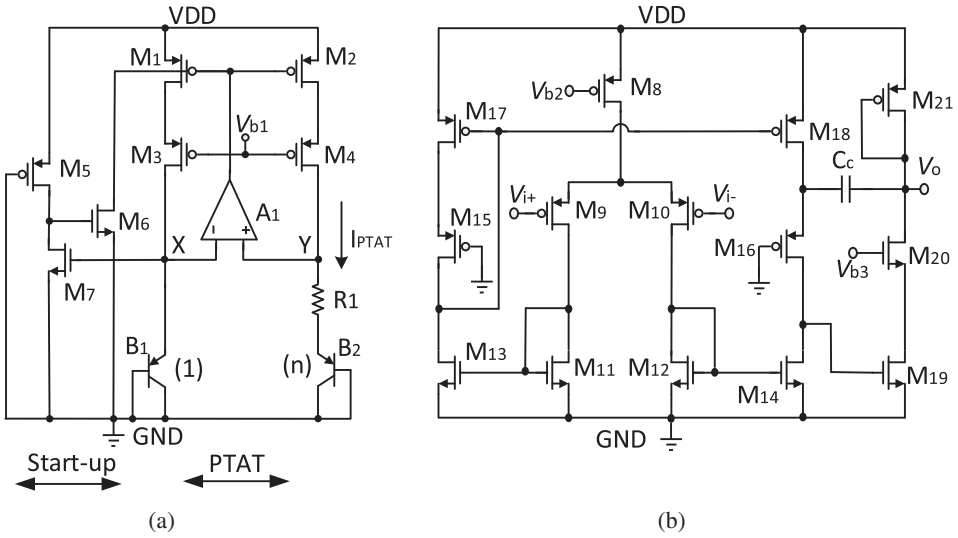


**Fig. 3.** (a) PTAT biasing circuit (b) Op-amp used in the PTAT

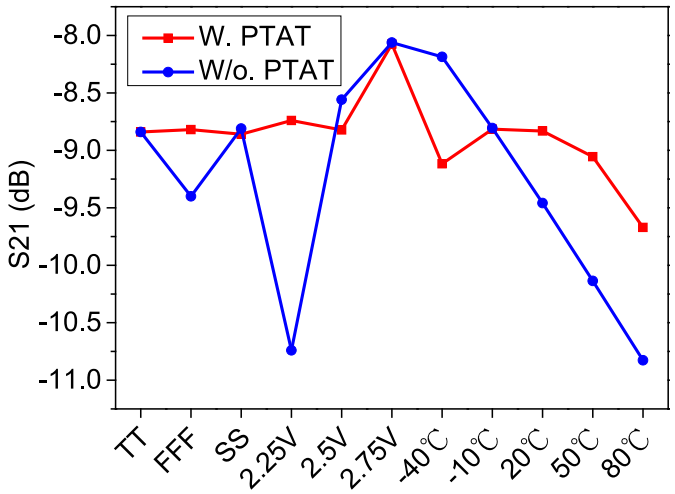


**Fig. 4.** Simulated S21 vs. PVT comparison with and without PTAT


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### 2.3 Scaling technology and impedance matching

In order to solve the gain variation caused by passive trombone structure at the different delay states, the scaling active switch size technology is proposed. The delay line loss is increased as a longer delay line length is set. By enlarging the active switch size as the delay line length increases, the gain loss variation is diminished.

In high frequency application, the impedance matching is an important design consideration, which determines the delay flatness and return loss over frequency band for all delay settings. Considering the parasitic effects, the input/output impedance of the each path switch, layout and electromagnetic (EM) simulation need be designed carefully.

## 3 Experimental results

The proposed delay line circuit is fabricated in a 0.13 µm SiGe BiCMOS process. A photograph of the chip is shown in Fig. 5, and the die area is $1.75 \times 0.35\,\text{mm}^2$ including pads. The circuit is measured on wafer with a SGS probe (ACP40-D) and two DC probes probes (MCW-13-3244-9).

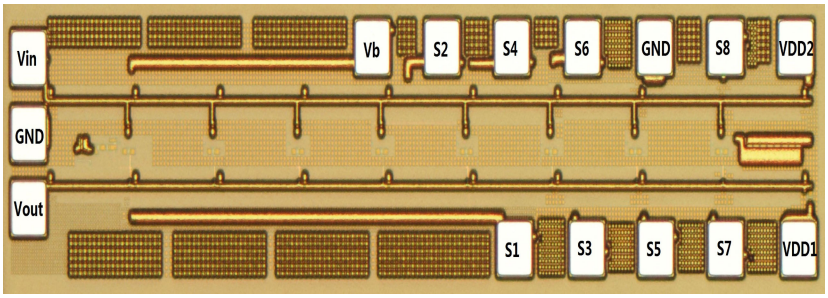


**Fig. 5.** Chip micrograph of the TTDL

The group delay and S-parameters are tested with an Agilent E8363B vector network analyzer. The measured results of the group delay are shown in Fig. 6(a), and the delay resolution is approximately 5 ps and the maximal relative delay of delay line can reach approximately 35 ps within 10% delay variation. The measured S21 is shown in Fig. 6(b), which presents a nominal gain of −11.5 dB and ±1.5 dB gain variation. The measured input and output matching performance at all delay settings is shown in Fig. 6(c). The measured input 1-dB compression point ($P_{1dB}$) at the shortest delay path over a frequency range of 1–40 GHz is shown in Fig. 6(d), and the average $P_{1dB}$ is 13 dBm. Table I shows the performance summary and comparison with the previous published TTDLs. The proposed circuit has the advantages on the frequency range, gain stability, power, delay range and linearity. Fig. 7 shows that the on-wafer measurement circumstance of the proposed delay line chip on the probe station. The S-parameters measurement using a network analyzer is shown on the right of the photograph.


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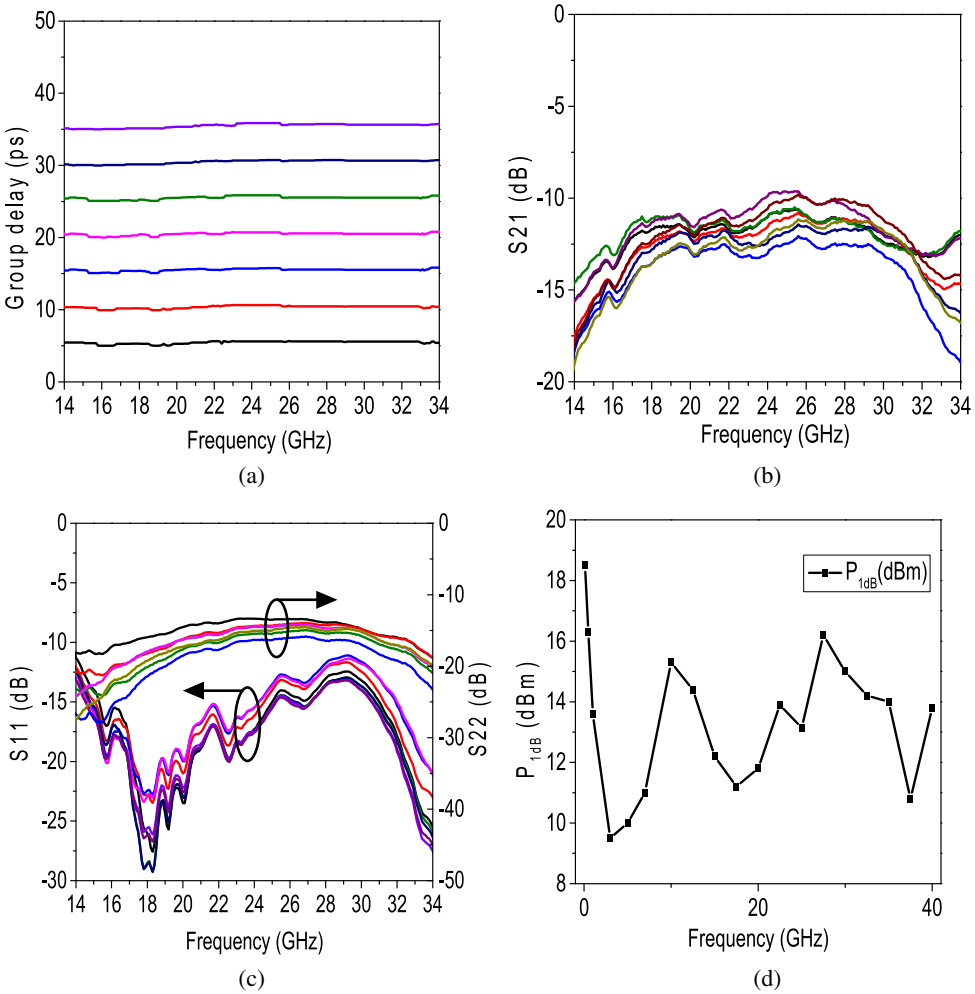


**Fig. 6.** Measured results of the TTDL (a) Measured group delay in reference to the shortest delay state, (b) Measured S21, (c) Measured S11 and S22, (d) Measured 1-dB compression point for the shortest delay path

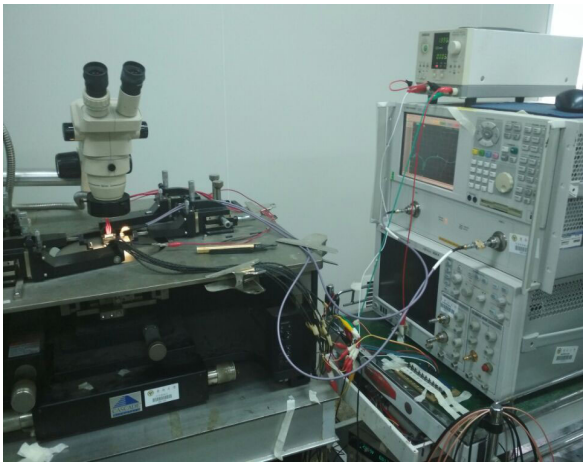

**Fig. 7.** Photograph of the measurement circumstance


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**Table I.** Performance summary and comparison

| Reference | [12] | [13] | [14] | [7] | This work |
|---|---|---|---|---|---|
| Technology | 0.13 µm SiGe | 0.8 µm SiGe | 90 nm CMOS | 0.13 µm CMOS | 0.13 µm SiGe |
| Frequency (GHz) | 55–65 | 3–10 | 0–8 | 15–40 | 14–34 |
| Max delay (ps) | 16 | 25 | 26 | 36 | 35 |
| Resolution (ps) | 1.2 | Cont. | 13 | 5.2 | 5 |
| Delay variation | N.A. | 40% | 10% | >20% | 10% |
| Nominal gain (dB) | N.A. | −4.5 | −4 | −14 | −11.5 |
| Gain variation (dB) | N.A. | ±0.7 | ±3 | ±2 | ±1.5 |
| Average $P_{1dB}$ (dBm) | N.A. | N.A. | N.A. | +8 | +13 |
| Power (mW) | Passive | 38.8 | Passive | 8.6–24.6 | 7.4–14 |
| Size ($mm^2$) | 0.35 | 0.23 | N.A. | 0.99 | 0.62 |

## 4 Conclusion

An ultra-broadband true-time delay line is presented for timed array antennas. The delay line uses trombone structure with passive delay cells and novel active switches to improve the delay stability. The PTAT biasing and scaling technique are analyzed and designed to reduce gain variation due to PVT variation at all delay settings. The proposed circuit is verified by experiment and presents the better performance on frequency range, gain stability, power, maximal delay and linearity.

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