ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.15, No.4, 1–7

# Design and implementation of the optimized digital controller with the simplified control algorithm for boost power factor correction converter

**Daying Sun**[a)], **Yu Yao, Wenhua Gu, and Li Li**

*School of Electronic and Optical Engineering,*

*Nanjing University of Science and Technology, 200 Xiaoling Wei, Nanjing, China*

a) *hasdysun@126.com*

**Abstract:** The design and implementation of a digital controller for a boost power factor correction (PFC) converter under continuous current mode is presented to reduce the harmonic distortion. Based on the circuit structure of boost PFC converter, the total digital control loop is simply implemented to improve the power factor of converter and reduce the calculation burden of digital controller. Meanwhile, the optimized digital pulse width modulator (DPWM) is adopted to improve the regulation performance of digital controller. The boost PFC converter with the proposed digital controller has been implemented via the FPGA platform, and experimental results indicate that the digital PFC converter with the proposed digital controller can aim high regulation linearity, power factor and output stability.

**Keywords:** power factor correction, continuous current mode, digital controller, digital pulse width modulator, high power factor

**Classification:** Integrated circuits

## References

[1] R. L. Newsom, *et al.*: "Digital power-factor correction for a capacitor-charging power supply," IEEE Trans. Ind. Electron. **49** (2002) 1146 (DOI: 10.1109/TIE.2002.803240).

[2] Y. Cho and J. Lai: "Digital plug-in repetitive controller for single-phase bridgeless PFC converters," IEEE Trans. Power Electron. **28** (2013) 165 (DOI: 10.1109/TPEL.2012.2196288).

[3] Y. S. Lai and C. A. Yeh: "Predictive digital-controlled converter with peak current mode control and leading edge modulation," IEEE Trans. Ind. Electron. **56** (2009) 1854 (DOI: 10.1109/TIE.2008.2009510).

[4] S. Bibian and H. Jin: "High performance predictive dead-beat digital controller for DC power," Appl. Power Electron. Conf. (2001) 67 (DOI: 10.1109/APEC.2001.911629).

[5] W. Zhang, *et al.*: "A new duty cycle control strategy for power factor correction and FPGA implementation," IEEE Trans. Power Electron. **21** (2006) 1745



DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

(DOI: 10.1109/TPEL.2006.882922).
[6] A. V. Peterchev and S. R. Sanders: "Quantization resolution and limit cycling in digitally controlled PWM converters," IEEE Trans. Power Electron. **18** (2003) 301 (DOI: 10.1109/TPEL.2002.807092).
[7] J. Zhang and S. R. Sanders: "A digital multi-mode multi-phase IC controller for voltage regulator application," Appl. Power Electron Conf. Expo. (2007) 719 (DOI: 10.1109/APEX.2007.357594).
[8] Z. Lukic, *et al.*: "Multibit Σ-Δ PWM digital controller IC for dc-dc converters operating at switching frequencies beyond 10 MHz," IEEE Trans. Power Electron. **22** (2007) 1693 (DOI: 10.1109/TPEL.2007.904199).
[9] W. Zhang, *et al.*: "New digital control method for power factor correction," IEEE Trans. Ind. Electron. **53** (2006) 987 (DOI: 10.1109/TIE.2006.874255).
[10] A. Prodic, *et al.*: "Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers," IEEE Trans. Power Electron. **21** (2006) 173 (DOI: 10.1109/TPEL.2005.861157).
[11] S. F. Lim and A. M. Khambadkone: "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," IEEE Trans. Ind. Electron. **47** (2011) 1802 (DOI: 10.1109/TIA.2011.2153815).

## 1 Introduction

To reduce the input current harmonic pollution and improve the stability of power grid, power factor correction (PFC) converters have been widely used in the switching power converter systems [1]. Meanwhile, owing to the advantages such as improved flexibility and increased functionality offered by digital controller, digital control implementation has received more and more attention in the research of PFC system [2]. As shown in Fig. 1, the digital controller of digital PFC converter mainly includes three parts: analog-to-digital converter (ADC), digital compensator and digital pulse width modulator (DPWM).

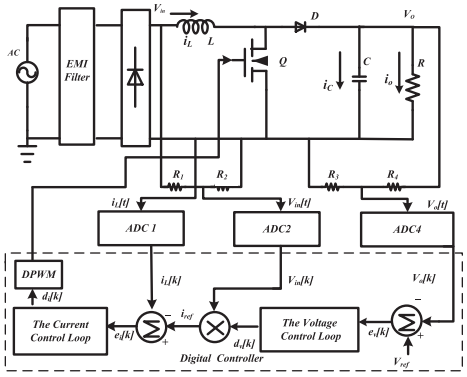


**Fig. 1.** The typical boost PFC converter structure With traditional digital controller

Based on the analysis of the above digital PFC converter structure, the performance improvement of such converter is often limited by relatively complex digital calculation process and restricted conversion resolution of ADC converter and DPWM module [3]. Several simplified digital controller methods have been presented to aim high power factor correction performance. The desired digital duty


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

cycle values are updated through the specific switching period instead of each switching cycle in [4], which could reduce digital calculation amount. A new duty cycle calculation method is proposed via the indirect digital calculation scheme to replace the traditional dual digital control loops in [5], which could simplify the control structure of digital controller. However, the accuracy of the desired digital duty cycle value is partly reduced. To further improve the regulation performance of digital PFC converter, high conversion resolution and regulation linearity are preferred for DPWM to reduce the regulation deviation, and the conversion resolution of DPWM module should be higher than the conversion resolution of ADC converter so as to prevent the limit-cycle status [6]. The hybrid DPWM is adopted to balance the clock frequency and hardware resource of the digital circuit when improving the conversion resolution. The digital dither [7] and sigma-delta technology [8] are respectively implemented to increase the effective conversion resolution by changing the pattern used in the generation of the output signal. However, the regulation linearity is limited owing to the affection of process, voltage and temperature of digital circuit.

In this paper, the digital controller for a single-phase boost power factor correction converter under continuous current mode is proposed to aim high power factor. Based on the circuit structure of boost PFC converter, the total digital control loop of PFC converter is simply implemented to improve the power factor of converter and reduce the calculation burden of digital controller. Meanwhile, the optimized digital pulse width modulator is adopted to further improve the regulation performance of converter.

## 2 The whole PFC converter structure with the proposed digital controller

The whole PFC converter structure with the proposed digital controller is shown in Fig. 2. The output voltage and inductor current of converter are sampled by ADCs, respectively. The proposed digital controller mainly consists of the simplified digital control algorithm and the optimized DPWM module. The desired digital duty cycle value of every switching cycle is calculated by the digital control algorithm, and the final duty cycle signal for the switching tube is converted via the DPWM module.

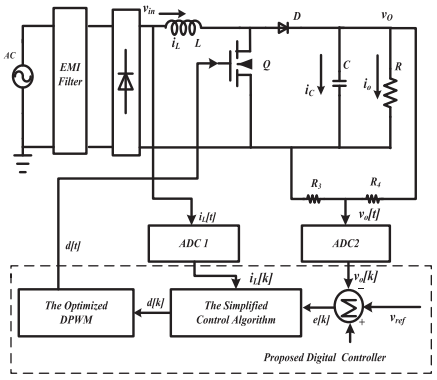


**Fig. 2.** The whole boost PFC converter structure with the proposed digital controller


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

### 2.1 The simplified control algorithm

The main purpose of PFC converter is to regulate the output voltage and input current. The output voltage of converter is expected to be stable near the specific reference value, and the input current of converter is expected to follow the input voltage of converter perfectly.

As shown in Fig. 1, in the traditional control scheme of digital PFC converter, the output voltage and the input current are respectively regulated by the voltage control loop and the current control loop. During every switching cycle, the data conversion in analog-to-digital domain and the implement of two control loops are included for digital controller, which means that digital calculation is complicated in every switching cycle. Meanwhile, three ADC converters are normally needed to execute the traditional two digital control loops, which will relatively improve the total cost of digital PFC converter.

Focusing on the main purpose of digital PFC converter, if the input current of converter is regulated to follow the input voltage perfectly, the whole digital PFC converter could be regarded as input resistance $R_{in}$, and the relationship between the input voltage and input current can be expressed as

$$v_{in} = i_{in}R_{in} \tag{1}$$

Meanwhile, when the digital PFC converter operating at continuous current mode, the relationship between the input voltage, the output voltage and the duty cycle ratio can be expressed as

$$v_{in} = v_o(1 - d) \tag{2}$$

Based on (1) and (2), the input current can be concluded as

$$i_{in} = v_o(1 - d)/R_{in} \tag{3}$$

When the equivalent current detection resistance of digital PFC converter is $R_d$, (3) can be modified as

$$i_{in}R_d = v_o(1 - d) \cdot R_d/R_{in} \tag{4}$$

According to *Ref.* [11], the output value of the voltage control loop is $v_m$, and $v_m = (v_o * R_d)/R_{in}$, (4) can be concluded as

$$i_{in}R_d = v_m(1 - d) \tag{5}$$

So the duty cycle value of every switching cycle $d$ can be concluded from (5), and the digital duty cycle value $d[k]$ can be expressed as

$$d[k] = 1 - \frac{R_d}{v_m[k]}\, i_{in}[k] \tag{6}$$

Compared to traditional two digital control loops used in digital PFC converter, based on the above principle as (6), the current control loop and the sampling of input voltage of PFC converter are without need, only the voltage control loop and two ADC converters are needed, which will reduce the calculation burden and total cost of digital controller effectively. The PI compensator is used in the design of the voltage control loop to regulate the output voltage to the reference voltage value, and the digital control law is


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

$$v_m[k] = v_m[k-1] + k_p e_v[k] + k_i e_v[k-1] \quad (7)$$

Where $e_v[k]$ and $e_v[k-1]$ are the errors between the output voltage of converter and the reference voltage during the $k_{th}$ and $(k-1)_{th}$ switching cycle, respectively.

## 2.2 The optimized DPWM

The DPWM module is adopted to realize the digital-to-analog conversion in digital PFC converter, the digital duty cycle value from the digital control algorithm is converted to the final analog duty cycle signal. High conversion resolution and regulation linearity via relatively low hardware resources are preferred for DPWM module, so as to reduce the regulation deviation and finally improve the regulation characters of digital PFC converter.

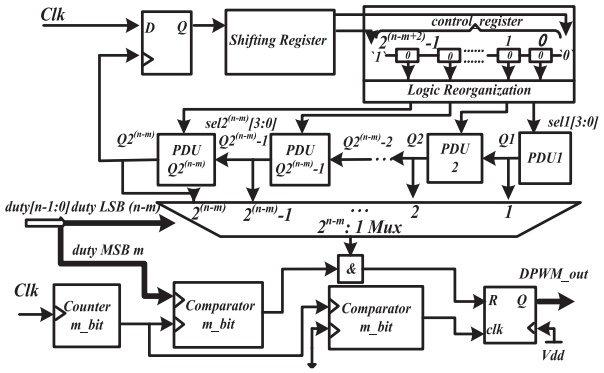


**Fig. 3.** The structure of the proposed optimized DPWM

Although many kinds of DPWM module architecture [8, 9, 10] are proposed to aim high conversion resolution and improve the regulation linearity via relatively low hardware resources, the detailed regulation and the coarse regulation of DPWM module are realized by the counter structure and the delay line structure, respectively. The final regulation linearity of DPWM module will still be inevitably influenced by the variation of the operating voltage or temperature during the conversion process. To reduce such influence due to the delay line structure of the DPWM module and improve the regulation linearity, a novel optimized DPWM module is proposed in the paper, and the detailed structure of DPWM module is shown in Fig. 3. The effective conversion resolution of the proposed DPWM module is $n$ bits, and the module is implemented with $m$-*bit* counter and $(n-m)$-*bit* delay line.

To improve the final regulation linearity effectively, the total control delay of the delay line structure should be accurately adjusted. As shown in Fig. 3, in the proposed DPWM module, the total control delay of the delay line structure is adjusted based on the digital delay locked loop controller, which consists of the shift register and logic reorganization. Meanwhile, the traditional delay cell in the delay line structure is replaced by the programmable delay unit (PDU) to improve the regulation precision. The output signal rising edge of the $2^{(n-m)}th$ in the delay line structure is supposed as the detecting signal to detect the input clock signal,


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

and the total delay through the delay line should be equal to one clock period of the input clock. When the high level signal is detected, the total delay should be reduced, otherwise when the low level signal is detected, the total delay should be improved. The final regulation process is implemented by the shift of the *control_register* via the digital delay locked loop controller, to reduce the error between the total delay through the delay line and one clock period of the input clock and finally improve the regulation linearity of DPWM module.

## 3 Experimental results

A boost PFC converter with the proposed digital controller has been implemented via the FPGA platform. The parameters of the digital PFC converter are listed as follows: the input voltage range $v_{in} = 90$–$265$ V, the output voltage $v_o = 400$ V, the line frequency $f = 50$ Hz, and the rated output power $P_o = 300$ W. Meanwhile, the switching frequency $f_s = 100$ KHz, and the effective conversion resolution of the DPWM module is 9 bits. The proposed digital controller is coded with Verilog HDL and implemented via the FPGA platform.

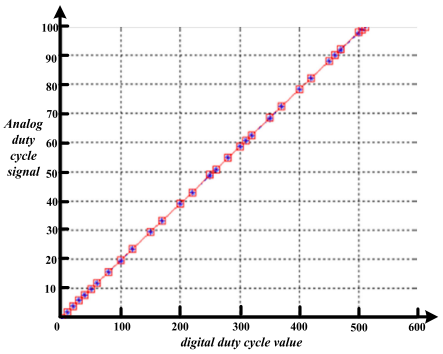


**Fig. 4.** The comparison between the ideal analog duty cycle signal and the measured analog duty cycle signal

The DPWM module is used to converter the digital duty cycle value to the analog duty cycle signal, so as to finally control the switching time of the the switch tube. The effective conversion resolution of the proposed DPWM module is 9 bits, so the conversion range is 0–511. The comparison between the ideal analog duty cycle signal and the measured analog duty cycle signal is shown in Fig. 4, the point as $*$ form in black is the ideal analog duty cycle signal and the point as $\square$ form in red is measured analog duty cycle signal. From the comparison, it can be observed that the deviation between the ideal analog duty cycle signal and the measured analog duty cycle signal is fairly slight, and the high regulation linearity can be aimed via the proposed DPWM module.

The output voltage, input voltage and input current waveforms under the full load are shown in Fig. 5. From the figure, it can be observed that the digital PFC converter can output the stable voltage and the input current can follow the input voltage perfectly. The reading of the voltmeter shows the power factor value is 0.99. The digital PFC converter with the proposed digital controller can achieve high power factor and well regulation stability.


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018

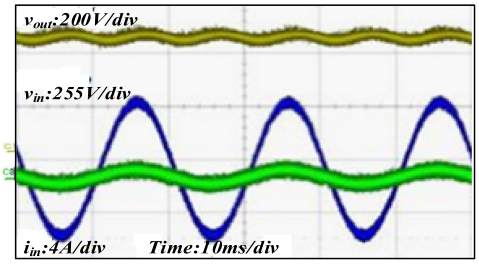


**Fig. 5.** Measured output voltage (channel 1), input voltage (channel 2) and input current (channel 3) waveforms under the full load

The performance comparison with previously reported works is shown in Table I, and the working conditions of the reported works are similar. From the table, it can be observed that the PFC converter with the proposed digital controller can aim high output stability and power factor.

**Table I.** Performance comparison

| | [9] | [10] | [11] | This Work |
|---|---|---|---|---|
| Input Voltage (VAC) | 220 | 110 | 230 | 220 |
| Output Voltage (V) | 400 | 375 | 392.5 | 400 |
| Output Power (W) | 300 | 250 | 300 | 300 |
| Switching Frequency (kHz) | 100 | 200 | 50 | 100 |
| Boost Inductor (mH) | 1 | 0.75 | 1.24 | 1 |
| Filter Capacitor (μF) | 1100 | 100 | 220 | 440 |
| Power Factor (Input Voltage/Power) | 0.975 (220 V/300 W) | 0.980 (110 V/250 W) | 0.985 (230 V/300 W) | 0.992 (220 V/300 W) |

## 4 Conclusions

This paper presents a novel digital controller for a single-phase boost PFC converter to reduce the harmonic distortion. The total digital control loop is simply implemented to improve the power factor and reduce the calculation burden. Meanwhile, the optimized DPWM module is adopted to improve the regulation performance of digital controller. The boost PFC converter with the proposed digital controller has been implemented via the FPGA platform, so as to verify the validity and effectiveness of the proposed digital controller, and experimental results indicate that the digital PFC converter with the proposed digital controller can aim high regulation linearity, power factor and output stability.

## Acknowledgements

The authors should like to thank the National Nature Science Foundation of China (61604075) and the Fundamental Research Funds for the Central Universities (30917012202).


DOI: 10.1587/elex.15.20171142
Received November 17, 2017
Accepted January 9, 2018
Publicized January 26, 2018
Copyedited February 25, 2018