Class AB flipped voltage follower with very low output resistance and no additional power

Ivan Padilla-Cantoya[1a)], **Jesus E. Molinar-Solis**[2], **and Jaime Ramirez-Angulo**[3]

[1] *Departamento de Electronica, Sistemas e Informatica DESI, Instituto Tecnologico y de Estudios Superiores de Occidente ITESO,*

Periférico Sur Manuel Gómez Morín No. 8585 Tlaquepaque, Jalisco, Mexico

[2] *Instituto Tecnologico de Ciudad Guzman ITCG,*

Avenida Tecnologico 100, Ciudad Guzman, Jalisco Mexico

[3] *Electrical and Computer Engineering Department, New Mexico State University,*

Las Cruces NM U.S.A.

a) *ivapadil@iteso.mx*

Abstract: A modified version of the flipped voltage follower (FVF) with class AB operation and very low output resistance is presented. Instead of passing one of the large bidirectional output currents through the voltage following transistor, which considerably degrades the output resistance as in other variations, the proposed circuit maintains a constant current in this device and, hence, a very low output resistance. Complementary-type output transistors that depend on the same signal give the circuit the ability to provide large bidirectional currents at high frequency. The implementation only requires an additional resistor and one connection change, with no additional power consumption. Simulation and experimental results of the fabricated circuit in a $0.5\,\mu m$ technology show an output resistance of the proposed circuit of $12\,\Omega$, with an enhancing factor of 60 with respect to previously reported variations.

Keywords: analog integrated circuits, CMOS integrated circuits, amplifiers, low-voltage low power design

Classification: Integrated circuits

References

[1] R. G. Carvajal, *et al.*: "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," IEEE Trans. Circuits Syst. I, Reg. Papers **52** (2005) 1276 (DOI: 10.1109/TCSI.2005.851387).

[2] I. Padilla-Cantoya and P. M. Furth: "High performance voltage follower with very low output resistance for WTA applications," IEICE Electron. Express **11** (2014) 20140629 (DOI: 10.1587/elex.11.20140629).

[3] I. Padilla-Cantoya, *et al.*: "Low-voltage differential voltage follower for WTA and fully differential applications," IEICE Electron. Express **9** (2012) 491 (DOI: 10.1587/elex.9.491).

[4] A. Saberkari, *et al.*: "A low voltage highly linear CMOS up conversion mixer based on current conveyor," IEICE Electron. Express **6** (2009) 930 (DOI: 10.1587/elex.6.930).

[5] M. R. Valero, *et al.*: "Rail to rail CMOS complementary input stage with only one active differential pair at a time," IEICE Electron. Express **11** (2014) 20140392 (DOI: 10.1587/elex.11.20140392).

[6] S. Mizuno, *et al.*: "Bandwidth enhancement technique for TIA using flipped voltage follower," IEICE Electron. Express **14** (2017) 20170310 (DOI: 10.1587/elex.14.20170310).

[7] I. Padilla-Cantoya, *et al.*: "Class AB low-voltage CMOS voltage follower," IEEE Midwest Symposium on Circuits and Systems MWSCAS'07 (2007) 887 (DOI: 10.1109/MWSCAS.2007.4488713).

[8] J. Ramirez-Angulo, *et al.*: "Simple class-AB voltage follower with slew rate and bandwidth enhancement and no extra static power or supply requirements," Electron. Lett. **42** (2006) 784 (DOI: 10.1049/el:20060617).

[9] J. E. Molinar-Solis, *et al.*: "Free class-AB flipped voltage follower using bulk-driven technique," Electron. Lett. **51** (2015) 1411 (DOI: 10.1049/el.2015.0768).

[10] J. Ramirez-Angulo, *et al.*: "Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities," IEEE Midwest Symposium on Circuits and Systems MWSCAS'05 (2005) 1151 (DOI: 10.1109/MWSCAS.2005.1594310).

1 Introduction

Over the last few years high performance voltage followers with attractive features have been proposed. Some of these followers are based on the commonly known Flipped Voltage Follower (FVF) [1], which offers very low output resistance. Designers have used this practical building block to enhance the operation of numerous implementations comprising Winner-Take-All (WTA) circuits [2, 3], current conveyors (CCII) for mixers [4], rail-to-rail differential amplifiers [5], and transimpedance amplifiers [6]. The schematic of the FVF is shown in Fig. 1a, and it offers two main advantages:

- <u>Large sinking current</u>: the shunt feedback permits node '*x*' to adjust its voltage level and, thus, the gate-source voltage of M1 for it to be able to sink large currents.

- <u>Very low output resistance</u>: the output voltage mainly depends on the input signal; M2 has a constant biasing current I_B and hence, a constant gate-source voltage –neglecting body effect,- thus reflecting the input voltage at the output node level shifted by V_{GS2} and operating as a voltage following device, where V_{GS2} is the gate-source voltage of M2. Voltage variations at node '*x*', due to current sinking by M1, are also reflected at the output node; however, these are attenuated by transistor M2 by a factor $g_{m2}r_{o2}$, thus offering a very low output resistance of $\approx 1/g_{m1}g_{m2}r_{o2}$, which ranges around a few tens of ohms. Here, g_{m1}, g_{m2}, and r_{o2} are the transconductance gain of M1 and M2, and the drain resistance of M2, respectively.

Unfortunately, the current-sourcing capability of the circuit is limited to I_B, when M1 turns off, making it a Class A circuit. Several class AB variations have been proposed; some of them include additional devices to provide large sourcing currents, such as transistors in parallel with M1 [1], or additional feedback loops

[7]. Unfortunately, these implementations result in asymmetrical current sourcing/ sinking capability and slew rates. Others use the voltage variations at node '*x*' to provide both sourcing and sinking currents, which gives the circuit symmetric operation.
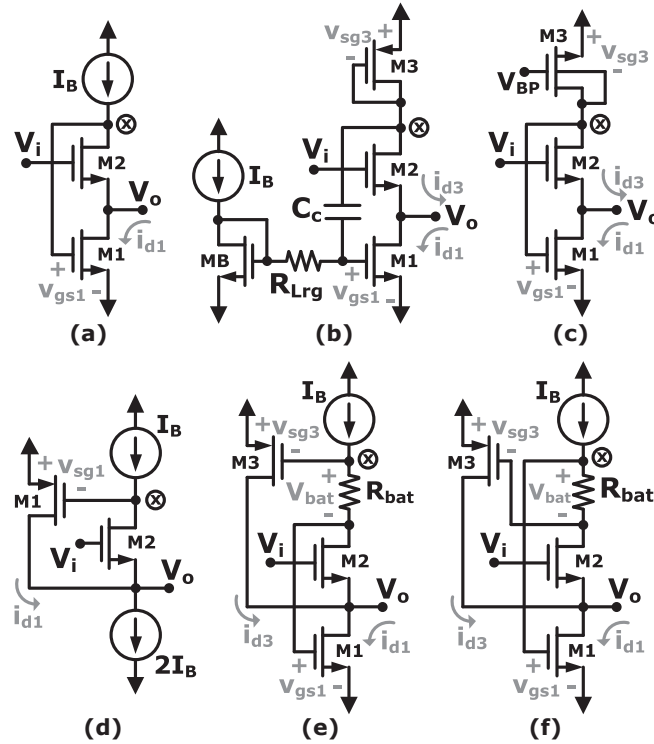

Fig. 1. Classification of voltage followers: a) Flipped Voltage Follower (FVF) [1], class AB modification of FVF using b) a floating battery [8], and c) a bulk-driven technique [9]. Also shown is d) the Folded FVF (FFVF) [10], e) the proposed class AB version with very low output resistance, and f) the proposed low-voltage version.

Fig. 1b shows the floating-gate technique reported in [8]. Capacitor *C* is included in the shunt feedback loop and operates as a floating battery of value V_{bat}, which has the ability to swing up and down to adjust the gate-source voltages of M1 and M3 complementary to provide large sourcing/sinking currents as required at the output. The large resistor R_{Lrg}, typically a transistor in cutoff or subthreshold region, impedes the capacitor to charge/discharge rapidly and maintains the value V_{bat}. Unfortunately, it does not offer class AB operation at frequencies below $1/R_{Lrg}C$. Fig. 1c shows a bulk-driven technique proposed in [9], where the transistor M3, conventionally used as the current source, has its bulk terminal connected to node '*x*'. Variations at this node change the source-bulk voltage of this transistor, V_{SB3}, which gives the ability to provide large sourcing currents at the output. However, the supply voltage is limited as large values of V_{SB3} result in excessive static currents and power consumption. Even though they offer large sourcing/sinking output currents, these two approaches have a common drawback; the sourcing current passes through the voltage-following transistor M2. When the circuit is sourcing large currents the output voltage is affected not only by

the input signal, but also by the gate-source voltage variations of M2. This results in a degraded output resistance of $\approx 1/g_{m2}$. In their respective references, only the immediate response of these techniques using a square input signal is reported; although a sustained behavior is also of interest.

2 Proposed class AB flipped voltage follower

The modified version of the FVF that provides large currents in the opposite direction is shown in Fig. 1d, denominated Folded Flipped Voltage Follower (FFVF) [10]. Here, M1 is replaced with its counter part, maintaining the gate and drain terminal connections –the source terminal is connected to the respective rail.– For a class AB implementation, these two topologies may be combined to allow large bidirectional currents. The proposed circuit is shown in Fig. 1e, where M1 (corresponding to the FVF) and M3 (corresponding to the FFVF) provide large sinking and sourcing currents respectively, whereas M2 remains as the voltage following device with a constant current. A resistor R_{bat} is included to induce the battery voltage V_{bat} between the gates of M1 and M3 in order to set their biasing point, according to the expression:

$$V_{Supply} = V_{SG3} + V_{bat} + V_{GS1} \qquad (1)$$

Where the battery voltage is defined as $V_{bat} = I_B R_{bat}$. It uses the same biasing current from M2, thus, it does not require additional power. V_{bat} operates as the battery conventionally used in class AB operation, giving complementary voltage variations to the gates of M1 and M3 and, therefore, their currents. Additionally, M2 maintains a constant current I_B and, hence, an output resistance of $\approx 1/g_{m1}g_{m2}r_{o2}$, contrary to the case of those in Fig. 1b and 1c. Note that it is similar to the FFVF, it only requires the addition of R_{bat}, and the shunt feedback of the gate of the transistor used as the lower current source. Observe that the proposed circuit operates with supply voltages of $V_{supply} > V_{SG3} + V_{GS1}$. However, it may be modified as shown in Fig. 1f to implement a negative value for V_{bat} so that $V_{supply} = V_{SG3} - V_{bat} + V_{GS1}$, making it suitable for low supply voltages. Additionally, note that the biasing current in M3 depends on R_{bat} and V_{supply}; therefore, mismatch values of R_{bat} due to fabrication process, or deviations in the supply voltage, might increase the current in this transistor and hence, the power consumption. This might be overcome by considering smaller values of I_B in M3 (i.e. $I_B/2$). Thus, one can design the circuit considering the deviations in the previous parameters to increase the current in M3 up to I_B, or decrease it down to ~ 0. In either case M3 is able to provide current if required.

DC operation: Under static conditions, M1 sinks the currents I_B and the drain current from M3, I_{D3}. This sets the gate-source voltage of M1, V_{GS1} which, level shifted by V_{bat}, defines V_{GS3} according to (1). Note that (1) may be rearranged as $V_{supply} = V_{DSsat3} + V_{bat} + V_{DSsat1} + V_{THN} + V_{THP}$, where the saturation voltages are $V_{DSsat1} = ((I_B + I_{D3})/K_1)$ and $V_{DSsat3} = ((I_{D3})/K_3)$; and constants K_1 and K_3 are $K_1 = (1/2)\mu_N C_{oxN}(W_1/L_1)$ and $K_3 = (1/2)\mu_P C_{oxP}(W_3/L_3)$. Considering these equations, currents I_B and I_{D3} may be selected to find the previous saturation voltages and, hence, find $R_{bat} = V_{bat}/I_B$.

Frequency analysis: Similar to all the other implementations, the shunt feedback loop of the proposed circuit requires frequency compensation to avoid oscillation. Referring to the open loop analysis described in [1], when opening the connection of gates of M1 and M3, and applying a testing voltage to both of them, we find the dominant pole at node 'x', and the first non-dominant pole at the output. Small signal analysis shows that the resistance at that node is defined as $R_o = (r_{o2} + R_B + R_{bat})/g_{m2}r_{o2} \approx 2/g_{m2}$ assuming $r_{o2} \approx R_B$ and $R_{bat} \ll (r_{o2}, R_B)$ where R_B is the drain resistance of the transistor used as the current source I_B. The resistance at node 'x' is given by $R_x = R_B \parallel (R_{bat} + g_{m2}r_{o2}(r_{o1} \parallel r_{o3}))$; as the resistance seen at the drain of M2 corresponds to a cascoding scheme, and much greater that R_{bat}, this relation results in $\approx R_B \parallel (g_{m2}r_{o2}(r_{o1} \parallel r_{o3}))$. The gain bandwidth product is given by:

$$GB = A_{OL}\omega_{px} = \frac{g_{m2}r_{o2}(g_{m1} + g_{m3})(r_{o1} \parallel r_{o3})}{C_x(RB \parallel (g_{m2}r_{o2}(r_{o1} \parallel r_{o3})))} \approx \frac{g_{m1} + g_{m3}}{C_x} \qquad (2)$$

The condition typically used to achieve enough phase margin to ensure stability is $2GB < \omega_{po}$, which in this case results in $C_x/C_L > 4(g_{m1} + g_{m3})/g_{m2}$, and can be easily achieved by adding a small compensating capacitor Cc at node 'x'.

3   Simulation and experimental results

The proposed and conventional circuits in Fig. 1 were simulated using Spectre, and fabricated in 0.5 μm C5N technology through MOSIS. The nominal threshold voltages are $V_{THN} = 0.7$ V and $V_{THP} = 0.9$ V, and the transistor sizes are 45/1.2 and 135/1.2 μm/μm for the NMOS and PMOS respectively. The circuits were tested with a supply voltage of $V_{DD} - V_{SS} = 2$ V and a biasing current of 50 μA, which results in a drain-source saturation voltage of 0.15 V. The proposed circuit in Fig. 1e was implemented with $I_{D3} = 35$ μA, resulting in $V_{DSsat1} = 0.2$ V and $V_{DSsat3} = 0.12$ V. These values, following the analysis in the DC operation section, result in $R_{bat} = 1.5$ kΩ. A compensating capacitor of $C_c = 1$ pF was connected to node 'x', considering a loading capacitor of $C_L = 15$ pF. All the signals applied at the input of the followers where mounted on a dc voltage offset of 1 V. Fig. 2 shows the simulation and experimental response of the proposed circuit in Fig. 1e for an input signal of $V_i = 250$ mV$_{pp}$ at 1 MHz. It shows simulated slew rates of $SR+ = 23$ V/μs and $SR- = 20$ V/μs, whereas it has experimental slew rates of $SR+ = 14$ V/μs and $SR- = 13$ V/μs; the difference is assumed to be due to parasitics in the setup.

Fig. 3 shows a comparison between the FVF, the FFVF, and the proposed circuit in Fig. 1e. A dc level shift was added intentionally for visualization purposes. An input signal $V_i = 200$ mV$_{pp}$ at 10 kHz was applied while driving a load resistor of $R_L = 300$ Ω. Note that the FVF and FFVF have limited response in one peak as they are bounded by the biasing current in the corresponding direction, whereas the proposed circuit is able to follow the input signal throughout the entire range, thus providing class AB operation. To test the output resistance, the input signal was kept at a dc voltage while bidirectional currents were applied at the output node in order to observe the voltage variations caused by these currents.
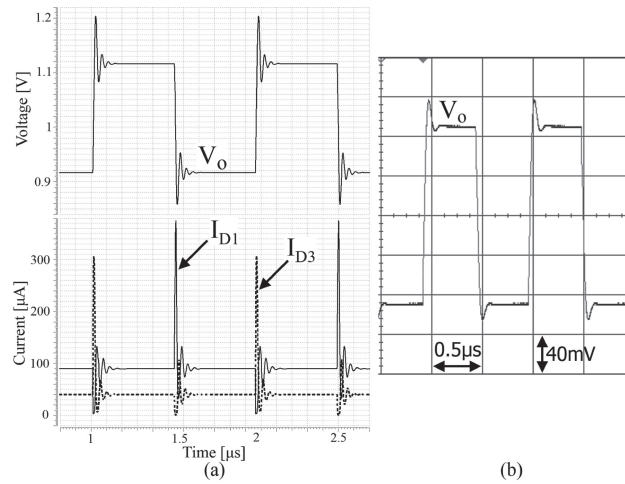
Fig. 2. a) Simulated transient response of the proposed circuit in Fig. 1e for $V_i = 250\,\text{mV}_{\text{pp}}$ at 1 MHz with $C_L = 15\,\text{pF}$, and b) experimental results where x-axis is $0.5\,\mu\text{s}$/div, y-axis is $40\,\text{mV}$/div.

Fig. 4 shows the output resistance of circuits in Fig. 1b, 1c and 1e for an applied current at the output from $-300\,\mu\text{A}$ to $300\,\mu\text{A}$ at 1 kHz. Circuits in Fig. 1b and 1c have large voltage variations of $0.7\,\text{V}$ showing an output resistance of $1.2\,\text{k}\Omega$, whereas the proposed circuit in Fig. 1e shows very small variations of only $12\,\text{mV}$, thus maintaining a very low resistance of $20\,\Omega$, offering an enhancing factor of 60.
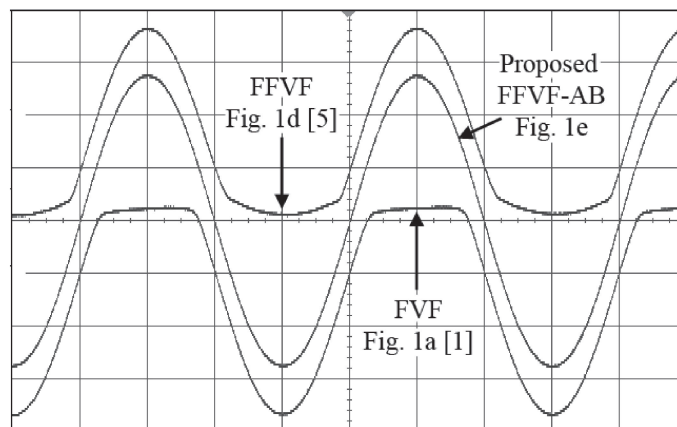

Fig. 3. Output voltage of the FVF, FFVF, and proposed circuits when driving a loading resistor of $300\,\Omega$ (x-axis = $25\,\mu\text{s}$/div, y-axis = $30\,\text{mV}$/div).

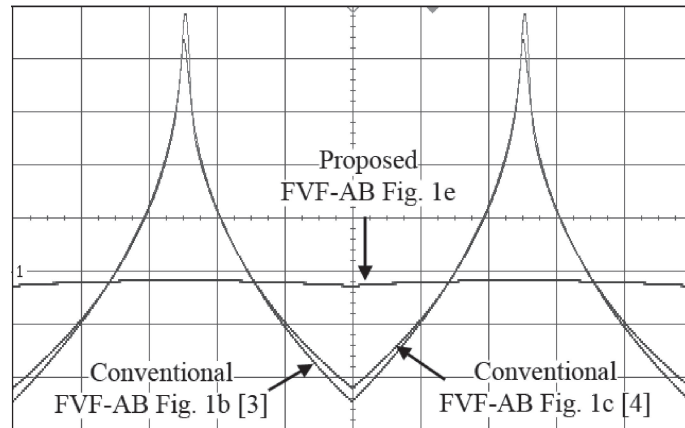**Fig. 4.** Output resistance of conventional and proposed circuits when applying a current at the output from −300 to 300 μA (x-axis = 100 mV/div, y-axis = 240 μA/div).

4 Conclusions

A simple modification of the conventional FFVF to provide class AB operation and maintain a low output resistance with one additional device and no additional power consumption was discussed. It was proven that Class AB operation is achieved with respect to the conventional versions FVF and FFVF, and that very low output resistance is maintained, contrary to the case of other class AB versions reported.