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A novel AGC scheme in a wideband receiver

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Abstract: A new automatic gain control (AGC) scheme in a wideband wireless receiver is presented in this paper. The proposed AGC scheme consists a receiver architecture with tuning the gain of RF amplifier, mixer and IF amplifier synchronously, and a novel exponential function current generator to achieve dB-linear gain control characteristic. Fabricated on a 0.18 um BiCMOS process, the proposed receiver provides a conversion gain dynamic range of 72 dB with the gain ripple of 5 dB that range from 0.8 to 2.7 GHz. At maximum gain operation, the noise figure of 9.9 dB and −25 dBm of third-order input intercept point are measured at 2.7 GHz. The chip draws 27 mW from a 1.8 V power supply and occupies an area of 2.8 mm^2.

Keywords: automatic gain control (AGC), receiver, dB-linear, wideband

Classification: Integrated circuits

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1 Introduction

The automatic gain control (AGC) is a key component in a wireless receiver. It adjusts the gain of the blocks in the signal path according to the input signal amplitude to avoid clipping distortion experienced by the baseband analogy-to-digital converters (ADC) [1]. As the demand for speed and bandwidth of communication system is increasing, the power consumption and data-rate of receivers become a bottleneck for the development of modern receiver. Traditional AGC scheme in receivers is implemented in programmable gain amplifier (PGA) [2], with applying power detector, ADC and digital processing in physical (PHY) layer to control the gain of PGAs [3, 4, 5]. However, PGAs have some drawbacks like requiring relatively large area overhead due to lots of switches as well as limited gain accuracy due to discrete and finite gain steps. But dB-linear gain control characteristic, which means that the gain in dB linearly follows the control voltage is a vital requisite to obtain a large dynamic range (DR) along with an independent settling time with respect to input signal power in AGC circuit [6].

In this paper, a new AGC scheme adopting a novel current regulator circuit is presented. Large DR and accurate gain control are both achieved in the scheme. In addition, the architecture of an *R*-2*R* attenuator network with multi-stage variable gain amplifiers (VGA) [7, 8] are performed in the design to achieve broadband response that frequencies range from 0.8 to 2.7 GHz [9]. The proposed AGC scheme is applied in RF VGA, Mixer and IF VGA, which means tuning the signal at RF frequency and IF frequency synchronously and optimizing the system signal-to-noise ratio (SNR) in an effective method.

The block diagram of the receiver is shown in Fig. 1. The remainder of this paper is organized as follows: In section 2, the AGC scheme in circuit design and analysis are described. Then in section 3, measurement results are presented and discussed. Finally, the results of this work are concluded in section 4.

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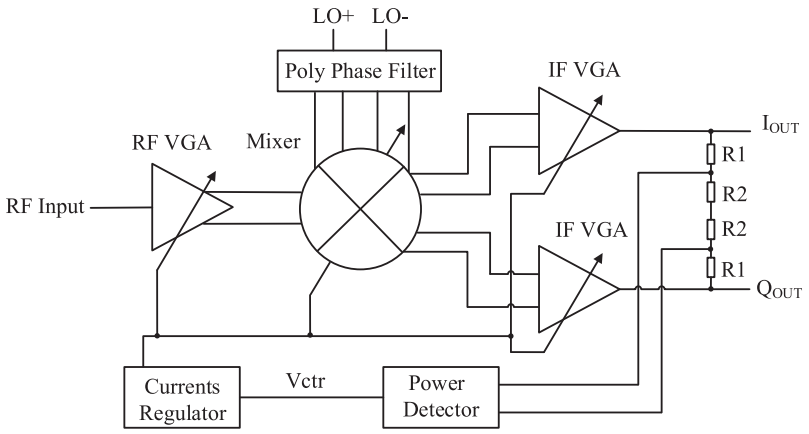

Fig. 1. AGC structure in a wireless receiver

2 AGC scheme in circuit design

2.1 Variable gain amplifier architecture

In order to achieve dB-linear gain control over a broadband frequency range, a wideband VGA architecture with an *R*-2*R* attenuator network combining a 5-stage VGA is proposed, whose gain is controlled by variable tail currents of the VGA. The architecture is applied in RF VGA, mixer and IF VGA synchronously.

The RF VGA architecture comprises a 5-stage parallel differential amplifier with one of the input being AC-grounded shown in Fig. 2(a), and a 5-stage *R*-2*R*

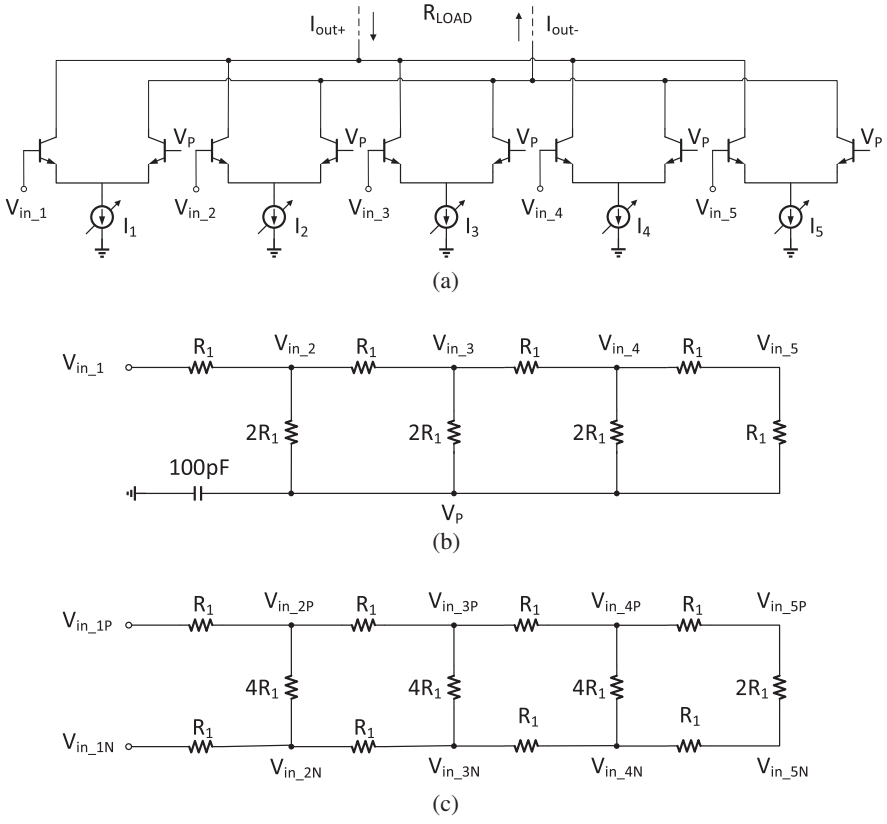

Fig. 2. (a) The architecture of RF VGA for single input.
(b) The input R-2R attenuator network for single input.
(c) The input R-2R attenuator network for differential input.

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attenuator network for single input shown in Fig. 2(b). The input *R*-2*R* attenuator network for differential input is shown in Fig. 2(c), which is applied in the cascade mixer and IF VGA. In Fig. 2(b) and Fig. 2(c), R_1 is set to 50 Ω. Thus, an equivalent resistor of 50 Ω for single input and 100 Ω for differential input is paralleled in each stage amplifier, which is independent of frequency and effective for wideband input matching. In the simulation, the input return loss of lower than −16 dB is achieved over the frequency range of 0.8 to 2.7 GHz. With the attenuation of *R*-2*R* attenuator network, the input signal for the n-stage amplifier is given by

$$v_{in\_n} = \frac{1}{2^{n-1}} \cdot v_{in\_1} \quad (n = 1 \sim 5) \tag{1}$$

Assuming the tail current and input signal voltage of the n-stage amplifier are I_n and v_{in_n}, the output current of the VGA can be expressed as

$$i_{out} = \sum_{n=1}^{5} \frac{v_{in\_n}}{V_T} \cdot I_n = \left(I_1 + \frac{I_2}{2} + \frac{I_3}{4} + \frac{I_4}{8} + \frac{I_5}{16} \right) \cdot \frac{1}{V_T} \cdot v_{in\_1} \tag{2}$$

Where V_T is the thermal voltage and can be expressed as

$$V_T = \frac{kT}{q} \approx 26\,\text{mV} \quad \text{at } 300°\text{K} \tag{3}$$

Thus, the gain of the RF VGA, related to the tail currents, can be expressed as equation (4), where R_{LOAD} is the load resistor.

$$G = \frac{v_{out}}{v_{in}} = \frac{R_{LOAD}}{V_T} \cdot \left(I_1 + \frac{I_2}{2} + \frac{I_3}{4} + \frac{I_4}{8} + \frac{I_5}{16} \right) \tag{4}$$

2.2 Current source regulator

A novel 5-stage current source regulator is proposed to provide tail currents for VGAs as shown in Fig. 3, which is the key component for dB-linear gain tuning. The tail currents are controlled by a DC voltage V_{ctr}. In this circuit, I_{ctr1} is equal to V_{ctr}/R_{ctr1}, and the sum of current I_{ctr1} and I_{ctr2} is 130 uA. The collector current I_C is set to 26 uA, and R_{ctr1} is set to 10 kΩ. Assuming V_n represent the DC voltage of point n (n = 1∼5), with linear superposition analysis, V_1, V_2, V_3, V_4 and V_5 are

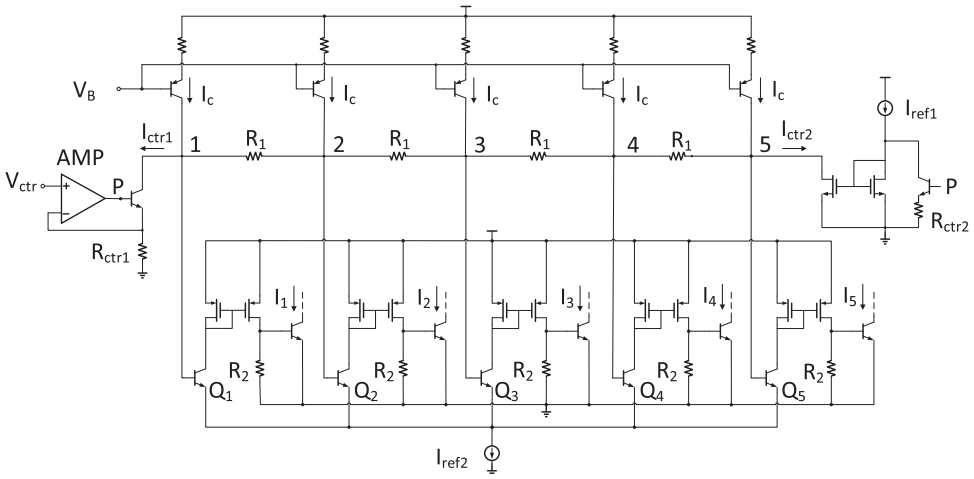

Fig. 3. The architecture of 5-stage current source regulator

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related to the variation voltage drop across resistor R_1 tuned by V_{ctr}. The voltage responses of point 1 to point 5 are shown in Fig. 4(a).

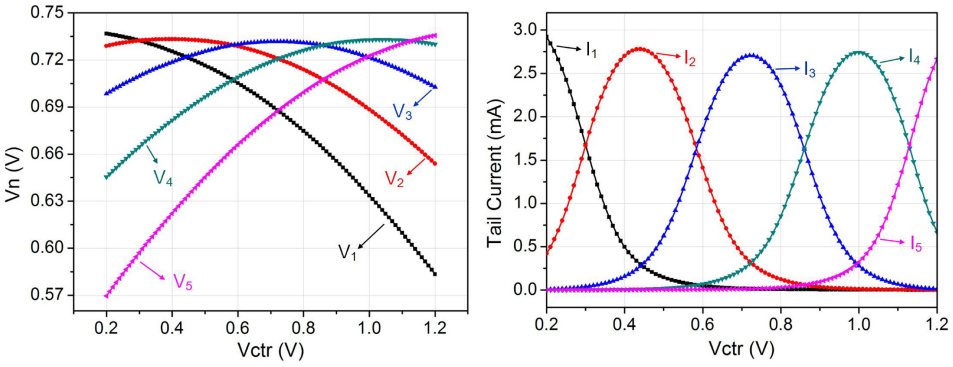

Fig. 4. (a) The DC voltage of points 1, 2, 3, 4 and 5 versus V_{ctr}. (b) The tail currents of RF VGA versus V_{ctr}.

With V_{ctr} tuning from 0.2 to 1.2 V, the current I_{ctr1} varies from 20 to 120 uA, and the maximum voltage among points 1 to 5 varies from point 1 to point 5 in sequence. When the point n is near to the maximum voltage, the gain of VGA is mainly determined by the n-stage amplifier in Fig. 2, and the tiny voltage variation of point n tuned by V_{ctr} can be expressed as

$$\Delta V_n = \frac{1}{2}\Delta V_{ctr} \cdot \frac{R_1}{R_{ctr1}} \tag{5}$$

For ΔV_n small enough, with reasonable approximation, the variation of the collector current of transistor Q_n can be expressed as (6). In (6), I_{cn0} represents the initial collector current of Q_n when ΔV_n is zero.

$$\Delta I_{cn} = I_{cn0} \cdot e^{\frac{\Delta V_n}{V_T}} \approx \frac{I_{cn0}}{V_T} \cdot \Delta V_n \tag{6}$$

Directly tuned by ΔI_{cn}, the tail current I_n can be expressed as equation (7), in which m is constant and determines the slop rate of dB-linear gain tuning.

$$\Delta I_n = I_{n0} \cdot e^{\frac{\Delta I_{cn} \cdot R_2}{V_T}} = I_{n0} \cdot e^{m \cdot \Delta V_{ctr}} \tag{7}$$

Thus, the voltage gain variation ΔG generated from ΔV_{ctr} can be expressed as (8), which is of dB-linear tuning characteristic.

$$\Delta G \approx \frac{R_{LOAD}}{V_T} \cdot \frac{\Delta I_n}{2^{n-1}} = K_n \cdot e^{m \cdot \Delta V_{ctr}} \tag{8}$$

The tail currents of RF VGA is shown in Fig. 4(b). As V_{ctr} tunes from 0.2 V to 1.2 V, the tail current I_n is tuned in exponentially, and the maximum current transfers from I_1 to I_n in sequence. Accordingly, the gain is determined by the amplifier ranging from the first-stage amplifier to the 5-stage amplifier in sequence. The gain dynamic range (DR) is about 24 dB, as shown in (9).

$$DR = 20\log(2^4) = 24\,\text{dB} \tag{9}$$

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2.3 AGC closed loop

The signal path of the receiver including RF VGA, Mixer and IF VGA, the gain of each stage is tuned synchronously with applying the same VGA architecture. The gain of RF VGA is in range −10 dB to 14 dB, the gain of mixer in range of −12 dB to 12 dB, and the gain of IF VGA in range of −10 dB to 14 dB. Thus, the total target gain of the receiver varies from −32 dB to 40 dB. In order to realize AGC function, a root mean square (RMS) power detector [10, 11] is applied in the design, which detects the amplitude of the IF signal and transforms it to a DC voltage. And then, the DC voltage can be switched to connect with the current source regulator V_{ctr} which tunes the gain of VGA blocks dynamically. Thus, the AGC closed loop is formed.

3 Measurement results

The microphotograph of the proposed receiver is shown in Fig. 5, which is fabricated in a 0.18 um Bi-CMOS process and occupies an area of 2.8 mm^2 including pads. The current consumption of the receiver is 15 mA with a 1.8 V power supply.

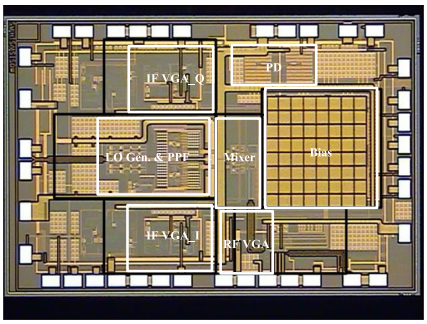

Fig. 5. The die micrograph of the receiver

The measurement results of the input return loss and the conversion gain are shown in Fig. 6(a) and Fig. 6(b) respectively. Over a wideband frequency range of 0.8~2.7 GHz, the S11 of better than −7 dB is measured. Due to the variation of the parasitic effect from package and the characteristic impedance of PCB transmission

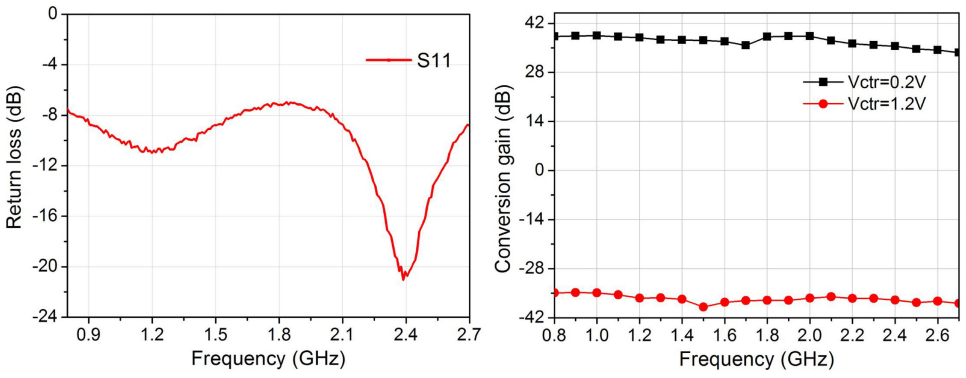

Fig. 6. (a) S11 of the receiver. (b) Conversion gain versus RF frequency.

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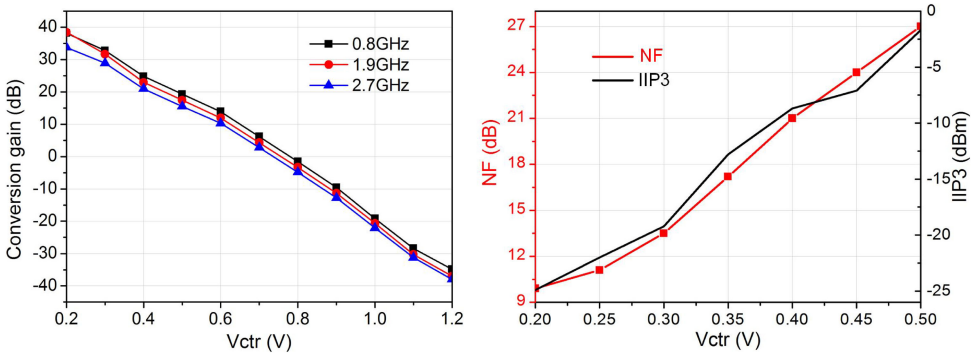
line, the input resistance is a little shift from 50 Ω and the measured S11 is a little worse than the simulated result. The maximum gain variation is 5 dB among the frequency range 0.8 to 2.7 GHz as shown in Fig. 6(b).

In Fig. 7(a), the conversion gain dynamic range of about 72 dB is shown. With tuning the gain control voltage V_{ctr}, the conversion gain at 0.8 GHz, 1.9 GHz, and 2.7 GHz are all plotted. From the figure, the experiment data has a good coherence to the mathematical analysis above. Compared with traditional PGAs, the gain in dB linearly follows the control voltage with little gain error, which is vital to keep along with the input signal power.



(a) (b)

Fig. 7. (a) Measured conversion gain versus V_{ctr}. (b) The NF and IIP3 versus V_{ctr}.

The measured noise figure (NF) and the input third-order intercept point (IIP3) are shown in Fig. 7(b). In the measurement, the LO signal is set to 2.7 GHz with amplitude of −5 dBm, and the two-tone frequencies are set to 2705 and 2706 MHz respectively in the IIP3 measurement. From the figure, the NF of 9.9 dB, and the IIP3 of −25 dBm are achieved. By tuning the gain control voltage V_{ctr}, the NF and IIP3 are tuned synchronously, and the signal to noise ratio (SNR) of the demodulated signal is optimized to satisfy the system requirement in an effective method.

4 Conclusion

In this letter, a novel AGC scheme in a wideband receiver is introduced. It is target for a wideband application with frequencies range from 0.8 to 2.7 GHz. The novel AGC scheme structure consists of an *R*-2*R* attenuator network, an exponential function current generator and a RMS power detector. Only analog circuits are used in circuit design. Larger than 72 dB conversion gain dynamic range and less than 10 dB NF at maximum gain are achieved at the whole band.

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