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An improved BIJM circuit based on undersampling technique

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Abstract: An improved BIJM (Built-in jitter measurement) circuit is presented in this paper, which is consisted of three improvement points. Firstly, multi-phase sampling technology improves the sampling efficiency based on the specially designed multi-phase clock generation circuit. Secondly, the median-edge alignment is used as the new jitter extraction method, which is taking the place of the mean-edge alignment. This method can filter low-frequency noise component to extract the cycle-to-cycle jitter. Thirdly, single-edge accumulation data processing method accumulates one edge in each cycle, blocking the correlation of adjacent sampling location, which can improve measurement accuracy and save the area overhead. The proposed jitter measurement circuit is designed at SMIC 40 nm CMOS process, and the circuit occupies a total silicon area of 9108 um^2. Post-layout simulation results show the measurement error is only 0.94%.

Keywords: jitter, multi-phase undersampling, mean-edge alignment, single-edge accumulation

Classification: Integrated circuits

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1 Introduction

With the development of semiconductor technology, the operating frequency of integrated circuits becomes higher and higher. PLL (Phase-Locked Loop) is one of the important modules in high speed communication system [1]. However the traditional testing methods have been unable to meet the test requirements, BIJM (Built-in jitter measurement) is becoming more and more important in the PLL testing [2, 3]. BIJM technology includes capacitor charging measurement circuit [4], vernier delay line (VDL) measurement circuit [5], time amplification measurement circuit [6], undersampling measurement circuit [7], and so on.

In various methods of on-chip jitter measurement, the undersampling technique is favored by the advantages of small PVT effect, high accuracy, and simple circuit. In literature [8], the undersampling method is demonstrated, which uses the same principle as the equivalent-time sampling oscilloscope in the jitter measurement. The paper [9] describes a PLL jitter test method based on the undersampling technique, which is developed from a SerDes undersampling DFT technique. This method is suitable for the high-frequency jitter. However, there are still some problems in the undersampling technology: the undersampling clock is very strict which should have no jitter in theory, the measurement accuracy is not high because of measurement resolution, the test time is long and the hardware cost of the undersampling data processing circuit is high.

The principle of jitter measurement technique based on undersampling is illustrated in Fig. 1. It uses a sampling clock signal f_s, whose frequency is the slightly offset from the PLL output signal's f_d. If undersampling clock's cycle time is Δt ps which is larger than the measured signal's, Δt is the measurement resolution and each undersampling clock sampling is Δt ps which is later than the previous sampling. Measurement resolution at the picosecond level can be achieved, if high precision of the sampling signal is provided. The jitter in the clock signal f_d, results in unstable bits in the Q_out. These unstable bits are defined as the transition regions, between stable 0 and stable 1. Therefore, by means of the statistical

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sampling output signal Q_out of the transition regions, jitter information of the signal f_d can be calculated.

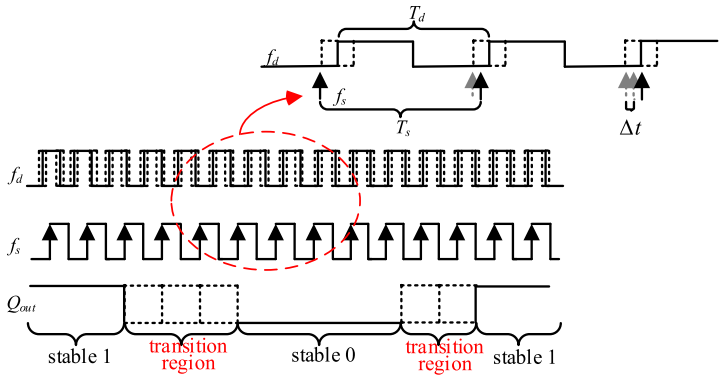

Fig. 1. The principle of jitter measurement technique based on undersampling

In this paper, a high accuracy and low cost measurement circuit is proposed, based on multi-phase undersampling, mean-edge aligned jitter extraction technique and single-edge accumulation data processing method. The paper is organized as follows. Multi-phase undersampling technique, the mean-edge aligned jitter extraction technique and the single-edge accumulation data processing method are described in section II. Section III introduces the novel jitter measurement circuit based on the proposed techniques. Section IV gives experimental results of the circuit which has been implemented with SMIC 40 nm technology. Finally, the paper is concluded in section V.

2 Improved undersampling techniques

2.1 Multi-phase undersampling

In traditional methods, there is a large number of sampling point not related to jitter (outside the transition region). In order to solve this problem, a multi-phase clock generation circuit is proposed, as shown in Fig. 2. The input signal in_CLK is decomposed into three signals with different phases through the multi-phase clock generation circuit.

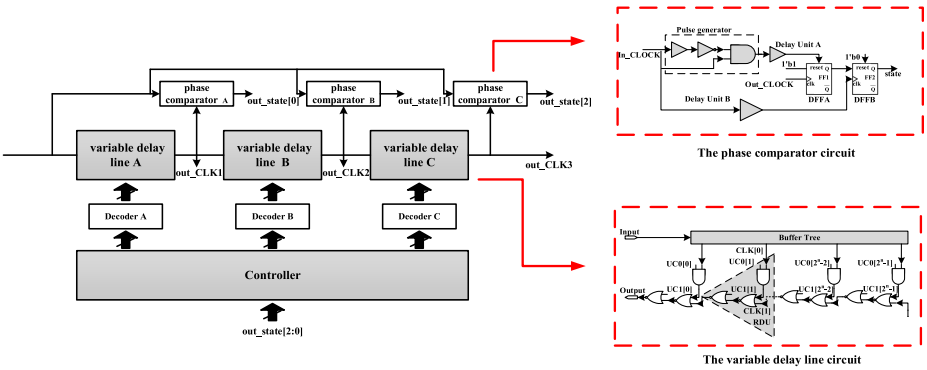

Fig. 2. Multi-phase clock generation circuit

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Multi-phase clock generation circuit is consisted of variable delay line circuit [10], decoder, phase comparator (PC), controllers, etc. The input signal in_CLK is decomposed four different phase signals (out_CLK1, out_CLK2, out_CLK3) through the variable delay line A, variable delay line B, variable delay line C, respectively. Each output of the variable delay line is compared with in_CLK by the phase comparator, obtaining the phase comparison results, out_state[2:0]. The controller changes delay control code by phase comparison results. Different delay control code leads to different delay, which makes the signals in_CLK, out_CLK1, out_CLK2, and out_CKL3 have the phase incremental offset.

2.2 The mean-edge aligned jitter extraction

In order to increase the test accuracy and avoid the complicated mathematical calculation, an improved jitter extraction method based on traditional median-edge alignment is used in this paper, called mean-edge alignment.

Function b(n) is defined related to the position of the unstable bits. When the bit value is 1, b(n) = 1. When the bit value is 0, b(n) = −1. Then the probability density function of the transition region is expressed as Eq. (1):

$$F_{\text{trans}}(n) = \sum_{-J}^{J} b(n+i) \tag{1}$$

In order to guarantee the measurement range, the 2J bit transition register is selected, which is the maximum estimated number of the transition region bits. Thus calculating the mean edge of the transition region is transformed into solving F_trans (n) = 0. When F_trans (n) = 0, the number of the value 1 and value 0 is the same inside the transition region.

The flow chart of jitter extraction method with mean-edge alignment is shown in Fig. 3. The flow is comprised of four states, which are “Stable 0”, “0-1 transition”, “Stable 1” and “1-0 transition”. In the “Stable 1” and “1-0 transition”, the logical value 0 of the Q_out signal is counted by the state counter, and the logical value 1 of the Q_out signal is counted by the state counter in “Stable 0” and “0-1 transition”. The En_A is the enable signal and the Reset_A is the reset signal of counter. The signal out_A is output of the counter. “Stable 0” is the wait state, when the logical value of the sampled signal Q_out changes to 1, the algorithm turns to the “0-1 transition” state. When the count value is 2J, the circuit turns to the “Stable 1” state. The changes from “Stable 0” to “Stable 1” is a complete “0-1 transition” process.

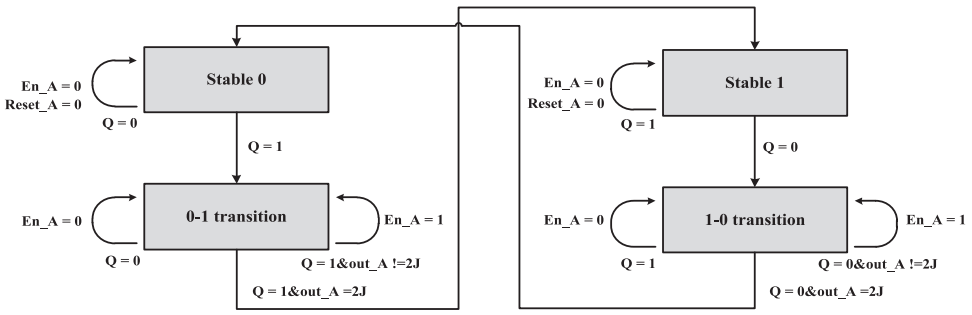

Fig. 3. The flow chart of mean-edge searching

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2.3 The single-edge accumulation data processing

The tradition method of accumulating transition region has two problems. If there are too many "1-0" states in "0-1" transition region, which may result in the value of the front column is higher than the value of the back column in the CDF (Cumulative Density Function) histogram. The other issue is that the number of the circuit area is determined by the number of the transition bits during the transition region.

To avoid these problems, a single-edge accumulation data processing method is proposed to accumulate one edge in each cycle. The traditional CDF synthesis process is shown in Fig. 4(a), and all the transitions in the transition region of the Q_out signal are accumulated simultaneously. After accumulating the unstable bits in one position, the value of the counter is shifted into the register group, the circuit measures the next position in the transition region in next cycle. As shown in Fig. 4(b), the counters record the data of the position① in transition region for N times (N is according to the test requirement). When the position① is recorded completely, the counters record the position② in the next cycle, and so on.

The proposed single-edge accumulation data process method blocks the correlation of adjacent sampling location to improve measurement accuracy, due to the adjacent counters record the unstable bits in non-adjacent cycle, which reduces low-frequency noise injection. What's more, the adjacent sampling locations are independent of each other, thus it's not necessary to prepare dedicated counter for each unstable position, and all the unstable positions share one counter, then reducing the area overhead. In addition, with the traditional method, in the worst case, all the counters would change value at the same time. With the proposed method, only one counter changes its value in one cycle, thus reducing the power consumption.

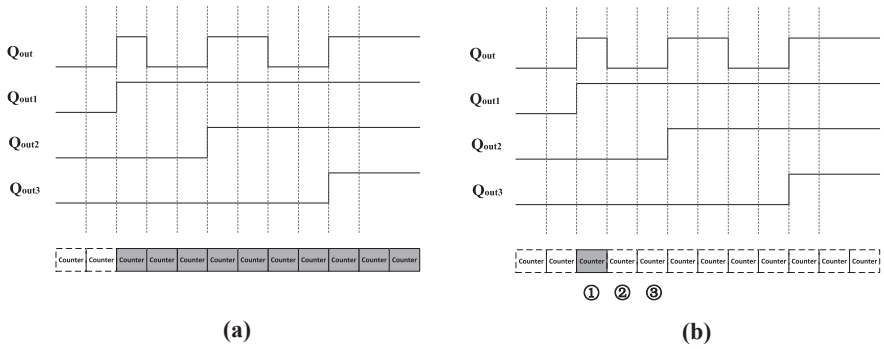

Fig. 4. (a) The traditional data process method (b) The proposed data process method

3 Proposed BIJM circuit

The architecture of the proposed jitter measurement circuit based on undersampling technology is shown in Fig. 5, including multi-phase clock generation circuit, sampler, shift register, jitter extraction circuit (JEC) based on the mean-edge alignment, data processing circuitry (DPC), register group, and JTAG circuit.

The working process of the circuit is as follows: The sampling clock F_s generates four different phase signal, F_s 0, F_s 1, F_s 2, F_s 3, after accessing

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multi-phase clock generation circuit. The signal F_d is sampled by the above four signals in the four arithmetic modules (CORE A, CORE B, CORE C, CORE D), respectively. The arithmetic module consists of sampler, shift register, JEC and DPC. The measured signal is sampled by the sampler, which is composed of register chains. Shift register is applied for storing the unstable bits in transition region. Jitter extraction circuit and data process circuit control the measurement process. Each arithmetic module processes the transition region with the mean-edge aligned method and the processed data is stored in the register group for synthesizing CDF function. The data in the register group is shifted out through JTAG serially for precise calculation with test equipment or computer.

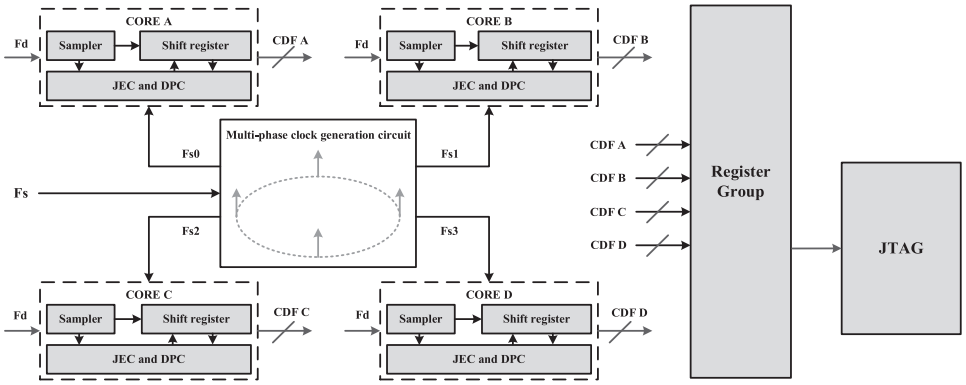

Fig. 5. The proposed jitter measurement circuit

4 Simulation results and analysis

In order to verify the performance of the measurement circuit, the circuit is designed in SMIC 40 nm CMOS process. The following section gives the simulation results.

Because the PLL does not match the actual environment in post-layout simulation, and the jitter generation technology is not concerned in the paper, the PLL model in MATLAB is used to generate the PLL clock and sample clock. The simulation result is indicated in Fig. 6. The jitter RMS value of the tested signal is 8.50 ps. The frequency of the tested signal is 600 MHz. The frequency of the sampling signal is 600.036 MHz. Thus the measurement resolution is 1 ps. After

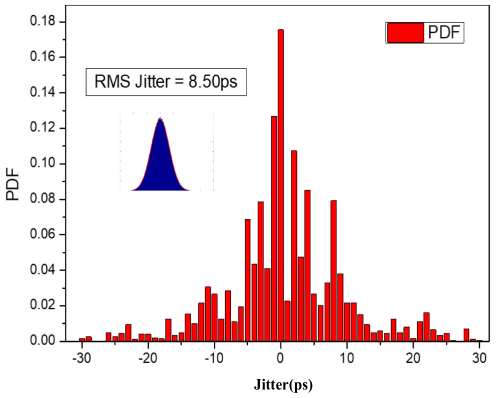

Fig. 6. The jitter measurement result in post-layout simulation

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measuring the 1000 transition regions, the simulated jitter RMS is 8.58 ps, and the test error is 0.94%. The PDF histogram of the jitter is depicted in Fig. 6.

In order to further analyze the circuit performance, the effects of different measurement resolutions on the measurement results are verified, as shown in Fig. 7. The tested signal at 600 MHz with 8.50 ps jitter is measured using the measurement resolution of 0.8 ps, 1.0 ps, 1.2 ps, 1.4 ps and 1.6 ps, respectively. It can be clearly seen that the measurement error can be kept at a low level within an appropriate range of measurement resolution.

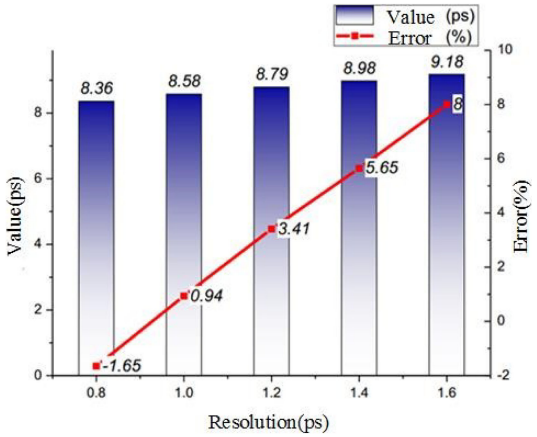

Fig. 7. The jitter measurement with different resolutions

Table I shows the performance comparisons of the proposed circuit with conventional BIJM design. The mean value of measurement error is less than 10%. At 600 MHz operating frequency, the circuit power consumption is 1.35 mw. Compared to the jitter measurement circuit using multi-phase sampling [11], the proposed circuit has the characteristics of small measurement error, small area overhead and low power consumption. However, the measurement time is long due to single-edge accumulation data processing method, which accumulates one edge in each cycle.

Table I. The comparisons between the proposed circuit and conventional BIJM design

	[11]	This work
Process	90 nm	SMIC 40 nm
Area (um^2)	26000	9108
Power (mw)	20.14	1.35@600 MHz
Test Condition	Chip test	Post-layout simulation
Measurement Time (ms)	/	100~1000 ms
Measure Error (%)	16%	<10%

5 Conclusion

In this paper, a novel jitter measurement circuit based on multi-phase undersampling, mean-edge aligned and single-edge accumulation is presented in this

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paper. Compared to the traditional circuits, simulation results indicate the proposed circuit can achieve high precision measurement requirement.

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