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# An efficient controlled LFSR hybrid BIST scheme

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**Abstract:** A new hybrid built-in self-test (BIST) test scheme is proposed. The test scheme consists of two components: the free LFSR mode (pseudo-random test) and the controlled LFSR mode (deterministic test). In order to improve the test quality of pseudo-random test sequence, a forward-backward pseudo-random test generation method is proposed. As every shifted-in bit is fully used to generate the most efficient test and the ratio of do not care bits is maximized in the remaining test pattern repository, the proposed controlled LFSR test generation method can find the targeted pattern with the minimal number of shift, efficiently embedding the deterministic test set into test-per-clock stream. Simulation results demonstrate that the proposed method considering for layout constraints shows great advantages in test data storage and test application time compared with previous methods.

**Keywords:** built-in self-test (BIST), hybrid test, test generation

**Classification:** Integrated circuits

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## 1 Introduction

Effective testing for guaranteeing the reliability of integrated circuit (IC) is particularly important. According to the difference in the test pattern generation, IC testing can be classified into three categories: the pseudo-random testing, the deterministic testing and the hybrid testing. The pseudo-random testing such as linear feedback shift register (LFSR) can well reduce test storage costs, but often fails to reach the satisfactory fault coverage. Conversely, the deterministic testing provide high fault coverage in exchange of large hardware overhead. The hybrid testing makes good use of the advantages of the former two, which usually compensates the irrelevant pseudo-random test sequences by deterministic test storage or logic hardware, such as weighted pseudo-random test, LFSR reseeding test, control bit-assisted test and so on. [1] proposed a weighted pseudo-random test, which effectively improve the efficiency of LFSR by changing the ratio of 0 and 1 of LFSR's output. However, the main drawback is that it only suits for small-scale circuit testing. Another technique to achieve high fault coverage and low test storage is the LFSR reseeding method [2, 3], where LFSR seeds stored in the ROM are serially loaded into the LFSR and decompressed to the deterministic test patterns. In [4], the control bits are used to skip the irrelevant pseudo-random test patterns. In [5], a scanning disabling technique is proposed to control the loading of pseudo-random scan slices. [4] and [5] both achieved a high test data compression rates by storing control signals rather than test sets. However, those all do not make full use of the test data bits stream during the test application.

On the other hand, while in test-per-scan based test schemes, test generator has to serially fill the scan-chain before launching a test pattern. With the test data volume increasing, the drawback of long test application time is exposed in test-per-scan scheme. Test-per-clock testing is getting more and more attention. In this scheme, test pattern is applied and its response is captured every test clock cycle. [6] proposed a circular self-test path (CSTP) method for test-per-clock test. [7] proposed an accumulator-based test-per-clock test generation. However, because of the existence of pseudo-random pattern resistant faults, it is difficult to achieve a satisfactory fault coverage in a limited cycling. [8] achieves test-per-clock test without data storage by adopting LFSR reseeding and test point insertion. [9] proposed a efficiently deterministic test-per-clock test using LFSR-reseeding and


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TVAC technologies. However, the implementation of test points insertion and TVAC is too complex. In this paper, a new efficient test-per-clock test generation for LFSR-ROM hybrid BIST structure with an appropriate test application time, low test storage, and a minimal routing overhead is proposed. First, the LFSR generates pseudo-random test for easy-to-detect faults. A forward-backward pseudo-random test generation method is proposed to effectively improve the pseudo-random test quality and limit the pseudo-random test sequence length. Then a controlled LFSR method is proposed to generate deterministic test for the rest fault detection, which effectively embeds the rest test set into test-per-clock stream. Instead of searching a targeted pattern from a compacted test set, a fully unspecified pattern for each undetected fault constitute the original targeted set, greatly improving the possibility of pattern matching and accelerating the process of test generation.

## 2 Proposed hybrid-mode BIST architecture

The proposed BIST structure is shown in Fig. 1. The test structure is composed of a test pattern generator (TPG) and a response analyzer (RA). The TPG consists of a LFSR followed by all the internal flip-flops formed in serial scan chain and a ROM that stores the control bits. Considering for layout constraints, the feedback lines of the LFSR are only drawn from the additional flip-flop added at each primary input (PI). As shown in the figure, $\oplus$ denotes an XOR gate, and $h_i$ represents a feedback network. The LFSR plays two roles during the test: free pseudo-random mode (MUX's 0 inputs are selected) and controlled shift mode. The Counter records the length of the LFSR test sequence. After pseudo-random test, the MUX then selects the controlled bit stream to generate deterministic test patterns for the remaining faults. At each test clock, a new test pattern is generated and applied to the CUT. Test responses are captured and compacted by the RA.

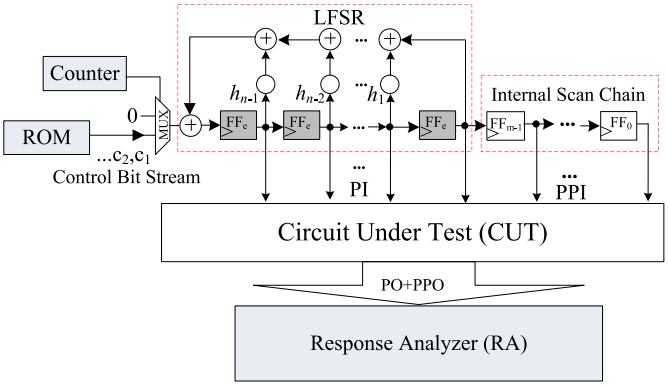


**Fig. 1.** Controlled shift BIST architecture.

## 3 Test generation

The test generation proposed in this paper consists of two parts: free LFSR pseudo-random test generation and controlled LFSR deterministic test generation.

### 3.1 Pseudo-random test generation

A forward-backward pseudo-random test generation method is proposed to determine the LFSR test sequence with an acceptable test sequence length. The


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algorithm is described as follows. First, a random pattern is selected as the initial state of the LFSR. Then, the LFSR runs to its next state obeyed to its characteristic polynomial, which is referred to forward pseudo-random test generation. To avoid generating a long redundant test sequence, a user-defined parameter $K$ is provided. When the number of consecutive redundant patterns that detect no new fault exceeds the limitation $K$, the forward pseudo-random test generation is ended. Next, the backward pseudo-random test generation starts form the initial state of the LFSR and runs to its prior state. Similarly, the algorithm is finished if the number of backward consecutive redundant patterns exceeds $K$.

### 3.2 Deterministic test generation

The analysis of he proposed test structure is shown as follows.

**Theorem 1.** *For an L-stage shifter(n-stage LFSR + m-stage internal scan chain as Fig. 1 shown), it will certainly be able to shift from the current state to any target state by applying $L'$ ($L' \leq L$) control bits.*

*Proof.* Supposed the the XOR network is cancelled, the proposed TPG work as a shift register, and the theorem holds. As $b = a \bigoplus c <=> c = a \bigoplus b$, by appropriately setting control bits, the feed-back values from LFSR-stages can be cancelled. □

Now, let's analyze this issue from another angle. Assuming that the current pattern $A$ in the shift register is randomly full specified (0 or 1 for each bit), and the probability that each bit of the target pattern $B$ is $X$ (do not care bit) is $\lambda$ ($0 \leq \lambda \leq 1$). The probability that the pattern $A$ matches $B$ is:

$$P_0 = \left(\lambda \times 1 + (1-\lambda) \times \frac{1}{2}\right)^L \tag{1}$$

The control bit shifted in each test clock can be regarded as $X$. After $L'$ clock cycles, the pattern in the shift register is $\{X_{L'} \ldots X_1, a_{n-1}, a_{n-2} \ldots a_{L'}\}$. Now, the probability that the pattern matches the target pattern $B$ is:

$$P_{L'} = \left(\frac{1+\lambda}{2}\right)^{L-L'} \tag{2}$$

As we know, $P_{L'}$ is positive growth with $\lambda$ and reverse growth with $(L - L')$. In order to obtain a short control shift time $L'$, we need a big $\lambda$ and a small $L$.

The flow of deterministic test generation algorithm proposed in this paper is shown as follows. After the pseudo-random test generation, the remaining fault list $F$ is obtained. To maximize the value of $\lambda$, one test pattern with the maximum number of $X$s is generated for each remaining fault. These patterns constitute the original targeted test pattern repository *ORG_T*. We use an improved ATALANTA as the test generation tool. The algorithm is divided into three steps.

Step 1 is shifting and pattern matching. For each test clock, one control bit shifted in the shift register is regarded as a temporary $X$, and the new current pattern is added to the new test set $T$. The current pattern then try to find the compatible pattern in the *ORG_T*. When there is no compatible pattern in the *ORG_T*, the shift continues. If there is more than one compatible pattern, the selection strategy is the pattern which has the smallest $\lambda$. As mentioned above, the pattern with higher value


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of $\lambda$ will be easier to be matched, so easy-to-match patterns left will increase the probability of subsequent pattern matching.

Step 2 is the process of solving control bits and pattern updating. The control bit $X$ is solved according to the matched pattern in $ORG\_T$, and the related patterns which contains the $X$ in the new test set $T$ also need to be updated. In order to speed up the fault detection, when the last bit of the pattern is $X$, it needs to be specified with random value and update its related patterns.

Step 3 is the process of fault simulation. Each new pattern in test set $T$ is simulated. When a fault is detected, it is deleted from the fault list $F$ and its corresponding pattern is deleted from the test repository $ORG\_T$. When the fault list $F$ is empty, the algorithm ends; otherwise, it continues to step 1.

Compared to previous methods, the main difference is that in the proposed method every shifted-in bit is tried to generate the most efficient test for the remaining faults, which makes full use of test bit stream. The time complexity of the proposed algorithm is $O(L^2 \times NoF^2)$, where $L$ denotes the number of stages of the shift register and $NoF$ denotes the number of faults remained, respectively.

## 4 Simulation results

In this section, we evaluate the effectiveness of the proposed method for the larger ISCAS89 benchmark circuits.

Table I shows the simulation results for stuck-at fault test generation (mean values of 10 times) and the comparisons with previous methods. The first two columns give the circuit name, the number of PI (the width of LFSR). The third column gives the value of the suggested limitation $K$ for each circuit, which is initialized to 0 and limited to 500, and incremented by 50 for each attempt time. The final value of $K$ takes the optimum in all the cases, which has an appropriate test length and a less control bits storage. Column "TAT/ROM" shows the total TAT and the number of the control bits of the proposed method, respectively. For each circuit, the fault efficiency has reached 100%. The fault efficiencies of the proposed forward-backward pseudo-random test set and the conventional unidirectional pseudo-random test patterns under the same conditions (the same number of test patterns and the same characteristic polynomial) are shown in the fifth and sixth column respectively. The following columns show the comparisons in TAT and test data storage with other methods, including LFSR reseeding method based on test-per-scan [2] (variation-R model), LFSR reseeding method based on test-per-clock [3], scan slices blocking method based on multiple scan chains [5]. The last row shows the average reductions in TAT and test data storage compared to other methods.

It can be seen that the forward-backward pseudo-random test is superior to conventional unidirectional pseudo-random test in fault coverage. As the ratio of do not care bits is maximized in the remaining test repository, the deterministic test algorithm can more effectively use the controlled bits to construct test pattern. Compared with the other methods, the proposed test method has significantly improvements in reductions of test storage and test application time.


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**Table I.** Results for comparisons with previous methods

| Circuits | PI | *K* | TAT/ ROM | R_FC | CR_FC | [2] TAT/ ROM | [3] TAT/ ROM | [5] TAT/ ROM |
|---|---|---|---|---|---|---|---|---|
| s5378 | 35 | 250 | 5290/ 720 | 98.7% | 98.3% | 13182/ 5040 | 11808/ 1935 | 11014 |
| s9234 | 36 | 300 | 13547/ 7039 | 89.5% | 88.7% | 19957/ 7931 | 21731/ 6696 | 20543 |
| s13207 | 31 | 250 | 8164/ 2857 | 92.4% | 89.3% | 47600/ 7723 | 8550/ 3505 | 16472 |
| s15850 | 14 | 250 | 8108/ 3761 | 93.5% | 92.3% | 45947/ 9423 | 12180/ 5508 | 17739 |
| s35932 | 35 | 200 | 1720/0 | 100% | 99.6% | N/A | N/A | 1295 |
| s38417 | 28 | 200 | 22829/ 15645 | 93.2% | 91.7% | 210329/ 36884 | 34510/ 34965 | 96645 |
| s38584 | 12 | 300 | 9478/ 3920 | 98.2% | 97.1% | 139372/ 15622 | 8052/ 8790 | 25685 |
| Ave.Red | – | – | – | – | – | 73.67%*/ 58.97%* | 26.09%*/ 36.75%* | 55.83%/ 81.64% |

*Except the test data of S35932

## 5 Conclusions

In this paper, we propose a hybrid BIST test scheme for full scan circuit. In pseudo-random test, the proposed forward-backward pseudo-random test generation method searches the LFSR test sequence both for forward and backward, efficiently improving the test quality of the LFSR test sequence. In deterministic test, a controlled LFSR test generation algorithm is proposed. Instead of searching pattern from a predefined compacted test set, a fully unspecified pattern for each undetected fault constitutes the original targeted set, which improves the possibility of pattern matching. Meanwhile, every shifted-in bit is fully considered to generate the test, effectively embedding the deterministic test set into the test-per-clock stream. In addition, the width of LFSR only equals to the number of PIs of the CUT, deriving a minimal routing overhead. The hardware overhead of the implementation of TPG is also low. Since flip-flops added on primary-inputs are the same design as other test approaches, they can be ignored as additional hardware. The additional hardware of the TPG is only the feedback XOR network (3 XOR gates for all the experimental cases).

The drawback is that the proposed scheme needs to capture the responses in every test clock. Since the internal flip-flops are no longer used as response capturer, it leads to an expensive hardware for the implementation of RA. However, this can be alleviated by zero-aliasing space compactor and MISR as [10]. Moreover, when this method is applied to register transfer level (RTL) partitioning [11] or scan partitioning [12], the RA can be constructed by internal resources of the CUT. Therefore, this proposed test scheme can serve as a promising alternative to IC testing.

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