

An improved noise immune level-shifter via IGBT gate-emitter voltage detection

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Abstract: In this paper, a noise rejection circuit for level-shift gate drive ICs is proposed. This circuit is composed of a detection module and a pull down module with good process matching robustness and low circuit complexity. The dv/dt noise is removed by monitoring the interval of the IGBT gate-emitter voltage variation and locking the output logic in the period of the dv/dt noise comes. Spectre simulation has been performed with a 700 V 0.6 μ m BCD process model to verify the performance of the proposed noise rejection circuit which shows a full removal of 80 V/ns dv/dt noise and only 15 ns increasing in propagation delay time.

Keywords: dv/dt noise, gate drive IC, level shift

Classification: Power devices and circuits

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1 Introduction

IGBT gate drive integrated circuits (ICs) with level shifters have been widely used in high voltage power applications. The high voltage level shifters, which are the most important part of the IGBT gate drive ICs, are used for transmitting signals between the low voltage side and the high voltage side. Normally, a typical half bridge switching system is constitutive of pulse generation, LDMOS level shifter, pulse filter, RS flip-flop and output driver, as shown in Fig. 1. The high side floating ground VS always increases or decreases rapidly as the IGBT turn-on or turn-off. A rapid variation of the VS will cause noise problems such as malfunction for gate drive ICs. The dv/dt noise rejection circuits of gate drive ICs are mainly divided into two categories: (1) Pulse filter technique [1]: utilize a RC delay network to filter out dv/dt noise. To guarantee the gate drive ICs normal function, the pulse filter must not to filter out normal pulse signals. The wider the pulse width that can be filtered out by the pulse filter, the longer the propagation delay time is. The delay time of the pulse filter contributes the most to the total propagation delay time, so the biggest drawback of the pulse filter strategy is the considerable increase in propagation delay time. (2) Common-mode noise cancelling [2, 3, 4, 5]: the dv/dt noise of the double-pulse LDMOS level shifter circuit has the characteristics of common-mode signal, with the dv/dt noise on two transmission paths having same waveform and duration, while the normal signals on the two transmission paths are different. Normal and dv/dt noise signals can be correctly distinguished by their characteristics. However, the common-mode noise cancelling strategy is usually sensitive to the fabrication process mismatch, such as resistor mismatch or current mismatch caused by MOSFETs mismatch, etc. Therefore, the noise signal cannot be exactly the same, and it's impossible to remove the dv/dt noise completely [2].

In this paper, a noise-rejection circuit for the IGBT level-shift gate drive IC via gate voltage detection has been proposed which is composed of a detection module and a pull down module. This circuit has a small propagation delay time with a simple structure. The noise suppression principle of the proposed circuit is to sense the IGBT switching transient via the gate-emitter voltage by detection block. The IGBT switching transient is the dv/dt noise generation interval. The detection block will output a signal to control pull down block to latch the output logic. So the state of the RS flip-flop will not affect by the dv/dt noise. In section II, the noise generation process and its relationship with the VS are discussed. In section III, the

structure of the proposed noise-rejection circuit is introduced. In section IV, simulation results are given to verify the above structure and technique.

2 Dv/dt noise in IGBT gate drive ICs

Fig. 1 shows a conventional half bridge switching system with a level shifter which has been used in product IR2213 [1]. When the high side IGBT (Q1) is switched on, the VS voltage changes from zero to near the bus voltage HV. At this time, the dv/dt noise is generated by the voltage variation and applied to the high side region through the VS line. According to $I = C_{DS} * dv/dt$, the voltage variation induces displacement current through LDMOS parasitic capacitance C_{DS} , causing a voltage drop on resistor R1, R2, and leading to an RS flip-flop malfunction. For the Q1 turn-off transient, when the collector current falls to zero, an inductive load keeps a current flowing out from the VS, which will induce a negative dv/dt noise at the VS terminal [6, 7]. Once the amplitude of the negative dv/dt noise exceeds the tolerance, the gate drive IC would be damaged or the high-side output would be temporarily irresponsive to the input signal.

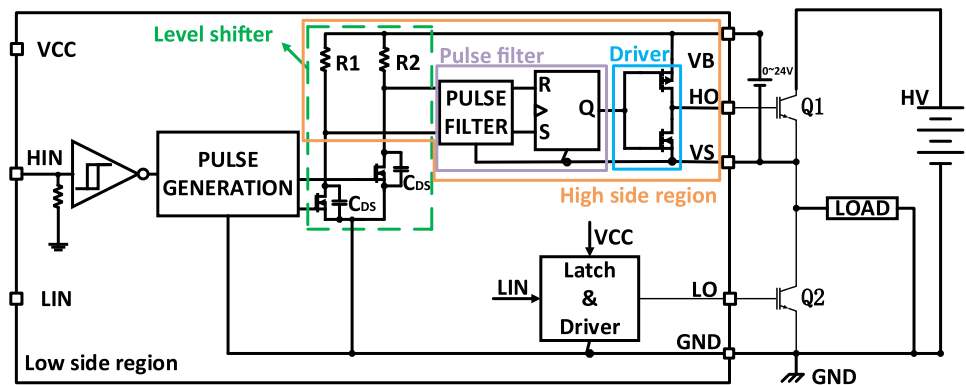


Fig. 1. Block diagram of the conventional half bridge switching system with level shifter.

3 Structure of the proposed noise rejection circuit

Fig. 2(a) are a kind of malfunction waveforms of a conventional circuit (Fig. 1). When a set signal arrives, the Vge rises up, the IGBT turns on, and the noise is generated at the rising edge of the VB. At the same time, the noise is identified by the subsequent logic circuits to form a narrow pulse signal. If the pulse filter fails to filter out the noise, the high side output of the gate drive IC (HO) would output incorrectly so that the IGBT would turn off by mistake. As the Fig. 2(a) shows, the red dash lines of the Vge and VB indicate the correct waveforms while the black lines indicate the incorrect waveforms.

Generally, the dv/dt noise is caused by VS variation, and the VS variation is within the IGBT turn-on transient and turn-off transient [8, 9, 10]. By monitoring the voltage between the IGBT gate node and emitter node, a noise rejection circuit can be designed to avoid malfunction by keeping the RS flip-flop input signal equals to the VS during IGBT's switching transient. Therefore, the outputs of the RS flip-flop remain the current state, which are not affected by the noise signal.

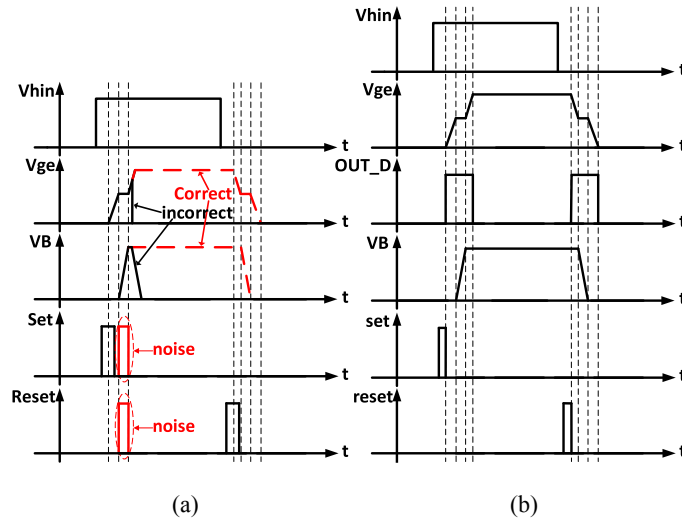


Fig. 2. (a) A kind of malfunction waveforms of a conventional circuit; (b) Waveforms of dv/dt rejection circuit.

The red sections in Fig. 3 show the block diagrams of the proposed double-pulse level shifter with the noise rejection circuit. The noise rejection circuit includes a detection module and a pull-down module. The detection module detects the duration of IGBT's turn-on and turn-off transients. During the IGBT's switching transient, the detection module outputs a high level "1", otherwise, it outputs a low level "0", as is shown in Fig. 2(b) OUT_D . When the output of the detection module is "1", the pull-down module will be activated to keep the RS flip-flop input at "0", and the output of the RS flip-flop will maintain its current state. Thus, the gate drive IC can avoid malfunction caused by dv/dt noise. When the output of the detection module is "0", the input of the RS flip-flop is not affected by the pull-down module, but only by outputs of the previous stage.

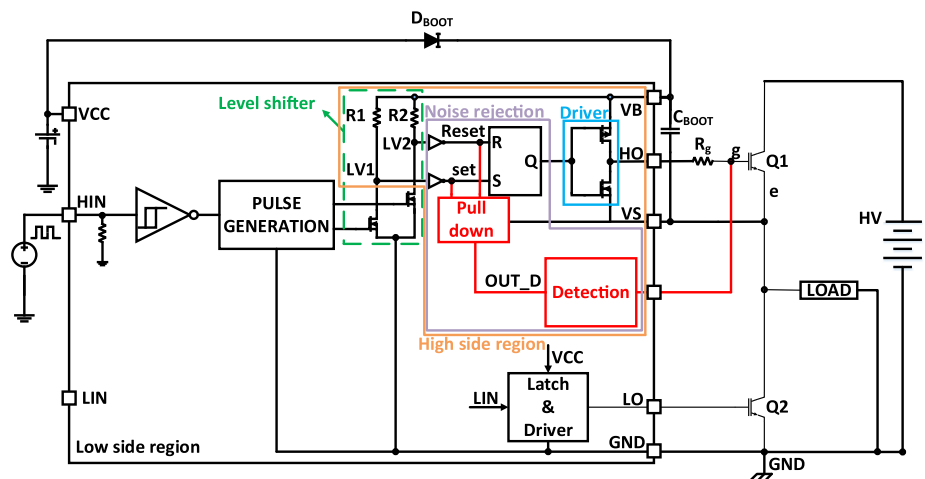


Fig. 3. Block diagram of the half bridge switching system with the proposed noise rejection circuit.

Fig. 4(a) shows the schematic of the detection module and Fig. 4(b) shows its output logic. This circuit has less propagation delay with the ability to detect variation of the V_{ge} in a few nanoseconds.

The main idea of the detection circuit is that only when a V_{ge} larger than $V_{TH,M2}$ and less than $V_B - V_{TH,M1}$, the detection module outputs a high level “1”. By choosing parameters of the MOSFETs and resistors properly, module 1 and module 2 will be activated once the V_{ge} gets to $V_{TH,M1,M2}$. At first, $V_{ge} = 0$, M1 is on, M2 is off, and j is low level. When V_{ge} rises up to the threshold voltage of M2, $V_{TH,M2}$, M1 is on, M2 turns on, and j turns to high level; when V_{ge} goes up higher than $V_B - V_{TH,M1}$, M1 is off, M2 is on, j is low level. Similarly, during the falling edge, when V_{ge} drops from $V_B - V_{TH,M1}$ to $V_{TH,M2}$, M1 and M2 are on, and the detection module outputs a high level. The threshold voltage of the MOSFET is smaller than the threshold of the IGBT, so the detection module can output a high level “1” before V_{ge} rising to $V_{ge(th)}$. This means that the detection module can pull down the inputs of the RS flip-flop before the onset of the dv/dt noise. Furthermore, the proposed detection module senses voltage variations of V_{ge} before I_c changes, thus the detection module won’t be affected by gate voltage oscillations [11]. Practically, there is a propagation delay, e.g. 22 ns, between the output of the RS flip-flop and the HO, so the logic of the RS flip-flop comes much earlier than HO. As a result, the method neither affects normal signal transmission nor increases in propagation delay.

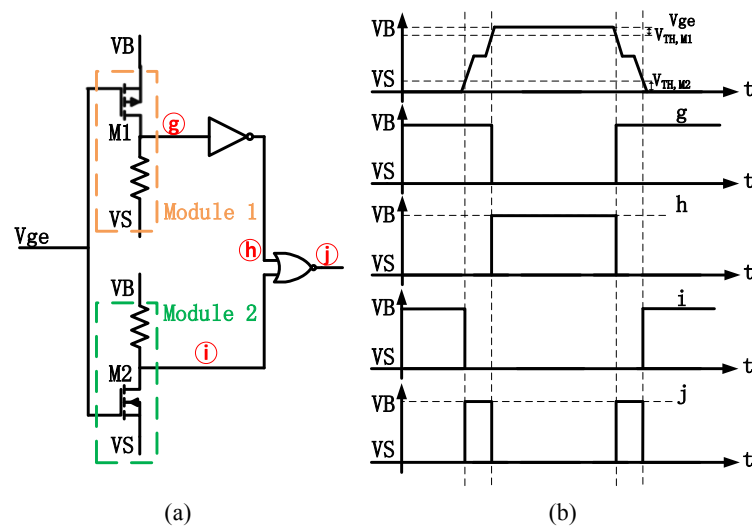
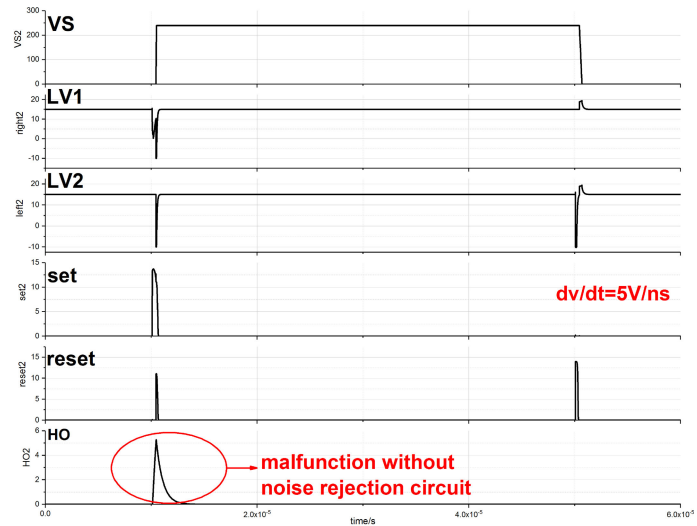


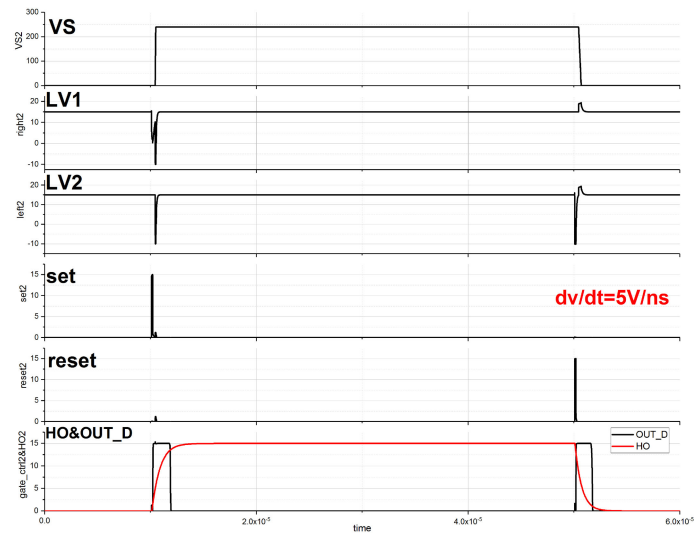
Fig. 4. (a) Block diagram of the detection module; (b) Waveforms of the detection module.

4 Dv/dt noise rejection simulation

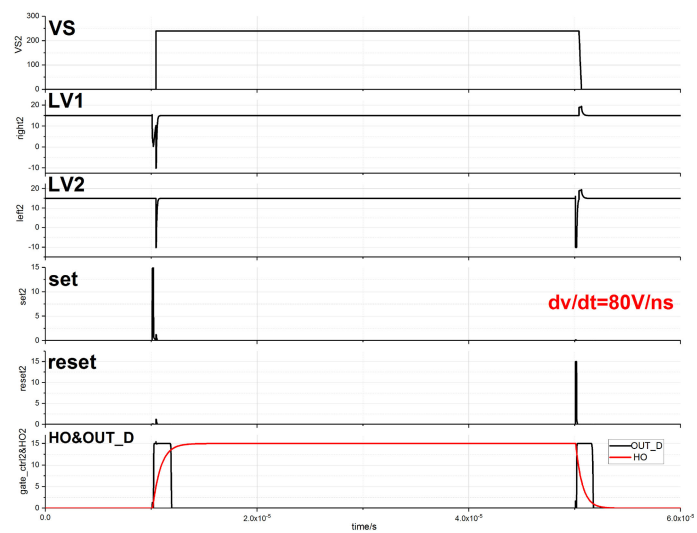
This gate drive IC with the noise rejection circuit is simulated by spectre based on the device model of 5 V/30 V/700 V BCD process. Fig. 5 shows the simulation waveforms of the double-pulse level shifter as the value of dv/dt varies from 5 V/ns to 80 V/ns. As is shown in Fig. 5(a), the gate drive IC without noise rejection circuit malfunctions caused by dv/dt noise. Meanwhile, it can be seen from Fig. 5(b) and (c), the HO and OUT_D follow the input signal correctly as the value of dv/dt varies from 5 V/ns to 80 V/ns which indicates the proposed noise rejection circuit has good noise rejection ability.



(a)



(b)



(c)

Fig. 5. (a) The gate drive IC without noise rejection circuit as $dv/dt = 5 V/ns$; (b) Noise rejection circuit as $dv/dt = 5 V/ns$; (c) Noise rejection circuit as $dv/dt = 80 V/ns$.

The interval from 50% of the input signal to 10% of the high-level output is defined as propagation delay. As shown in Fig. 6, The propagation delay of three different double-pulse level shift gate drive IC were compared as $dv/dt = 5 \text{ V/ns}$. The only difference between the three circuits is the noise rejection circuit. The first gate drive IC is without noise rejection circuit, the second one is with the pulse filter circuit and the third one is with the proposed noise rejection circuit. For the gate drive ICs with the pulse filter, filtering out 150 ns pulse width cause the propagation delay time of 343 ns, while the delay of the gate drive IC with the proposed circuit is 147.7 ns, which is approximate to 132.3 ns of the gate drive IC without noise rejection circuit. In other words, the proposed noise rejection circuit only results in a slightly increasing in propagation delay.

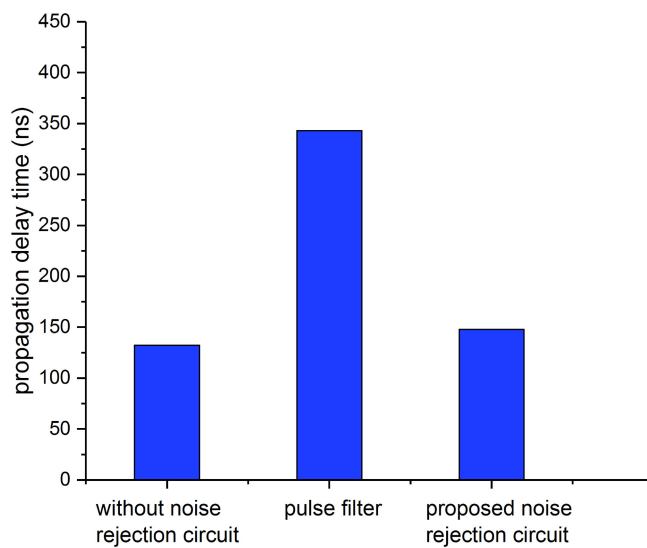


Fig. 6. Propagation delay comparison as $dv/dt = 5 \text{ V/ns}$.

5 Conclusion

In this paper, an improved noise immune level-shift gate drive IC is proposed and simulated. The noise rejection mechanism of the proposed circuit is active monitoring IGBT gate voltage switching transient and ensuring the RS flip-flop not be changed by the false signal generated by dv/dt noise during IGBT turn-on and turn-off transient. The performance of the proposed noise rejection circuit was simulated using a 700 V 0.6 μm BCD process model, which showed a strong noise immunity with value of the dv/dt up to 80 V/ns at the cost of a very small increase in propagation delay. Besides, the mechanism of the proposed noise rejection circuit makes this circuit structure not sensitive to the process mismatch. Therefore, the proposed noise rejection circuit can be applied to high voltage gate drive ICs with various process.