

Offset voltage suppressed sense amplifier with self-adaptive distribution transformation technique

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Abstract: An offset voltage suppressed sense amplifier (SA) with self-adaptive distribution transformation technique is proposed. By means of the peripheral assisted circuits, the offset voltage of the proposed SA will be automatically judged, and the most appropriate offset amount will be selected to narrow the distribution of the offset voltage in two stages. Moreover, the calibration results can be locked in the peripheral circuits by the initialization operation, thus, the calibration process is unnecessary for each read operation. Compared with the conventional voltage latch SA (VLSA) and the robust latch-type SA (RLSA), the simulation results show that the offset voltage of the proposed SA is reduced by 57.1% and 45.4%, respectively, at 1.2 V supply voltage with TT corner in TSMC 65-nm CMOS technology. Additionally, under the extreme conditions, it is also reduced by 49.9~58.3% and 35.8~47.9% compared with that of the VLSA and RLSA, respectively.

Keywords: sense amplifier, self-adaptive, distribution transformation technique, offset voltage, SRAM

Classification: Integrated circuits

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1 Introduction

With the rapid development of integrated circuit industry in recent years, static random access memory (SRAM) with high-speed, low-power features plays an increasingly significant role in circuit design [1, 2, 3]. For SRAM, the capacitances of the bit-line and the internal storage node are discharged to accomplish the read and write operation, respectively. Due to the capacitance of the bit-line is larger than that of the internal storage node, thus, the read speed determines the performance bottleneck of SRAM. For speed up the read operation, the sense amplifier is generally used [4]. Ideally, the sense amplifier can amplify an extremely small voltage difference. Actually, due to the mismatch exists in transistors caused by random dopant fluctuations [5], the offset voltage (V_{OS}) of it cannot be eliminated. And, the small voltage difference which less than the offset voltage will be improperly amplified.

In order to suppress the offset voltage for reliable read operation, many techniques were proposed. Ref. [6] presents a reconfigurable sense amplifier, which divides the conventional SA into two smaller ones. It effectively reduces the offset voltage without extra area consumption. However, four phases are need to accom-

plish the configurations. By choosing the best substrate voltage to reduce the offset, a digitized multiple body biasing technology was proposed in [7]. In this strategy, besides the calibration clock signal, a pair of extra input signals called DL and DLB are need, and many peripheral circuits, such as counter, decoder, latch, et al., are employed which leads to large area overhead. And the threshold matches by capacitive storage are used in Refs. [8, 9], however, the decision circuit and timing are quite complex. To increase offset tolerance, a self-adaptive distribution transformation technique with the aid of simple peripheral assisted circuit is proposed in this paper.

In this paper, we propose offset voltage suppressed sense amplifier with self-adaptive distribution transformation technique. The rest thesis organized as follows: Section II introduces the principle of the proposed circuit and Section III proposing the peripheral assisted circuits. Simulation results and analysis described in Section IV. Finally, conclusion of the paper in Section V.

2 Principle of the proposed circuit

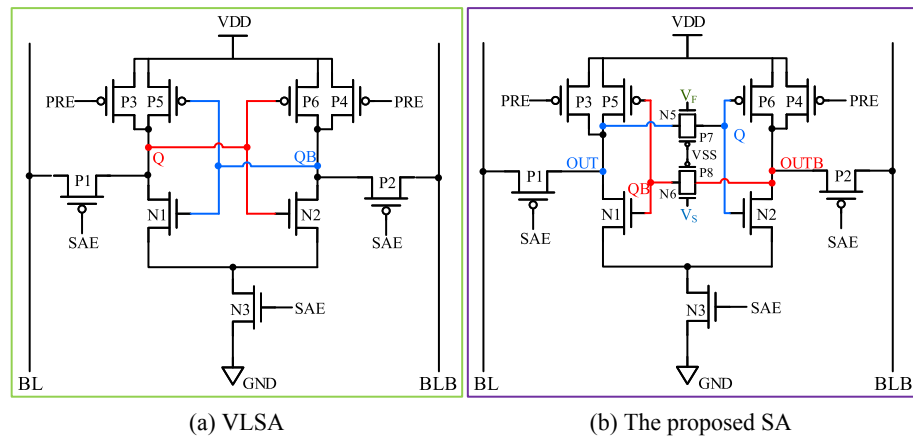


Fig. 1. Schematics of the conventional VLSA and the proposed SA.

Fig. 1(a) and (b) present the conventional VLSA and the proposed SA, respectively. As shown, compared with the conventional SA, two transmission gates are added between the internal storage nodes. Unlike the RLSA proposed in [10], in the proposed design, the gates of the PMOSs (P7 and P8) are connected to ground rather than the signal SAE. Thus, there is no threshold loss between the Q (QB) and OUT (OUTB) during the normal operation. Meanwhile, in order to suppress the offset voltage obviously by the digital calibration technique, the gates of the NMOSs (N5 and N6) are controlled by the signals V_F and V_S rather than BL and BLB. As shown in Fig. 1(b), the signals Q/QB and OUT/OUTB are pre-charged to high voltage. Assume that the threshold voltage of N2 is larger than that of N1, when the SAE is activated, the voltage of the node OUT/Q will be lower than OUTB/QB. Therefore, V_F will be set to a reference voltage which is smaller than V_S (V_S is set to VDD) to reduce this phenomenon. In order to suppressed the offset voltage by adjusting the gate voltage, V_G (V_S or V_F), of the NMOS (N5 or N6), the relationship between the change of offset voltage (ΔV_{OS}) and the V_G is

shown as Fig. 2. As shown in Fig. 2, it can conclude that ΔV_{OS} is almost linearly related to V_G . Thus, a quantitative offset will be achieved by adjusting the V_G .

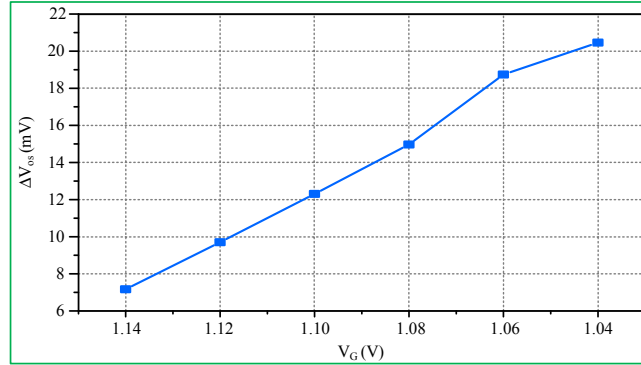


Fig. 2. Relationship between ΔV_{OS} and the V_G .

It is well known that, as shown in Fig. 3(a), the offset voltage distribution of conventional SA is a Gaussian distribution [11, 12, 13]. Based on this point, Fig. 3 gives the main concept of the self-adaptive distribution transformation technique proposed in this work. That is by judging the direction (positive or negative) of the offset voltage, an offset, M , is selected to compensate it (refer to Fig. 3(b)). If the direction of the offset voltage is changed after calibration, indicating that the original value of offset voltage is less than M (blue and green parts). In this case, the compensation will be revoked and a smaller offset, N , is selected to accomplish the compensation (refer to Fig. 3(c)). On the contrary, that is the original value of offset voltage is large than M (red and yellow parts), the amount of the offset remains unchanged. By this means, the offset voltage distribution of conventional SA is visually calibrated as Fig. 3(d) shown.

In order to determine the value of M and N , the offset voltage probability distribution density of the conventional SA is assumed as follow:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \quad (1)$$

Where, the x is the original value of offset voltage, μ and σ are the mean and the standard deviation of the original offset voltage, respectively. Meanwhile, assuming that $M > 2N$, $\alpha = \frac{(|x_0|+M)^2}{2\sigma^2}$, $\beta = \frac{(|x_0|+N)^2}{2\sigma^2}$, and $\gamma = \frac{(|x_0|-N)^2}{2\sigma^2}$, thus, the offset voltage probability distribution density after calibration, $f_0(x_0)$, can be deduced as follow:

$$f_0(x_0) = \begin{cases} \frac{1}{\sqrt{2\pi}\sigma} (e^{-\alpha} + e^{-\beta} + e^{-\gamma}), & |x_0| < N \\ \frac{1}{\sqrt{2\pi}\sigma} (e^{-\alpha} + e^{-\beta}), & N < |x_0| < M - N \\ \frac{1}{\sqrt{2\pi}\sigma} e^{-\alpha}, & |x_0| > M - N \end{cases} \quad (2)$$

As equation (2) given, taking the $x_0 > 0$ as an example, the analyses of it are demonstrated as follow:

Case 1): When $x_0 < N$, the $f_0(x_0)$ is consisted by three parts: a) x between $-N$ and 0, by right shifting an offset N , b) x voltage between N and $2N$ by left shifting an offset N , and c) x between M and $M + N$ by left shifting M .

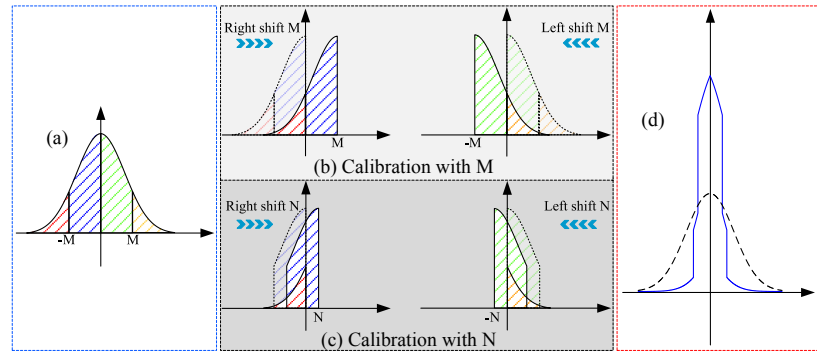


Fig. 3. Concept of the self-adaptive distribution transformation technique proposed in this work.

Case 2): When $N < x_0 < M - N$, the $f_0(x_0)$ is consisted by two parts: a) x between $2N$ to M with left shifting N , and x between $M + N$ and $2M - N$ with left shifting M .

Case 3): When $x_0 > M - N$, the $f_0(x_0)$ is consisted by the x larger than $2M - N$ with left shifting M .

Thus, the value of ΔV_{OS} can be deduced as equation (3):

$$\sigma_0^2 = \int_{-\infty}^{+\infty} x_0^2 f_0(x_0) dx_0 \quad (3)$$

As formulas (2) and (3) shown, the value of M and N can be obtained by solving the minimum value of σ_0 (i.e. the maximum value of $1/\sigma_0^2$, as the Fig. 4 shown).

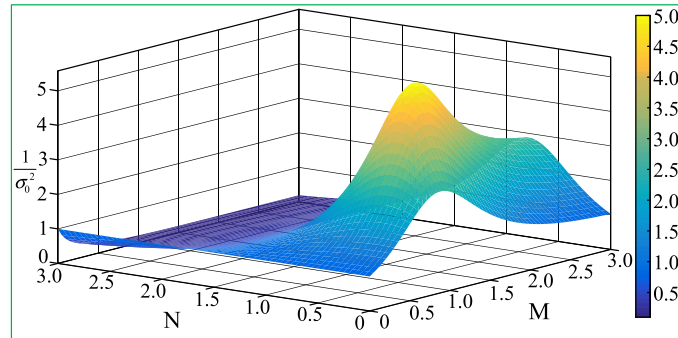


Fig. 4. The relationship among the minimum value of σ_0 and the offsets (M and N), as $\sigma = 1$ for example.

3 Peripheral assisted circuits

In order to achieve the function of self-adaptive distribution transformation, the peripheral assisted circuits are shown in Fig. 5. Where, the Fig. 5(a) presents the circuits for determining the direction (positive or negative) of the offset voltage and selecting the offset amount (M or N). The judgment results of the direction are locked in the circuits shown in Fig. 5(b). And the generation circuits of reference voltages corresponding to M and N , respectively, are shown in Fig. 5(c).

The calibration process is consisted of two stages, as shown in Fig. 6(a). Initially, the proposed SA is pre-charged, and the signals, RSET and CK are set to high voltage level. When the signals mentioned above are discharged to low

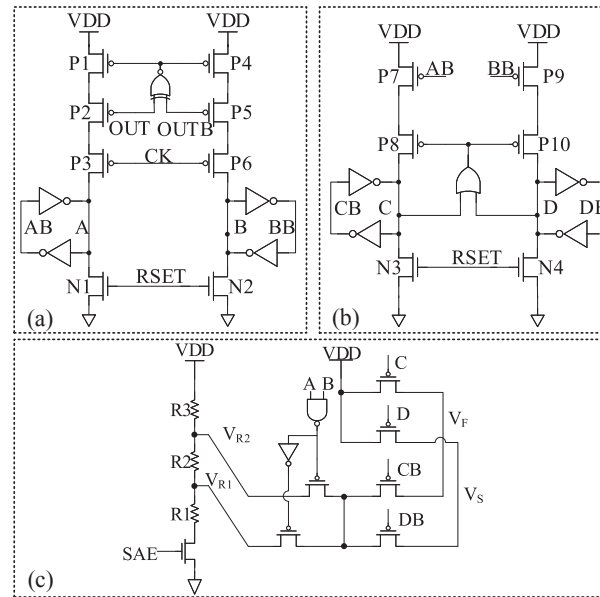


Fig. 5. Peripheral assisted circuits of the proposed SA, (a) the offset voltage determining and offset amount selecting circuit, (b) the result-latching circuit, and (c) the generation circuits of reference voltages.

voltage, and SAE is activated, the first stage of calibration process is started. In this stage, the direction of the offset voltage will be determined. Assuming that the output of SA caused by the mismatch is ‘0’ ($OUT = ‘0’$), the internal signals, $A = C = ‘1’$, and $B = D = ‘0’$. As a result, $V_F = V_{R1}$, V_S remains as VDD and a larger offset, M , corresponding to V_{R1} will be compensated. In the second stage, the offset amount will be selected. Similarly, the proposed SA is pre-charged before the process beginning. When SAE is activated again, the output of SA will be obtained based on the mismatch and the compensation in the first stage. With the assumption above, if $OUT = ‘1’$, it means that the original offset voltage is smaller than M and there is a over-compensation in the first stage. As a result, $A = B = C = ‘1’$, and $D = ‘0’$. Correspondingly, the $V_F = V_{R2}$, V_S still remains as VDD. Thus, the offset, M , will be revoked, and a smaller offset, N , corresponding to V_{R2} will be compensated, as shown in Fig. 6(b). On the contrary, if $OUT = ‘0’$, the compensation amount remains unchanged, as shown in Fig. 6(c). Then the $CK = ‘1’$, the compensation process finished, all the data are locked in the assisted circuits for the regular work, thus, only two clock cycles are needed for the proposed technique.

4 Simulation results and discussion

In order to verify the efficiency of the proposed self-adaptive distribution transformation technique, the simulations are accomplished based on the Taiwan Semiconductor Manufacturing Company's 65-nm CMOS technology. Under this process condition, the μ and σ of the proposed SA without calibration (i.e., V_F and V_S are set to VDD) are about 0 V and 13.6 mV, respectively. According to the formulas (2) and (3), by solving the minimum of σ_0 (here, σ_0 is about 5.85 mV), it can be deduced that M and N are about 18 mV and 8 mV, respectively, as shown in Fig. 7. Thus, the V_{R1} and V_{R2} will be achieved according to the Fig. 2.

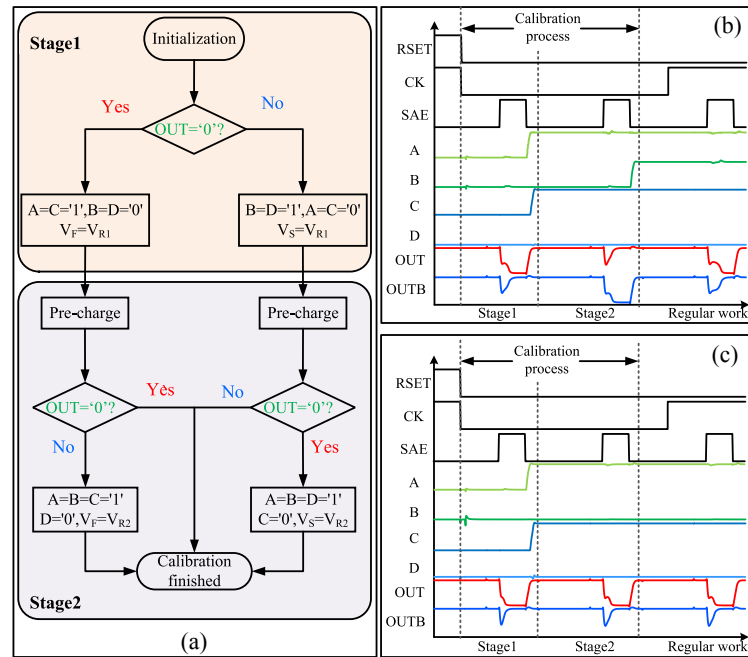


Fig. 6. (a) The calibration process of the self-adaptive distribution transformation technique, (b) waveform with over-compensation in fist stage, and (c) waveform without over-compensation in fist stage.

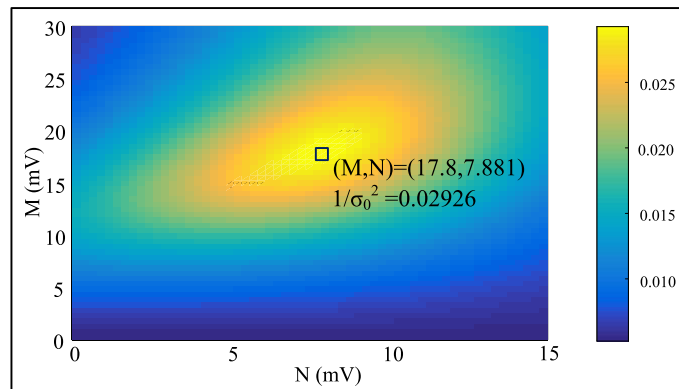


Fig. 7. The values of M and N obtained from TSMC 65 nm CMOS technology.

Fig. 8 presents the waveform of the conventional VLSA and the proposed SA. Where, for the proposed SA, when $V_F = V_S = V_{DD}$, there is no calibration. As Fig. 8(a) shown, the decrease of the minimum value of OUTB indicates the offset voltage reducing. Thus, the minimum value of OUTB_W (represent with calibration) smaller than OUTB_W/O (represent without calibration) demonstrates that the offset voltage will be optimized by the proposed technique.

Fig. 9 shows the scatter diagram of the 2500 times Monte Carlo simulation results for the VLSA, RLSA and proposed SA under different process corners. It can be found that the offset voltage of the proposed SA is reduced by 49.9~58.3% and 35.8~47.9% compared with that of the VLSA and RLSA, respectively, which indicates the proposed SA still worked better than the VLSA and RLSA in suppressing the offset voltage under the extreme conditions.

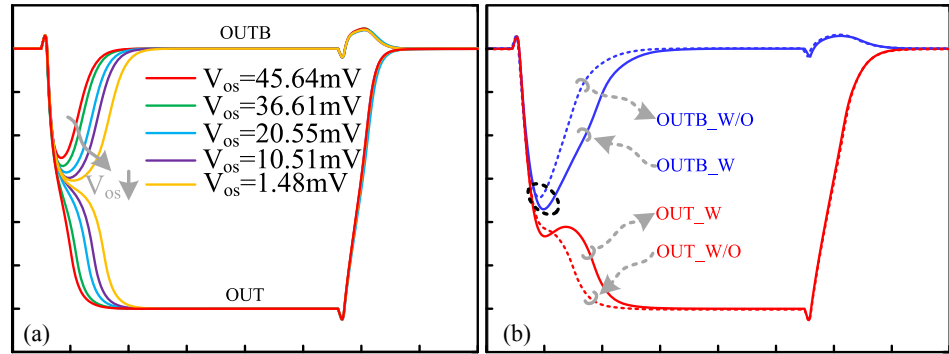


Fig. 8. Waveforms of (a) the conventional VLSA with different V_{OS} , and (b) the proposed SA (_W and _W/O represent with and without calibration, respectively.).

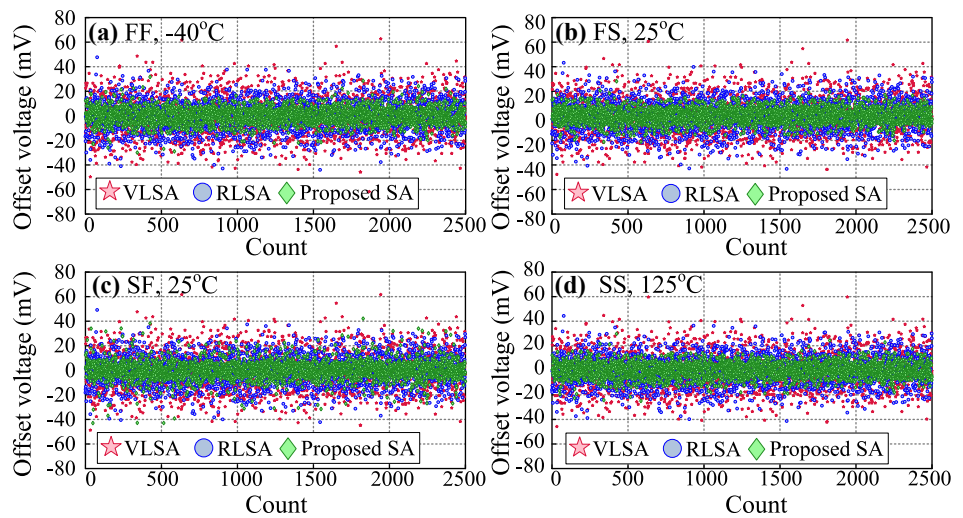


Fig. 9. Scatter diagram of the Monte Carlo simulation results under different corner.

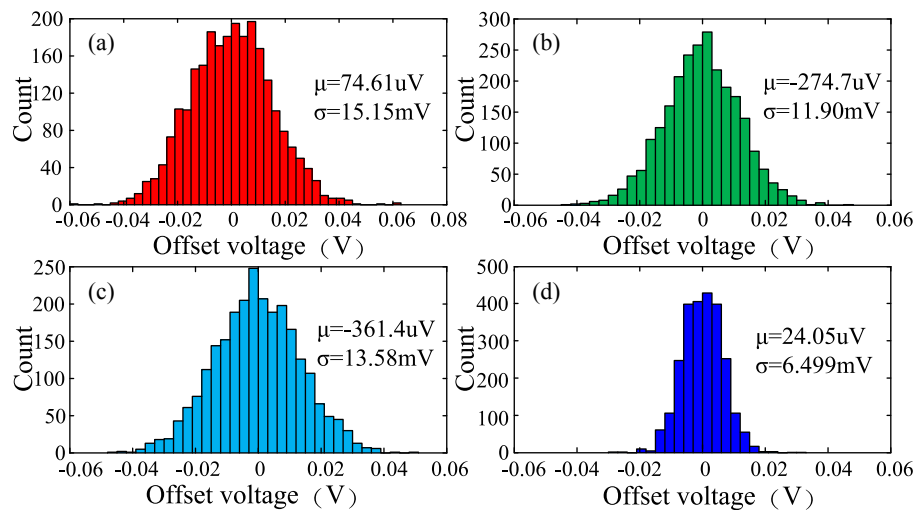


Fig. 10. Histograms of the Monte Carlo simulation results at the TT corner, (a) VLSA, (b) RLSA, (c) the proposed SA without calibration and (d) the proposed SA with calibration.

the TT corner. As shown in Fig. 10, for the proposed SA, the standard deviation achieves 52.14% reduction after calibration, and it is also reduced by 57.10% and 45.38% compared with that of the conventional VLSA and RLSA, respectively.

5 Conclusions

Self-adaptive distribution transformation technique is proposed for suppressing the offset voltage of the SRAM sense amplifier in this paper. Simulation results show that, the standard deviation of offset voltage can be reduced by 57.10% and 45.38% compared with that of the conventional VLSA and RLSA at 1.2 V under TT corner.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 61674002 and 61474001) and National Science and Technology Major Project (Grant No. 2017ZX01028-101-003).