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Accurate large-signal modeling using neuro-space mapping for power transistors

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Abstract: In this paper, a novel neuro-space mapping (Neuro-SM) modeling approach for lager-signal transistors is proposed. A new structure of Neuro-SM model with capacitors and inductors is created to change the DC and AC characteristic of the model respectively. An additional current signal extracted with a novel nonlinear function is adopted to improve the large-signal characteristic of existing device models while remain the ***S***-parameters unchanged. A step-by-step training method is developed for fast training of the proposed Neuro-SM model avoiding variables adjustment repeatedly. In addition, the modeling experiment for measurement data of LDMOS transistor demonstrate that the novel Neuro-SM method can accurately reflect the large-signal characteristics of transistor with simple operation process and enhance the accuracy of the existing model.

Keywords: large-signal model, transistors, Neuro-SM, modeling

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

With the development of semiconductor manufacture techniques, developing accurate computer-aided design (CAD) models of large-signal power transistors becomes necessary [1, 2]. Accurate large-signal models for the power transistors which can be used in commercial microwave circuit simulators play a decisive role in the circuit/system design [3]. Furthermore, the increasing integration of the monolithic circuit has reinforced the need of efficient large-signal modeling method to minimize the required number of design and fabrication cycles.

Recently, neuro-space mapping (Neuro-SM) techniques have been recognized as useful alternatives to conventional approaches in microwave modeling [4, 5]. This technique uses neural networks to map the voltage or current signals of the existing device model into that of the device data. The Neuro-SM method can be applied to not only the simple DC and ***S***-parameters modeling of nonlinear devices, but also the complex large-signal modeling [6, 7, 8]. In [9], a dynamic neural network is used as the mapping network for the Neuro-SM model of power transistors. Two mapping networks are added over the existing device model in [10] to match the transistor outputs in large-signal simulations. These existing Neuro-SM modeling methods improve the DC and AC characteristic by using the same optimized variables, which make the variables interact and increase the difficulty of the optimization process. The research on the large-signal modeling method with high precision and simple operation is still an open topic.

In this paper, a new Neuro-SM structure with a novel mapping network for lager-signal transistor modeling is created. A new nonlinear function is developed to improve the larger-signal characteristic of the existing model while remain the DC and ***S***-parameters characteristic of the existing model unchanged. An advanced training method is developed reducing the difficulty of optimization. The proposed modeling method can match the device well with a few optimized variables and simple operation process.

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2 Proposed large-signal modeling method

2.1 Proposed Neuro-SM model

Normally, the existing device models which are roughly similar to the devices are defined as the coarse model, and the actual data from simulator or measurement are defined as the fine model. Fig. 1 shows a new Neuro-SM model for power transistor. Let $\boldsymbol{v}_c = [v_{gc}, v_{dc}]^{\mathrm{T}}$ and $\boldsymbol{i}_c = [i_{gc}, i_{dc}]^{\mathrm{T}}$ represent the voltage and current signals of the coarse model respectively. Let $\boldsymbol{v}_f = [v_{gf}, v_{df}]^{\mathrm{T}}$ and $\boldsymbol{i}_f = [i_{gf}, i_{df}]^{\mathrm{T}}$ represent the voltage and current signals of the fine model respectively. The input voltage signals $\boldsymbol{v}_f$ are mapped into $\boldsymbol{v}_c$ by voltage controlled voltage source achieving $v_{gc} = v_{gf}$ and $v_{dc} = v_{df}$. We proposed to add capacitors and inductors into the circuit dividing the output current of the coarse model into DC component $\boldsymbol{i}_{c\_DC}$ and AC component $\boldsymbol{i}_{c\_AC}$. The capacitors and inductors make the model more flexible and make it possible to change the DC and AC characteristic of the model respectively. In the proposed Neuro-SM model, the DC component $\boldsymbol{i}_{c\_DC}$ is directly transmitted to the fine model terminal while the AC component $\boldsymbol{i}_{c\_AC}$ is mapped into the fine model $\boldsymbol{i}_{f\_AC}$ by a novel mapping network. This model can change the AC feature of the coarse model without changing DC feature, which can improve the large-signal characteristic more effective. The proposed mapping network is realized by the current controlled current source.

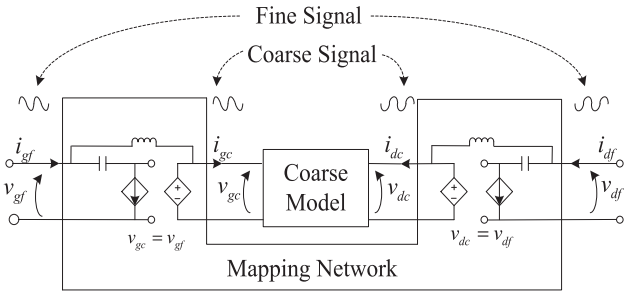

Fig. 1. Structure of the circuit-based Neuro-SM model for power transistors.

In order to further describe the proposed model, Fig. 2 shows the schematic of the proposed model in the large-signal simulation. The AC component of the output current at the drain electrode is the main factor for the mismatch between the coarse model and the fine model in the large-signal simulation. We focus on the output signal of the models at the drain electrode and add subscript d to represent the relevant signals. The output current signals i_{dc_DC} and i_{dc_AC} of the coarse model are obtained with the excitation signals: the input power P_{in}, the source impedance Z_S, the load impedance Z_L, the fundamental frequency $freq$, and the bias voltages v_{gf} and v_{df}. In Fig. 2, the proposed mapping network realizes signal adjustment from $\boldsymbol{i}_{dc}$ to $\boldsymbol{i}_{df}$. The accurate output of the proposed model: the output power P_{out}, the gain $Gain$, the power efficiency η and the power added efficiency PAE, can be calculated with the excitation signals and the mapping current i_{df} by the function module.

In the mapping network, the signal i_{dc_add} is proposed as an additional current which is extracted with the novel nonlinear formula $f_{FUN}(\cdot) \bullet f_{ANN}(\cdot)$ as follows:

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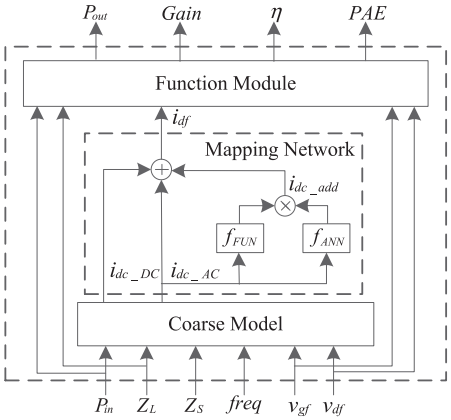

Fig. 2. Schematic of the Neuro-SM model for large-signal power transistors.

$$i_{dc\_add} = f_{FUN}(i_{dc\_AC}, \boldsymbol{k}) \bullet f_{ANN}(i_{dc\_AC}, \boldsymbol{w}) \tag{1}$$

where the formula $f_{ANN}(\cdot)$ is obtained by a multilayer perceptron (MLP), and $\boldsymbol{w}$ represents the synaptic weights in the MLP network. $f_{FUN}(\cdot)$ can be computed as

$$f_{FUN}(i_{dc\_AC}, \boldsymbol{k}) = \begin{cases} a_1 * (i_{dc\_AC} - b_1)^3, & i_{dc\_AC} > b_1 \\ 0, & b_2 \le i_{dc\_AC} \le b_1 \\ a_2 * (i_{dc\_AC} + b_2)^3, & i_{dc\_AC} < b_2 \end{cases} \tag{2}$$

where $\boldsymbol{k}$ is a vector containing all optimized variables in the formula $f_{FUN}(\cdot)$, such as a_1, a_2, b_1 and b_2. The function $f_{FUN}(\cdot)$ is adopted to ensure that the large-signal characteristics of the coarse model are changed while the $\boldsymbol{S}$-parameters of that remain unchanged. The large-signal characteristics can be greatly improved by the function $f_{FUN}(\cdot)$ with appropriate variables value. The formula $f_{ANN}(\cdot)$ further improves the accuracy of the Neuro-SM model by adding more free variables. The mapping current i_{df} can be described as

$$i_f = i_{dc\_DC} + i_{dc\_AC} + i_{dc\_add} \tag{3}$$

2.2 Proposed training method

An appropriate mapping network is obtained by training the proposed Neuro-SM model with the transistor data. The training error represents the difference of large-signal characteristics between the model and the fine device data, as follows:

$$E(\boldsymbol{w}, \boldsymbol{k}) = \frac{1}{2} \sum_{i=1}^{4} \sum_{n=1}^{N} \| A^i (Y_n^i(\boldsymbol{w}, \boldsymbol{k}) - Y_{nD}^i) \|^2 \tag{4}$$

where Y_{nD}^i and $Y_{\boldsymbol{n}}^{\boldsymbol{i}}(.)$ are the large-signal response of the transistor data and the proposed Neuro-SM model, respectively. The superscript i means the index of the large-signal response, and the response Y_{nD}^1, Y_{nD}^2, Y_{nD}^3 and Y_{nD}^4 represent P_{out}, $Gain$, η and PAE respectively. The subscript n is the training data index, and N is the total number of the training data. $\boldsymbol{A}$ is the scaling variable which is equal to the reciprocal of the maximum-to-minimum of the output signal Y_{nD}^i.

In order to improve the optimizing efficiency of the novel Neuro-SM model, an efficient training method is proposed as follows:

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Step 1) Initialize the mapping network by solving $f_{FUN}(i_{dc\_AC}, \boldsymbol{k}) = 0$ and $f_{ANN}(i_{dc\_AC}, \boldsymbol{w}) = 1$ and obtain the initial variables $(\boldsymbol{k}_0, \boldsymbol{w}_0)$, which can avoid reducing the coarse model performance.

Step 2) Fix the variable $\boldsymbol{w}_0$ and optimize the variables $\boldsymbol{k}_0$ to $\boldsymbol{k}^*$ making the training error as small as possible, which can achieve the significant performance improvements with a few iterations.

Step 3) Fix the variable $\boldsymbol{k}^*$ and optimize the variables $\boldsymbol{w}_0$ to $\boldsymbol{w}^*$ making the training error as small as possible, which can further improve the accuracy of the Neuro-SM model in the large-signal simulation.

Step 4) Optimize the variables $(\boldsymbol{k}^*, \boldsymbol{w}^*)$ to $(\boldsymbol{k}^{\#}, \boldsymbol{w}^{\#})$ making the training error as small as possible, which can make the Neuro-SM model match the device data well.

The proposed training method speeds up the modeling process by adjusting the variables in steps, which can avoid variables adjustment repeatedly. The accurate Neuro-SM can be obtained with few variables and simple operation. After training, the proposed Neuro-SM model can be used as accurate and fast models for efficient high-level circuit and system design.

3 Experimental verification

In this example, the proposed method is applied to measured LDMOS transistor AFT18S230. The model with the method in [5] which has good agreement with the measurement data of AFT18S230 in DC and ***S***-parameters simulation is used as the existing coarse model. The I-V curve and the ***S***-parameters characteristics at the quiescent bias point ($V_{gf} = 2.75$ V, $V_{df} = 28$ V) are shown in Fig. 3. As seen from the figure, the proposed model can maintain the high precision of the coarse model in DC and ***S***-parameters simulation.

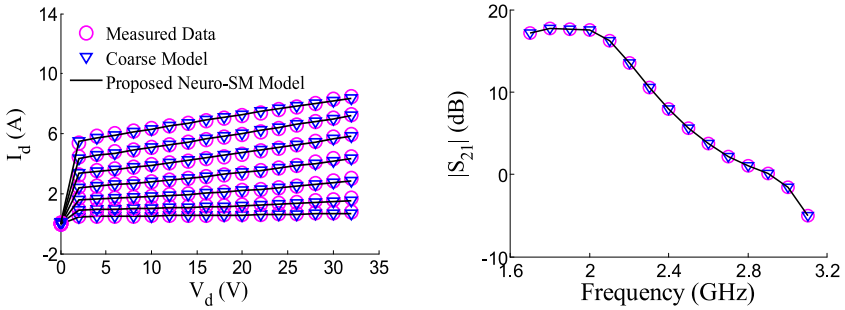

Fig. 3. I-V and ***S***-parameters comparison between the measured data and the models.

To verify the accuracy and feasibility of the proposed modeling method, we compared the large-signal characteristic of the proposed model with that of the coarse model as well as the middle model which is composed of the coarse model and the formula $f_{FUN}(\cdot)$. Those models operate with $V_{gf} = 2.75$ V, $V_{df} = 28$ V, $freq = 1.805$ GHz, $Z_S = 1.535 - j4.232\,\Omega$ and $Z_L = 1.403 - j3.748\,\Omega$ in harmonic balance (HB) simulation. The input power P_{in} sweep from 4.2 to 40.2 dBm and the step of P_{in} is 2 dBm. The errors of the three models which demonstrate that the proposed Neuro-SM model has higher accuracy are shown in Table I.

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Table I. Accuracy comparison of the three models in HB simulation

Parameters	Coarse Model Error (%)	Middle Model Error (%)	Proposed Model Error (%)
P_{out}	5.1	0.8	0.9
Gain	11.1	3.3	2.2
η	16.1	3.9	1.6
PAE	13.2	4.0	1.7

To further show the detail results, the *Gain* and *PAE* comparison of the three models is shown in Fig. 4. The three models can match the data well with low P_{in}. However, as the input power increases, the gap between the coarse model and the measured data becomes larger. The performance of the middle model is much better than that of the coarse model, but the mismatch between the middle model and the measured data cannot be ignored. The proposed model has the best agreement with the measured data than the other models, which demonstrates that the novel Neuro-SM method improves the current capabilities of the coarse model.

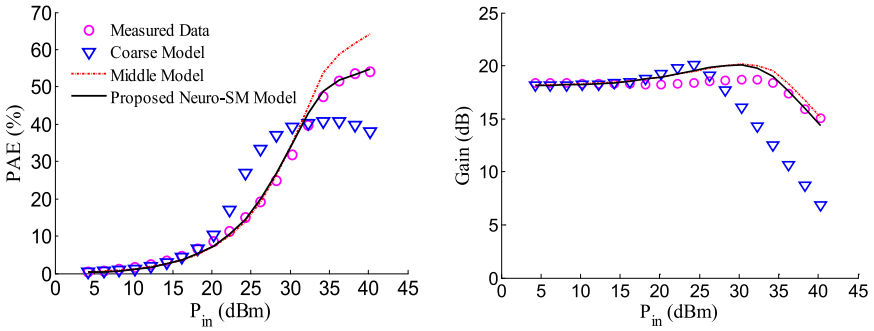

Fig. 4. The *Gain* and *PAE* comparison between the measured data and the models.

4 Conclusion

In this paper, an effective and convenient lager-signal transistor modeling method based on the Neuro-SM is created. The proposed model can improve the larger-signal characteristic of the coarse model while remain the DC and ***S***-parameters characteristic unchanged. The novel modeling method is not only accurate but also easy to operate, which meets the development requirements of electronic technology.

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