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Picowatt 0.5 V supply with 3 ppm/°C CMOS voltage reference for energy harvesting system

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Abstract: This paper presents a novel picowatt CMOS voltage reference for energy harvesting (EH) system applications. The output voltage is 133.6 mV with subthreshold operations of MOSFETs at a supply of 0.5 V. It was simulated in 0.18-µm CMOS technology. The simulation results show voltage variation of 0.594%/V line sensitivity for supply voltage from 0.5 V to 3 V and about 3 ppm/°C of temperature variation from −20°C to 80°C. Its power consumption is only 205.027 pW. The power supply rejection ratio (PSRR) has been kept stably at −41.99 dB up to GHz level.

Keywords: voltage reference, picowatt, subthreshold operation, energy harvesting

Classification: Energy harvesting devices, circuits and modules

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1 Introduction

A current attractive substitute to conventional battery-powered or self-power-ed devices or system is energy harvesting (EH), which gathers energy from the ambient available sources including photovoltaic, thermal, piezoelectric and RF energy [1]. Because these devices employing EH technology usually work in harsh temperature conditions, the voltage reference should be more insensitive to temperature. Due to the weak surrounding energy sources and poor conversion efficiency, the output power of EH system is low and output voltage has a large swing. Thus, voltage reference circuit embedded in an EH system must operate in low power, low voltage and be insensitive to supply.

Over the years many methods have been proposed to realize the voltage reference in low-power and low-voltage [2, 3, 4, 5, 6, 7]. A common approach is to use devices with different threshold voltages (Vth) biased in weak inversion to achieve low power requirement and obtain a temperature independent voltage reference [2, 3, 4, 5, 6, 7]. A voltage reference with 2-Transistor structure has been proposed in [2], which only includes a native NMOS and a standard NMOS with different threshold voltages. Based on the Vth difference, a voltage reference is generated only consuming picowatt power, operating in low voltage and being insensitive to supply. However, native transistor usually lacks accurate device model [8], has relatively large leakage current and is not supported by all standard CMOS technologies. In [4], Oliveira et al. explore the relevance between Vth and transistor length to obtain two distinct Vths, but the Vth difference generated using this approach is low which could not produce large enough voltage output.

In this work, a 3-Transistor structure voltage reference based on temperature compensation technique derived from subthreshold operation characteristics was proposed. It can operate from 0.5 to 3 V, consume 205.027 pW, and obtain a temperature coefficient (TC) as low as 3 ppm/°C.

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2 Proposed circuit and principle

Fig. 1(a) shows the conventional 3-T voltage reference with all transistors operating in weak inversion [4]. The M1 and M2 form the self-cascode structure which is used to produce the Vth difference and the biased current is provided by M3.

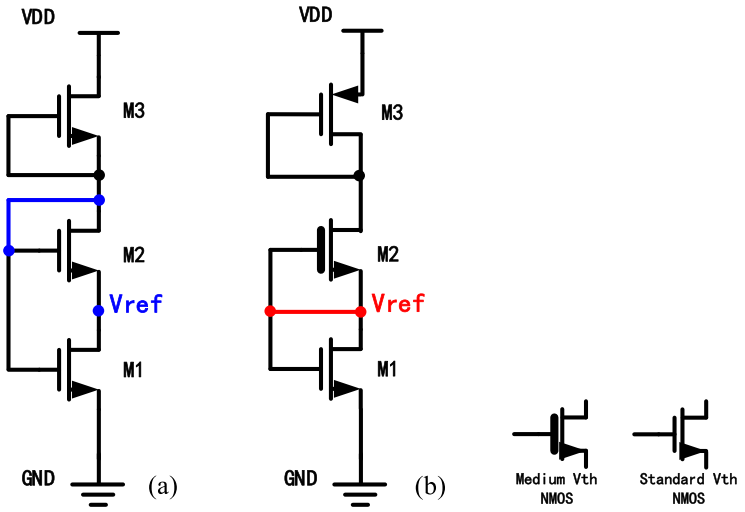

Fig. 1. (a) Conventional 3-T voltage reference (b) Proposed 3-T voltage reference

The I-V characteristic of NMOS transistor operating in weak inversion can be expressed as [9]:

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}(n-1)V_T^2 e^{\frac{V_{GS}-V_{TH}}{nV_T}}\left(1 - e^{\frac{-V_{DS}}{nV_T}}\right) \tag{1}$$

where μ_n, C_{ox}, n, W/L, V_T, V_{GS}, V_{DS} is the electron mobility, oxide capacitance per unit area, subthreshold slope factor, transistor sizes ratio, thermal voltage, the gate-source voltage and the drain-source voltage of the transistor, respectively. To ensure $V_{DS} > 4V_T$, I_{ds} is

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}(n-1)V_T^2 e^{\frac{V_{GS}-V_{TH}}{nV_T}} \tag{2}$$

For the drain current of M1 is

$$I_{ds1} = \mu_{n1} C_{ox1}\left(\frac{W}{L}\right)_1 (n_1 - 1){V_T}^2 \exp\left(\frac{V_{GS1} - V_{TH1}}{n_1 V_T}\right) \tag{3}$$

Similarly, the drain current of M2 is

$$I_{ds2} = \mu_{n2} C_{ox2}\left(\frac{W}{L}\right)_2 (n_2 - 1){V_T}^2 \exp\left(\frac{V_{GS1} - V_{ref} - V_{TH2}}{n_2 V_T}\right) \tag{4}$$

Because $I_{ds1} = I_{ds2}$, thus,

$$V_{ref\_con} = n_2 V_T \ln \frac{\mu_{n2} C_{ox2}\left(\frac{W}{L}\right)_2 (n_2 - 1)}{\mu_{n1} C_{ox1}\left(\frac{W}{L}\right)_1 (n_1 - 1)} + \frac{n_2 V_{TH1} - n_1 V_{TH2}}{n_1} + \frac{n_1 V_{GS1} - n_2 V_{GS1}}{n_1} \tag{5}$$

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The first term in (5), the thermal voltage V_T, is proportional to the absolute temperature (PTAT) and the second term, the Vth difference, is complementary to the absolute temperature (CTAT) [10]. However, the third term in (5), V_{GS1}, has a bad temperature variations linearity. This influence factor could be difficult to eliminate in this structure because that subthreshold slope factor of M1 and M2 are distinct.

To solve this problem, a novel voltage reference is proposed in this work as shown in Fig. 1(b). Here, a standard PMOS transistor M3 is diode connected to serve as a current generator, M1 and M2 are configured by connecting their gates together to the source of M2 as reference voltage output. Refer to the previous derivation, its output voltage can be obtained as follows:

$$V_{ref\_novel} = n_1 V_T \ln \frac{\mu_{n2} C_{ox2} \left(\frac{W}{L}\right)_2 (n_2 - 1)}{\mu_{n1} C_{ox1} \left(\frac{W}{L}\right)_1 (n_1 - 1)} + \left(\frac{n_2 V_{TH1} - n_1 V_{TH2}}{n_2}\right) \tag{6}$$

In (6), the nonlinear temperature coefficient component in (5) is removed, which helps to improve the TC performance. Thus, with proper sizing of transistors adopted in this circuit, the influence of temperature on voltage variation can be minimized. The transistors sizes configuration in this design was listed in Table I.

Table I. Transistor sizing in this circuit

Transistors	M1	M2	M3
Size W/L (μm/μm)	17/10	27/10	4/10

In this structure, medium Vth transistor (M1) and standard Vth transistor (M2) are employed to obtain bigger Vth difference instead of adopting the same type transistor with different gate lengths in [4]. M3 helps to shield M1 and M2 from supply variations and also provides the bias current. Long channel devices are employed to reduce the subthreshold voltage difference sensitivity to VDD and the drain induced barrier lowering (DIBL) and other short channel effects [2]. Moreover, because the circuit is biased with the leakage current, a startup circuit is not needed.

3 Simulation results and comparison

The proposed voltage reference depicted in Fig. 1(b) was realized in TSMC 0.18 μm CMOS process. Fig. 2(a) shows temperature coefficient when VDD = 0.5 V. The average voltage is 133.6 mV with 0.04 mV deviation, which is 3 ppm/°C. Fig. 2(b) shows that power consumption of this circuit at room temperature (27°C) is 205.027 pW (410.054 pA × 0.5 V).

Fig. 2(c) illustrates the supply voltage dependence with the line sensitivity of 0.594%/V for VDD ranging from 0.5 V to 3 V at room temperature. The simulated supply rejection ratio is presented in Fig. 2(d) showing −45.76 dB at 100 Hz with 0.5 V supply voltage and this parameter can be kept stably at −41.99 dB with the frequency up to GHz level.

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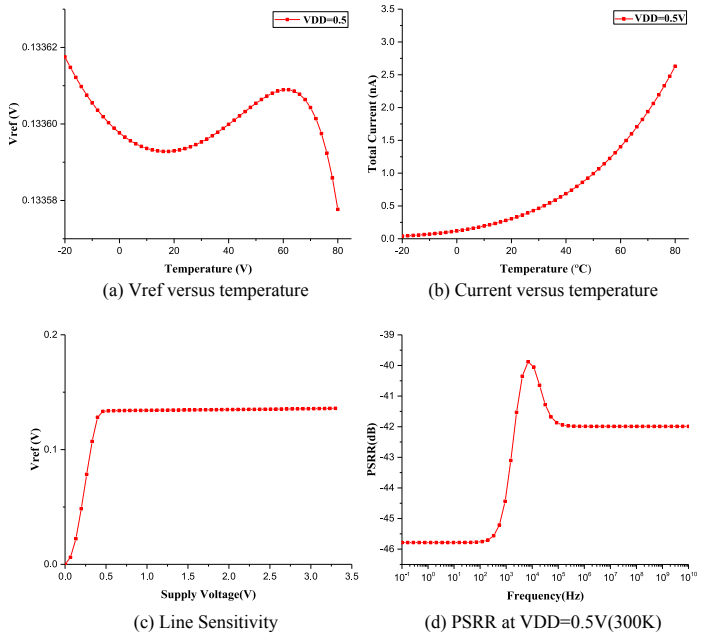

(a) Vref versus temperature (b) Current versus temperature

(c) Line Sensitivity (d) PSRR at VDD=0.5V(300K)

Fig. 2. The simulation results of the proposed voltage reference.

Table II summarizes the main characteristics of the proposed voltage reference in comparison with other similar designs. The proposed reference circuit has the smallest TC compared to [2, 4, 5, 6], which indicates this circuit can be used to improve the TC performance. As shown in Table II, the minimum design supply voltage of the proposed reference circuit is 0.5 V with 205.027 pW.

Table II. Comparison with other voltage reference

	This work	[2]	[4]	[5]	[6]
Process (μm)	**0.18 μm**	0.13 μm	0.13 μm	0.18 μm	0.18 μm
Power (pW)	**205.027**	10.85	7	9600	400
Temp.Range (°C)	**−20–80**	−20–80	0–120	−20–80	−40–120
Supply.Voltage (V)	**0.5–3.0**	0.5–3.0	0.3–1.2	0.75–3.5	0.7–2.5
Vref.Voltage (V)	**133.6m**	341.5m	85m	319m	263.1m
TC (ppm/°C)	**2.981(3)**	80.2	17.4	7.2	9.5
Line Sensitivity (%/V)	**0.594**	0.036	0.417	0.0752	0.84
PSRR (dB)	**−45.76 @100 Hz −41.99 @1 GHz**	−58 @100 Hz −59 @100 kHz	−18 @100 Hz	−79 @100 Hz −56 @1 MHz	N/A

4 Conclusion

In this paper, a picowatt, 0.5 V with 3 ppm/°C voltage reference is proposed and simulated in 0.18 m CMOS technology. All transistors are operating in sub-threshold region to obtain a low power consumption of 205.027 pW. Its TC is 3 ppm/°C in the range of −20°C to 80°C and its line sensitivity achieves 0.594%/V from 0.5 V to 3 V. Due to these good characteristics, the proposed circuit shows its advantages in ultra-low power and temperature variation tolerant applications, such as EH systems and sensing systems.

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