

Impact of mutual inductance on timing in nano-scale SoC

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Abstract: This paper investigates the impact of mutual inductance (M) on interconnect signal delay estimation according to resistance (R), inductance (L), and capacitance (C) in nano-scale system on a chip (SoC), suggesting a method to predict and suppress the impact. The proposed methodology first calculates the difference in delay between RLC and $RLMC$ wire models for a set of parameter variations, then builds response surface functions (RSF) using physical parameters including wire width and spacing. The proposed method contributes to the following actions.

- 1) Describe design rules to avoid mutual inductance effects.
- 2) Select wires which require $RLMC$ models for delay estimation.
- 3) Correct the estimated delay when using an RLC model.

As an example, situations to limit the mutual inductance effect is shown as to a 14 nm technology node.

Keywords: on chip inductance, mutual, screening, delay, timing analysis, nano-scale, system on a chip

Classification: Integrated circuits

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1 Introduction

Impacts of on-chip inductance on signal propagation delay have been discussed [1, 2, 3, 4] for 1 GHz or higher clock frequencies. The articles [1, 2] revealed effects of on-chip self-inductance and then proposed methods for screening interconnects which should be treated as *RLC* models [5, 6], rather than the conventional *RC* expressions [7]. As for the recent System-on-a-Chip (SoC) applications including 4K8K HDTV processing [8], processor cores need more speed to complete the required operations. Towards further high clock frequencies, the articles [3, 4] pointed out necessity of taking into consideration the inductive coupling effects in timing analysis. In order to reappear the inductive coupling effects, we have to extract the mutual-inductance (*M*) in addition to the loop self-inductance (*L*) [9, 10]. However, the existing papers have not explicitly suggested screening methods of on-chip mutual-inductance effects, which predict physical dimensions of interconnects to require *RLMC* models.

We propose a method to screen the mutual inductance effects on timing in terms of physical dimensions including wire width, spacing, and distance from the

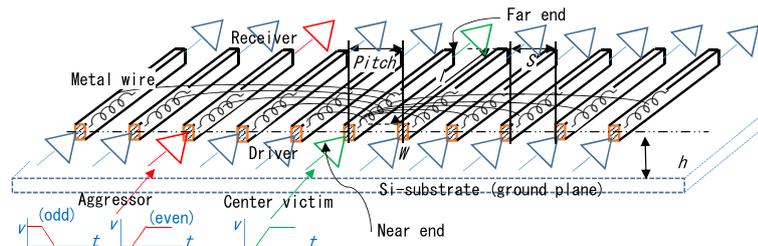


Fig. 1. Interconnect structure for screening the mutual inductance effect.

aggressor [11]. This paper reveals layout pattern dependence of the *RLC* delay estimation error compared to the *RLMC* delay, as well as describing the screening method. Using the results, we can minimize signal delay estimation errors associate with the inductive coupling.

2 Screening method of the impact of mutual inductance on timing

The overall flow consists of the following two steps.

1. Estimation of difference in signal propagation delay between wire models with and without mutual inductance (*M*).
2. Generation of RSF to predict the delay difference between *RLMC* and *RLC* models using physical dimension for mutual inductance impact evaluation along with precise timing analysis.

2.1 Estimation of difference in signal propagation delays

Three dimensional interconnect structures under test have cross-sectional dimensions including metal and dielectric thickness defined by the wafer process technologies. Conversely, horizontal dimensions such as width, spacing, and length of wires can be managed by designers. The horizontal dimension parameters are treated as variables. Fig. 1 shows the interconnect structure. We assume regular meshes of ground grids that provides the return current. Here, all neighbors are considered as candidates of the current return path during *RLC* extraction with the lumped self-inductance *L*. On the other hand, selection of the current return path affects inductive coupling effects between the objective (victim) and the aggressor wires. To avoid excessive pessimism, the substrate plane is treated as the current return path when extracting *RLMC*. The extracted *RLC* and *RLMC* form ladders so that the unit length is sufficiently small compared to the wave length derived by the significant frequency f_s [2, 4]. It is expressed as the function of the signal rising time t_r and the signal falling time (Eq. (1)). The driver size is determined so that the transition at the receiver becomes t_r and t_f .

$$f_s = \max\left(\frac{0.35}{t_r}, \frac{0.35}{t_f}\right) \quad (1)$$

2.2 Response surface function generation

After differences between *RLC* and *RLMC* delays are estimated for the parameter variation, the screening equations are built using response surface methods (RSM)

Table I. Predictor variables x_i to predict the difference between RLMC and RLC delays.

Variable	Explanation
S_{min}/S	Reciprocal of wire spacing normalized by the minimum.
W/W_{min}	Wire width normalized by the minimum.
l/l_{min}	Wire length normalized by the minimum.
D_{min}/D	Reciprocal of distance from the aggressor norm. by the pitch.

Table II. Interconnect parameter and constant for 14 nm node.

Parameter, Constant	Unit	Variation
Relative dielectric constant	-	2.375
Wire sheet resistance	Ω/\square	5.08
Wire thickness t	nm	89
Wire height h	nm	1015.8
Wire spacing S	$S_{min} = 38$ nm	$\times 5, \times 10, \times 20, \times 40, \times 80$
Wire width W	$W_{min} = 38$ nm	$\times 5, \times 10, \times 20, \times 40, \times 80$
Wire length l	$l_{min} = 10$ μ m	$\times 1, \times 2, \times 4, \times 8, \times 16$
Distance from aggressor D	$Pitch = W + S$	$\times 1, \times 3, \times 5$

[12]. We build response surface functions (RSF) expressed as Eq. (2), based on the physical dimension parameters. $f()$ stands for fourth order polynomials separated by cases where the aggressor and the victim transition in the same (even), and the opposite (odd) directions.

$$RSF = f(x_1, x_2, \dots, x_i, \dots, x_n) + \epsilon \quad (2)$$

In Eq. (2), x_i denotes predictor variables which predicts the difference between RLMC and RLC delays, and ϵ expresses residual error in the prediction. In detail, referring the amount of mutual inductance [9, 10] as well as the relative ratio of reactance [13], we define the RSF as the fourth order polynomial functions of the predictor variables shown in Table I.

It contributes to estimate impact of the mutual inductance in floor-planning, or physical design phases.

3 Quantitative evaluation of the screening method in a 14 nm FinFET process

Based on the parameters in International Technology Roadmap for Semiconductors (ITRS) [14] along with Predictive Technology Model (PTM) [15], the interconnect structure with buffers and receivers for high-performance SoC are defined as shown in Table II.

We apply the proposed method to the 14 nm technology node to evaluate prediction of the mutual inductance effects. Size of the drivers and the receivers is $\times 64$ of the unit size [16] so that t_r and t_f becomes 10 ps., where the operating frequency is targeted at 10 GHz and the significant frequency f_s is 35 GHz. The corresponding wavelength is 3.6 mm. According to a preliminary experiment, domain of the horizontal dimension parameters are decided so that the maximum relative delay difference exceeds 5%. Since the wire length is below a quarter of the

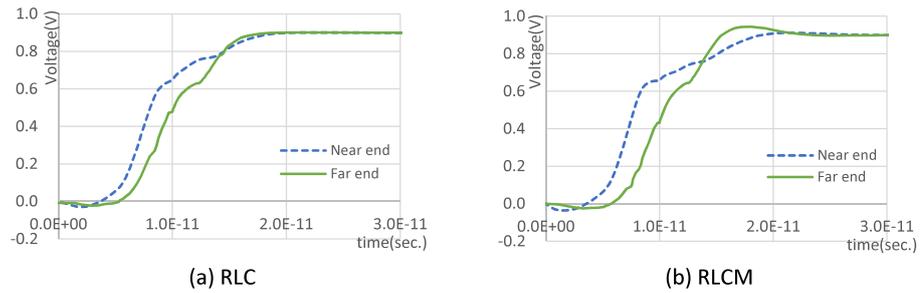


Fig. 2. Simulated signal propagation with and without mutual inductance. (l : $\times 16$, W : $\times 80$, S : $\times 5$, D : $\times 1$, Even)

wavelength, we apply a FEM based 2.5D field solver [17]. Fig. 2 compares RLC and RLCM waveforms when both the victim and the aggressor signals transition in the same direction (even). We separate the opposite transition from the even case because the mutual inductance effects act reversely for these two cases. Here, the self inductance varies from 0.47 nH/mm to 0.96 nH/mm, whereas the mutual inductance between the adjacent interconnects varies from 0.11 nH/mm to 0.52 nH/mm.

Fig. 3 shows the RLC delay estimation errors compared to the RLCM delays with the corresponding predictions using the RSFs. The degree of freedom adjusted coefficient of determination (R^2) exceeds 0.9, which indicates that the prediction has good fit [12].

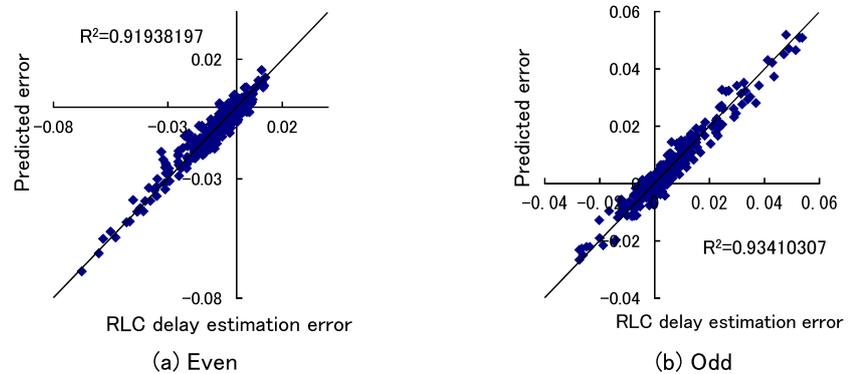


Fig. 3. Prediction accuracy of the delay estimation without mutual inductance.

Fig. 4 depicts wire width and spacing dependence of the mutual inductance effect. The wire length is fixed to 160 μm here. We can read that the impact of the mutual inductance increases with the wire width. It exceeds 5% when the wire width is larger than 35 times of the minimum width. Contrary, wire spacing mitigates the impacts. Even when the wire width is larger than 35 times, we can suppress the impact within 5% by making the wire spacing wider than 20 times of the minimum spacing. Fig. 5 shows that the distance from the aggressor wire also reduces the impacts. In terms of length, longer wires result in larger impacts as shown in Fig. 6. In this case, the RLC modeled delay cause 5% or larger errors with 100 μm or longer wires.

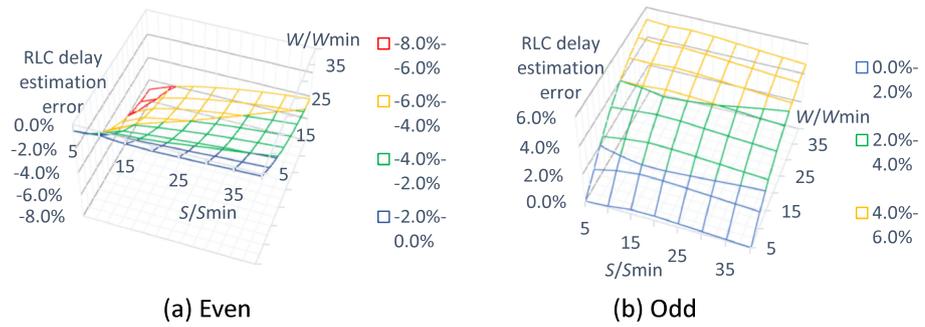


Fig. 4. Impact dependence on wire width and spacing. ($l: \times 16, D: \times 1$)

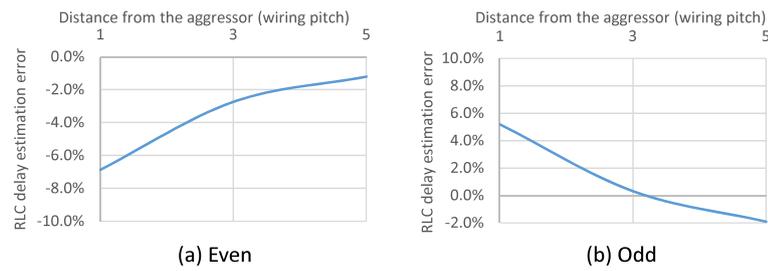


Fig. 5. Impact dependence on distance from the aggressor. ($l: \times 16, W: \times 80, S: \times 5$)

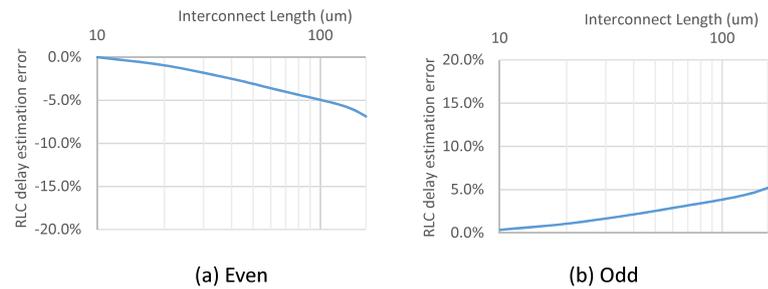


Fig. 6. Impact dependence on wire length. ($W: \times 80, S: \times 5, D: \times 5$)

4 Conclusion

This paper studied the impact of mutual inductance on interconnect signal delay estimation in a nano-scale system on a chip (SoC), suggesting a method to dimensionally predict and then screen the impact. The proposed methodology first calculates the delay difference between *RLC* and *RLMC* wire models for a set of parameter variations, then builds RSFs using dimensional parameters including wire width and spacing. The proposed method helps to avoid mutual inductance effects by pointing out interconnects which require *RLMC* delay models, as well as to correct the estimated delay using *RLC* models.