

# A 24 GHz enhanced neutralized cascode LNA with 4.7 dB NF and 19.8 dB gain

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**Abstract:** This paper presents a two-stage low noise amplifier (LNA) for 24 GHz automotive radar applications. Compared with traditional common source (CS) stage, the neutralized topology is used to improve the gain and reverse isolation in the first stage. In the second stage, an enhanced neutralized technique is adopted to improve the gain further. The LNA is fabricated by using standard 180-nm CMOS technology and occupies a chip area of  $1.0 \times 0.8 \text{ mm}^2$ . The design realizes a gain of 19.8 dB, a noise figure (NF) of 4.7 dB and an input 1 dB compression point ( $\text{IP}_{1\text{dB}}$ ) of  $-12 \text{ dBm}$ .

**Keywords:** LNA, CMOS, cross-coupled

**Classification:** Microwave and millimeter-wave devices, circuits, and modules

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## 1 Introduction

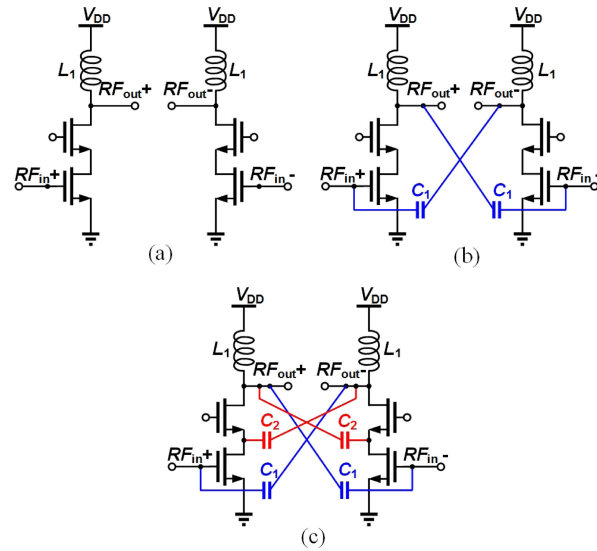
Recently, the wireless system has attracted tremendous attentions from both academia and industry for its huge potential in 24 GHz and 77 GHz automotive radar applications. The LNA is one of the key components in a communication system because it mainly determines the noise performance of the receiver chain. The common source stage is widely used in LNA designs for its high gain and low noise [1, 2, 3]. To improve the gain and counteract the Miller effect, cross-coupled capacitors are always added in the CS stage [1, 4]. Another way of using capacitors which are called gm-boosted technique is introduced in [5]. Nevertheless, the capacitors usually have large size and the low quality factor at high frequency, which may degrade the gain and noise performance. In [6], the gm-boosted technique realized by using transformer is proposed. However, the transformer occupies additional expensive chip area at 24 GHz. In this paper, a LNA using enhanced neutralized cascode structure is proposed. It has a higher gain compared to conventional neutralized structures. Circuit design and measurement results are introduced as follows.

## 2 Circuit design

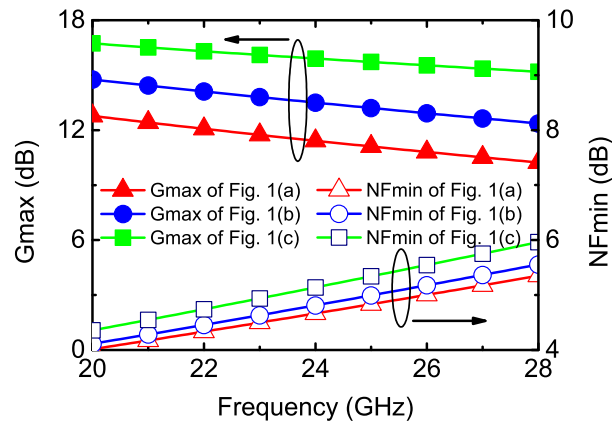
Fig. 1 shows several LNA topologies. Conventional cascode stage is shown in Fig. 1(a). Neutralized cascode stage with cross-coupled capacitors is shown in Fig. 1(b). The cross-coupled capacitors are employed in the cascode to counteract the parasitic capacitors between the gate and the drain to enhance the gain. The enhanced neutralized cascode structure is shown in Fig. 1(c). Compared with Fig. 1(b), another pair of cross-coupled capacitors is added between the source and the drain of the common gate transistor in the cascode stage. The  $G_{max}$  and  $NF_{min}$  of these three structures from 20 GHz to 28 GHz are shown in Fig. 2. It can be found that the  $G_{max}$  of the proposed structure is about 5 dB higher than the conventional one while the  $NF_{min}$  is 0.5 dB higher simultaneously. As the gain is higher than 10 dB, the increased noise will not degrade the noise performance of the system. The NF of the receiver ( $NF_{RX}$ ) can be calculated as

$$NF_{RX} = NF_1 + (NF_2 - 1)/G_1 + (NF_{mix} - 1)/(G_1 G_2), \quad (1)$$

where  $NF_1$ ,  $NF_2$ , and  $NF_{mix}$  are the NF of the first stage, second stage of LNA and zero-IF mixer.  $G_1$  and  $G_2$  are the small signal gain of the first stage and second stage of LNA. When the  $NF_{mix}$  is assumed as 10 dB, the  $NF_{RX}$  is 4.4 dB and 4.2 dB for the traditional and enhanced neutralized cascode, respectively. Though the NF



**Fig. 1.** (a) Conventional cascode stage; (b) Neutralized cascode stage; (c) Enhanced neutralized cascode stage.



**Fig. 2.**  $G_{max}$  and  $NF_{min}$  of three cascode structures.

of the proposed topology is 0.5 dB higher, it can reduce the  $NF_{RX}$  by 0.2 dB due to the higher gain.

The schematic of the proposed two-stage LNA is shown in Fig. 3. An input balun is used to convert the single-ended signal to differential signal and constitutes the input impedance matching network with the help of two series connected inductors. To design the balun accurately and fast, the equivalent circuit model on [7] is utilized in the simulation process. For the first stage, the CS structure is implemented to ensure enough gain and low NF. The cross-coupled capacitors are added to cancel the parasitic capacitance  $C_{gd}$  of the transistor  $M_1$  to deliver the higher gain and better differential stability. Due to the limitation of 180-nm CMOS, the maximum available gain of the transistor at 24 GHz is smaller than 8 dB. Therefore, in order to meet the gain requirement, the enhanced neutralized cascode structure is adopted in the second stage.

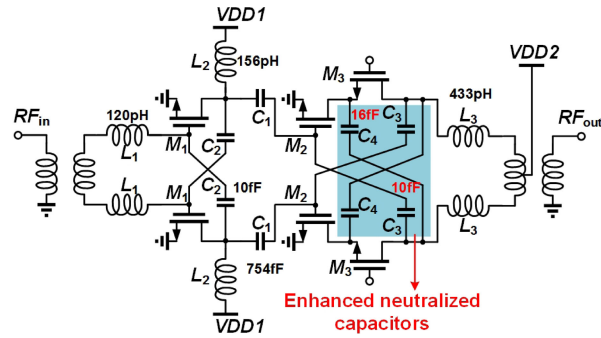


Fig. 3. Schematic of the proposed 24 GHz LNA (biasing not shown).

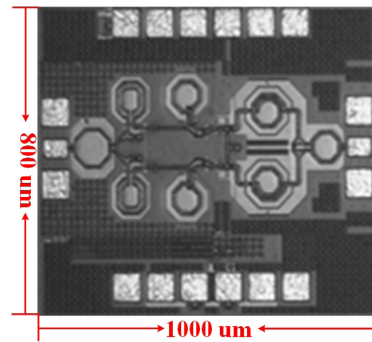


Fig. 4. Die photo of the proposed 24 GHz LNA.

### 3 Measurement results

The proposed LNA is fabricated in a 180-nm standard CMOS process. The chip as shown in Fig. 4 has a die size of 1.0 mm × 0.8 mm. The measured and simulated small signal gain (S21) and NF are shown in Fig. 5. The peak gain is about 19.8 dB at 23 GHz and the S21 is 19.34 dB at 24 GHz. The proposed LNA has a 3-dB bandwidth of 3.1 GHz from 22.1 GHz to 25.2 GHz. The minimum NF is 4.6 dB at 23.5 GHz while the NF is about 4.7 dB at 24 GHz. In Fig. 6, the simulated and measured S11 and S22 are compared from 22 GHz to 26 GHz. The measured S11 is below −10 dB from 22.5 GHz to 26 GHz and S22 is smaller than −9 dB, respectively. The measured power gain is plotted versus input power in Fig. 7, from which an  $IP_{1dB}$  of −12 dBm at 24 GHz can be extracted. The power consumption is 48 mW with supply voltages of 1.8 V and 2.4 V.

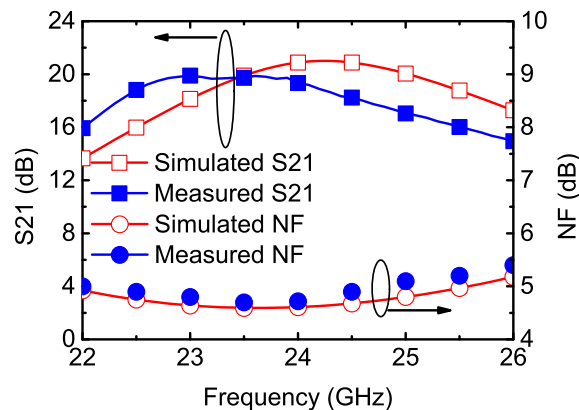


Fig. 5. The S21 and NF of the proposed 24 GHz LNA.

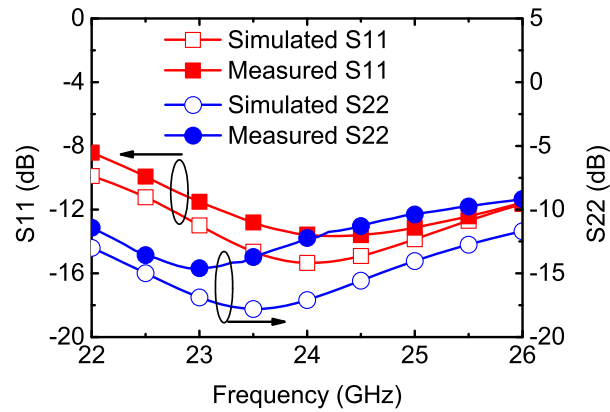


Fig. 6. The S11 and S22 of the proposed 24 GHz LNA.

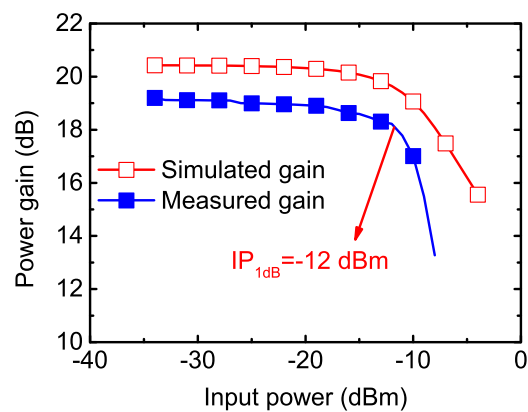


Fig. 7. The power gain varying with input power.

The performance of the proposed LNA is summarized in Table I together with the performance characterizations of other reported CMOS LNAs. Compared with the others, this work demonstrates the highest peak gain due to the help of the enhanced neutralized topology. The NF of this design is a little higher because it includes the 1.2 dB loss of the input balun compared with others.

Table I. Comparison Table

	This	[8]*	[9]	[10]	[11]
Topology	2 diff.	3 single.	2 single.	1 single.	1 single.
Tech. (nm)	180	180	180	65	180
Freq. (GHz)	24	24	24	24	21.8
Gain (dB)	19.8	10.76	13.7	14.3	15
NF (dB)	4.7	4.18	3.8	2.8	6
IP <sub>1dB</sub> (dBm)	-12	-	-8	-15	-
P <sub>dc</sub> (mW)	48	1.09	18	7	24
Area (mm <sup>2</sup> )	0.8	-	0.2756	-	0.05**

\*Simulated

\*\*Core Area

#### 4 Conclusion

A 24 GHz two-stage differential LNA is proposed and fabricated in standard 180-nm CMOS. As the frequency increases to tens of gigahertz, the gain of the transistors is limited. In this paper, an enhanced neutralized cascode LNA with double cross-coupled capacitors is proposed. Take good advantages of enhanced neutralized cascode structure, a differential LNA with a gain of 19.8 dB and a NF of 4.7 dB is realized.

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