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Broadband high-efficiency Doherty power amplifier based on novel phase and impedance transform structure

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Abstract: Traditional Doherty power amplifiers (DPAs) have severely limited bandwidth due to the presence of a quarter wavelength ($\lambda/4$) compensation microwave line. This paper proposes a novel phase compensation and impedance transform structure that can maintain a 90-degree phase shift over a wide frequency range, which is a good alternative to traditional $\lambda/4$ microwave line. To verify the validity of the proposed structure, a DPA has been designed and fabricated based on the proposed structure. The saturated output power reaches 43 dBm, and the output efficiency of the drain stage is more than 65% from 2.6 GHz to 3.8 GHz. Meanwhile, over 43% drain efficiency is obtained at 6 dB back-off power.

Keywords: $\lambda/4$ microstrip line, broadband, high efficiency, phase compensation, impedance transformation

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

With the rapid development of wireless communication, the large peak to average power ratios (PAPR) of the transmitted signal is increasing. Doherty power amplifiers (DPAs) have recently become a research focus due to their high back-off efficiency just because traditional power amplifiers have poor efficiency at back-off power [1]. However, the traditional DPAs require $\lambda/4$ compensation microstrip lines to accomplish the phase compensation and impedance conversion [2]. Unfortunately, it is well known that $\lambda/4$ microstrip line have narrow band characteristic, which severely limits the bandwidth of DPAs [3]. This bandwidth limitation is inconsistent with the broadband requirements of future communications. Therefore, many methods have been reported to improve the bandwidth of DPAs [4, 5, 6]. In [4], a low-pass topology has been adopted to absorb the transistor output capacitance, which results in improving the bandwidth significantly. The post matching DPA topology has been proposed in [5], which replaced $\lambda/4$ inverter by the Chebyshev impedance inverter to extend the bandwidth of a DPA. In [6], an 87% fractional bandwidth DPA has been designed by adopting a simplified bandwidth estimation method. S. Chen et al. add a short-circuited $\lambda/4$ microstrip line to constitute a novel compact output combiner, which leads to enhance bandwidth for the whole DPA [7]. In this paper, a novel phase compensation and impedance transform structure is proposed using anti-coupled lines and open circuit stub, which has a stable 90-degree phase shift characteristic over a wide frequency range. A bandwidth enhanced DPA is designed and fabricated based on the proposed phase compensation and impedance transform structure which replaces the $\lambda/4$ microstrip line as well. The measurement results fully validate the effectiveness of the proposed structure.

2 Theoretical analysis

A traditional $\lambda/4$ microstrip line can only maintain a stable 90-degree phase shift

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and impedance transformation in a narrow band, which is unfavorable for designing a wideband power amplifier. In order to expand the bandwidth of DPA, a novel phase compensation and impedance transform structure proposed in this paper is shown in Fig. 1. It is composed of a pair of anti-coupled lines loaded with an open circuit stub to make it have good broadband characteristics. Then, the new structure will be analyzed theoretically and the scattering parameter matrix of the structure will be derived. From Fig. 1, it can be seen that the proposed structure is standardized symmetry. According to the odd-even mode analysis method of a symmetrical two-port network, the symmetrical interface can divide the structure into two identical parts. When performing even-mode excitation, the equivalent circuit is shown in Fig. 2(a). Similarly, when performing odd-mode excitation, an one-port odd-mode network under odd-mode excitation can be obtained, and its equivalent circuit is shown in Fig. 2(b).

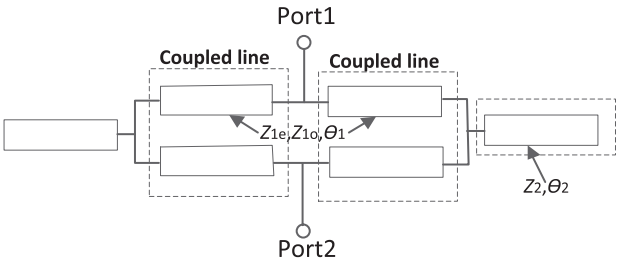
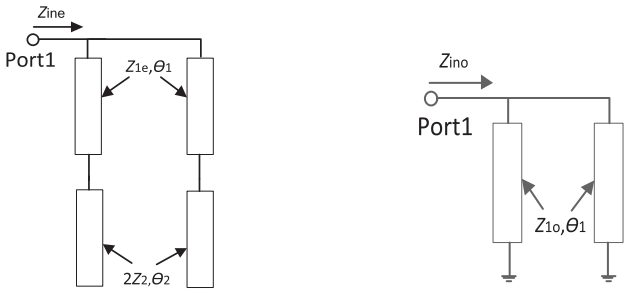


Fig. 1. Proposed phase compensation and structure



(a) (b)

Fig. 2. The equivalent circuit of the proposed structure for: (a) even-mode equivalent circuit and (b) odd-mode equivalent circuit

As shown in Fig. 2, Z_{ine} and Z_{ino} represent the even-mode and odd-mode input impedance respectively. $Z_{1\text{e}}$ and $Z_{1\text{o}}$ represent the even-mode and odd-mode impedance of the coupled line and θ_1 is the electrical length of the coupled line. Z_2 and θ_2 represent the characteristic impedance and the electrical length of the open circuit stub respectively. According to ideal transmission line theory, the even-mode input impedance is given by

$$Z_{\text{ine}} = \frac{jZ_{1\text{e}}(Z_{1e}\tan\theta_1\tan\theta_2 - 2Z_2)}{Z_{1e}\tan\theta_2\tan\theta_2 + 2Z_2\tan\theta_1} \tag{1}$$

and the odd-mode input impedance can be calculated as

$$Z_{\text{ino}} = jZ_{1\text{o}}\tan\theta_1 \tag{2}$$

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Then, the relationship between input impedance and scattering parameters in the network are written as follows

$$S_{11k} = \frac{Z_{ink} - Z_0}{Z_{ink} + Z_0}, \quad k = o, e \tag{3}$$

$$S_{11} = \frac{S_{11e} + S_{11o}}{2}, \quad S_{21} = \frac{S_{11e} - S_{11o}}{2} \tag{4}$$

Therefore, using (1) (2) (3) and (4), the S11 and S21 can be derived as

$$S_{11} = \frac{[(2Z_{1e}Z_{1o}Z_2 - 2Z_0^2Z_2)\sin\theta_1\cos\theta_1\cos\theta_2 - Z_{1e}Z_{1e}Z_{1o}\sin^2\theta_1\sin\theta_2 - Z_0^2Z_{1e}\cos^2\theta_1\sin\theta_2]}{jZ_0\left\{\begin{array}{l}[(Z_{1e}Z_{1e} + Z_{1e}Z_{1o})\sin\theta_1\cos\theta_1\sin\theta_2 + 2Z_{1o}Z_2\sin^2\theta_1\cos\theta_2 - 2Z_{1e}Z_2\cos^2\theta_1\cos\theta_2] + \\ [(2Z_{1e}Z_{1o}Z_2 + 2Z_0^2Z_2)\sin\theta_1\cos\theta_1\cos\theta_2 + Z_0^2Z_{1e}\cos^2\theta_1\sin\theta_2 - Z_{1e}Z_{1e}Z_{1o}\sin^2\theta_1\sin\theta_2]\end{array}\right\}} \tag{5}$$

$$S_{21} = \frac{jZ_0[(Z_{1e}Z_{1e} - Z_{1e}Z_{1o})\sin\theta_1\cos\theta_1\sin\theta_2 - 2Z_{1o}Z_2Z_{1o}\sin^2\theta_1\cos\theta_2 - 2Z_{1e}Z_2\cos^2\theta_1\cos\theta_2]}{jZ_0\left\{\begin{array}{l}[(Z_{1e}Z_{1e} + Z_{1e}Z_{1o})\sin\theta_1\cos\theta_1\sin\theta_2 + 2Z_{1o}Z_2\sin^2\theta_1\cos\theta_2 - 2Z_{1e}Z_2\cos^2\theta_1\cos\theta_2] + \\ [(2Z_{1e}Z_{1o}Z_2 + 2Z_0^2Z_2)\sin\theta_1\cos\theta_1\cos\theta_2 + Z_0^2Z_{1e}\cos^2\theta_1\sin\theta_2 - Z_{1e}Z_{1e}Z_{1o}\sin^2\theta_1\sin\theta_2]\end{array}\right\}} \tag{6}$$

where Z_0 is the characteristic impedance of coupling line.

Assuming that C is the coupling coefficient of the microstrip coupling line, it can be written as

$$C = (Z_{1e}/Z_{1o} - 1)/(Z_{1e}/Z_{1o} + 1) \tag{7}$$

Hence, the relationship among the odd-even mode impedance, the coupling coefficient and the characteristic impedance of the coupling line can be expressed as

$$Z_{0e} = Z_0\sqrt{\frac{1+C}{1-C}}, \quad Z_{0o} = Z_0\sqrt{\frac{1-C}{1+C}} \tag{8}$$

It is required that $\theta_1 = \theta_2 = 45°$ for the 90-degree of phase shift. Then (6) can be simplified to as following

$$\mathrm{S21} = 0.5 * \left[\left(\frac{\sqrt{1+C} - 3\sqrt{1-C}}{\sqrt{1-C} + \sqrt{1+C}}\right) - \frac{j * 4Z_2}{2Z_2 + Z_0 * \sqrt{1+C}/\sqrt{1-C}}\right] \tag{9}$$

The relationship between the phase shift and the impedance of the coupling line, the coupling coefficient and the impedance of the open short intercept line are shown in Fig. 3. It is can be found that when the coupling coefficient C is 0.7, the corresponding phase is near 90°. According to the relationship diagram shown in Fig. 3, in this paper, a new structure with characteristic impedance of 50 Ω and 90° phase shifting is designed which contain coupling line with coupling coefficient 0.7 and characteristic impedance 50 Ω and open circuit stub impedance 100 Ω.

Fig. 4 is the simulation results of transmission phase of the new structure. It is clear that the structure has an excellent broadband characteristic compared with $\lambda/4$ microstrip line. The phase transformation is ±4°. And the insertion loss of this structure is less than 2 dB. In addition, the structure has strong suppression ability for the 2, 3 harmonics, which is well beneficial to improve the linearity of the power amplifier.

3 Doherty power amplifier design and measurement

Based on the proposed novel phase compensation and impedance conversion

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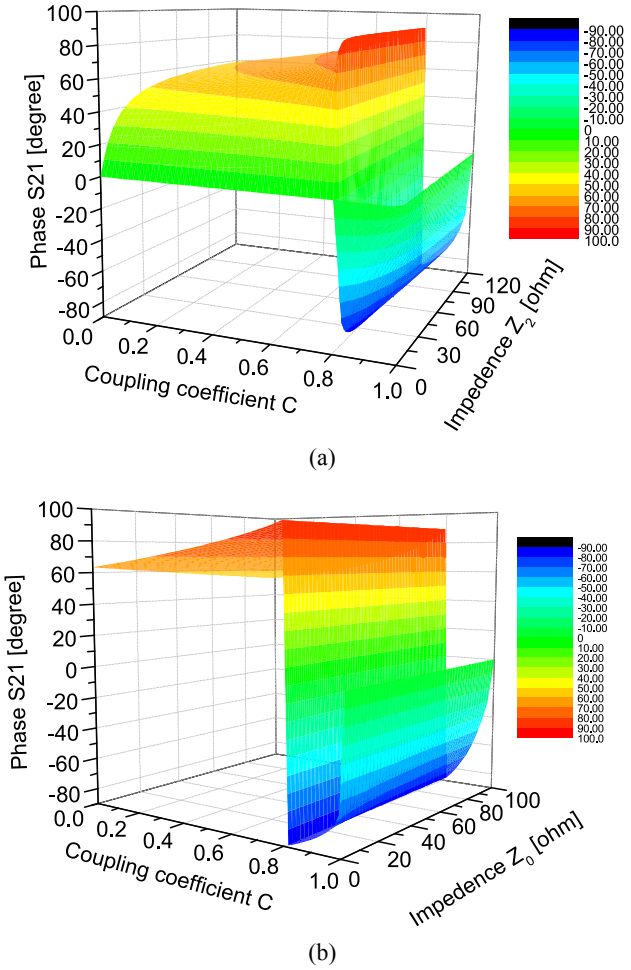

Fig. 3. (a) Relationship between the phase shift and impedance of the coupling line
(b) Relationship between the coupling coefficient and impedance of the open short intercept line

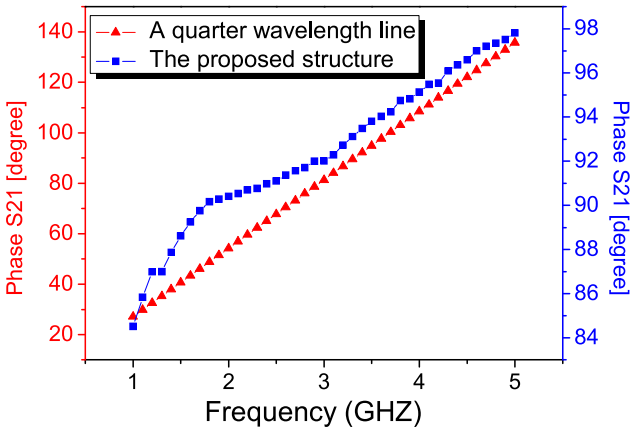

Fig. 4. Simulation of transmission phase of the new structure

structure, a bandwidth enhanced high efficiency DPA is designed using CREE's CGH40010F GaN transistor, which is symmetrical configuration. The main amplifier working at class AB state and the auxiliary amplifier working at class C state. And the drain voltage is 28 V, the main power amplifier and the auxiliary power

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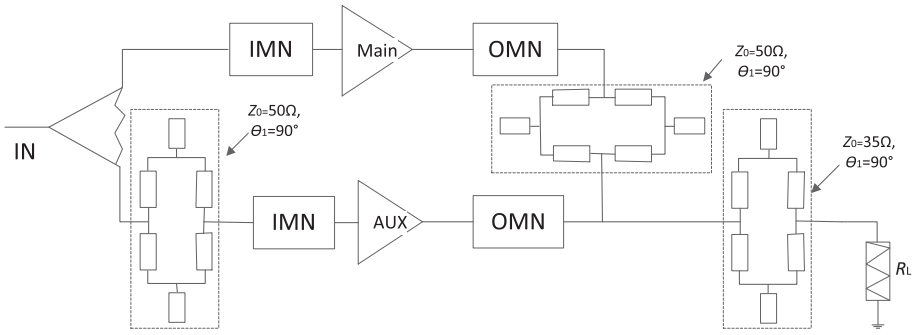

Fig. 5. Designed DPA topology diagram

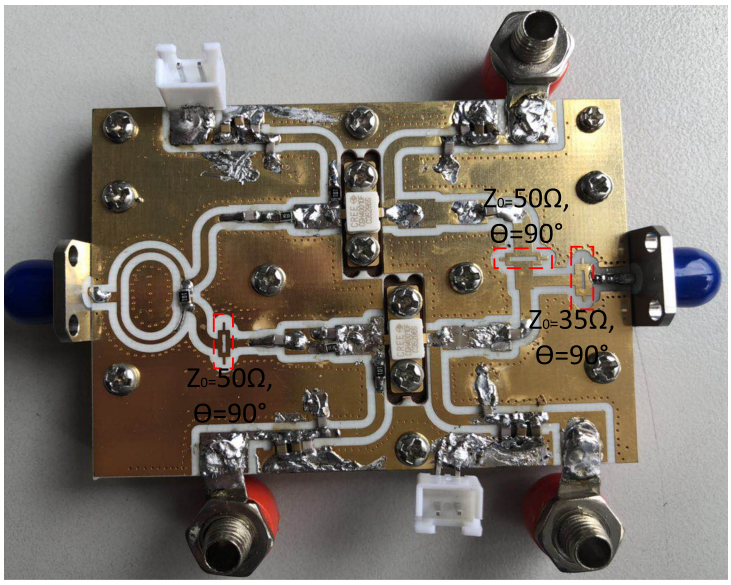

Fig. 6. Photograph of the fabricated DPA

amplifier's gate bias are −3 V and −5.5 V respectively. The specific DPA topology is shown in Fig. 5, which replaces the $\lambda/4$ microstrip line in traditional DPA with the proposed structure. And the broadband DPA is implemented on substrate Rogers 4350B with a dielectric constant of 3.66 and a thickness of 0.508 mm, as shown in Fig. 6.

It is necessary to incorporate the bias circuit into the matching circuit when performing output matching, which can effectively prevent power leakage and maintain good broadband characteristics, since a wideband circuit is designed. In addition, in order to reduce the influence of parasitic parameters of package on the overall performance of the power amplifier as much as possible, the parasitic model equivalent model [8] of CGH40010F is embedded in the output matching of the carrier power amplifier and peak power amplifier. The matching circuit is a multi-level low-pass matching structure. This matching method is suitable for designing a wideband circuit. The power amplifier is designed to be symmetrical structure by applying the 1:1 Wilkinson power divider with broadband characteristics.

Fig. 7 shows the output power simulation and measurement results of the proposed DPA. It can be seen that the saturated output power level of the DPA is flat and reaches 43 dBm in 2.6–3.8 GHz. Fig. 8 shows the power amplifier's drain efficiency simulation and measurement results. The saturated drain efficiency

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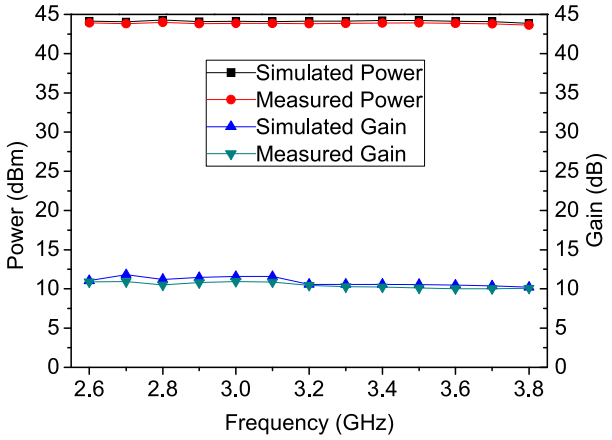

Fig. 7. The simulated and measured results of the saturated power and gain of the proposed DPA

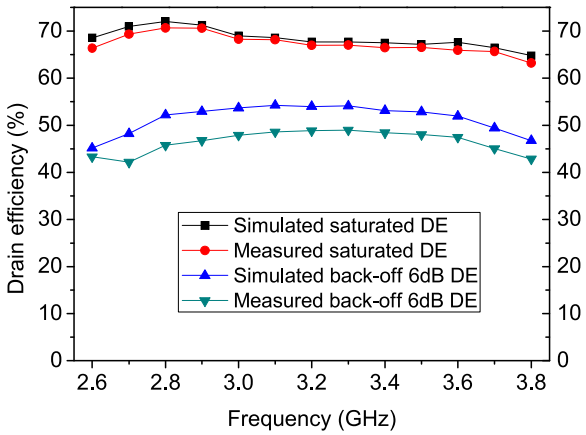

Fig. 8. The DPA drain efficiency simulation and measurement results

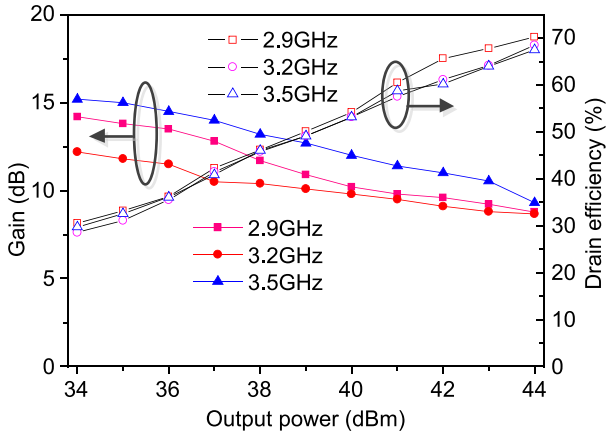

Fig. 9. Measured drain efficiencies and gain profiles versus output power

reaches 64.5% in the range 2.6–3.8 GHz. And the efficiency is greater than 43% at 6 dB back-off power. The measured drain efficiency and gain curves versus the output power at 2.9, 3.2, and 3.5 GHz are depicted in Fig. 9. It can be observed that the fabricated DPA approximately follows the classic Doherty type efficiency profiles at the measured frequencies.

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Table I. Performance comparison with DPAs

Ref	Frequency (GHz)	Power (dBm)	Saturation DE (%)	Back-off 6 dB DE (%)
[5]	1.7–2.6	44–46.3	57–66	47–57
[6]	1.5–2.5	42.5–44	55–72	42–43
[9]	2.0–2.7	40.5–42	58–70	36–65
[10]	1.05–2.55	40–42	45–83	35–58
[11]	1.6–2.6	41.7–43	50.8–54	41.5–45
This work	2.6–3.8	43.07–43.53	64.6–70	43–46

Table I is a comparison of the performance of Doherty power amplifiers reported in this article and some recent works. [5] has a higher back-off efficiency and power but poorer saturation efficiency and bandwidth compared with the proposed DPA. The proposed DPA has wider bandwidth compared with other works except [10], which has poorer power. It can be clearly observed that the proposed DPA takes into account various aspects of the indicators such as bandwidth, power and efficiency so that better practical applications can be achieved.

4 Conclusion

This paper proposes a novel phase and impedance transform structure which replaces the traditional $\lambda/4$ microstrip line limiting the bandwidth of DPA. A bandwidth enhanced DPA using the proposed novel structure is implemented. Meanwhile, the multi-level low-pass matching method and parasitic model of transistor have been applied to design a wideband matching circuit.

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