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Temperature-dependent characterizations on parasitic capacitance of tapered through silicon via (T-TSV)

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Abstract: With increasing integration density of three-dimensional ICs, temperature is one of the major concern of circuit design, which influences the performance and reliability. In this paper, the parasitic capacitance of tapered TSV (T-TSV) with respect of thermal properties is studied. The concept of the Temperature Coefficient of Capacitance (*TCC*) is proposed to model the sensitive of TSV capacitance to temperature. It is found that TSV capacitance is sensitive to temperature under high frequency application, and the MOS capacitance variation is the main reason for the change of TSV capacitance and the *TCC* increases with elevated temperature. Furthermore, the affection of TSV dimensions on *TCC* are discussed. It is shown that the *TCC* increases gradually as the TSV radius increases, while the thickness of dielectric layer is the opposite. The cylinder TSV is less thermal sensitive than tapered TSV. This paper provides basis for TSV design considering the temperature effect.

Keywords: three-dimensional ICs (3D ICs), tapered through silicon via (T-TSV), temperature effect, parasitic capacitance

Classification: Electron devices, circuits and modules

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1 Introduction

For the past few years, three-dimensional ICs (3D ICs) are architectural innovations for integrated circuits which provide an effective solution for improving packing density, reducing power consumption and achieving faster speed [1, 2, 3, 4, 5]. In 3D ICs, through silicon via (TSV) is the core component which providing a interconnection among the stacking dies vertically. The electrical model in terms of parasitic resistance, capacitance and inductance are important because the circuit overall performances can be estimated by combing models. There are already many models (tapered, cylindrical, annular, and coaxial TSVs) have been proposed to model the TSV electrical characterization [6, 7, 8, 9, 10, 11], however, most of the models did not consider the effect of temperature. Owing to the increasing integration density, a large amount of heat is generated during operating. Parasitic capacitance is one of the most important parasitic parameters of TSV under high frequency application. It is necessary to study the parasitic capacitance with varying temperature.

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In previous works, the temperature impact on noise coupling of TSV and high-speed TSV channel has been presented in [12]. A semi-analytical model of the TSV capacitance for elevated operating temperatures has been derived and verified with electrical measurements in [13]. It is found that the capacitance has insignificant changes and the capacitance hysteresis decreases with elevated temperatures of TSVs with BCB-liners in [14].

In this paper, the effect of temperature on T-TSV capacitance is studied. The concept of the *TCC* is proposed to model the sensitive of T-TSV capacitance to temperature. In addition, the *TCC* with various geometrical dimensions are analyzed.

2 Temperature coefficient of C_{tsv}

The cross-section and bottom view of a T-TSV are illustrated in Fig. 1, the TSV channel interconnects the top and bottle dies vertically. As shown in Fig. 1, an insulating layer surrounds the TSV metal to avoid the signal flows from the TSV conductor to the silicon substrate. Due to the insulating layer, there is an insulating capacitance C_{die} between TSV and substrate. In addition, a depletion capacitance C_{dep} exists because the MOS (Metal-Oxide-Semiconductor) structure. The capacitance of TSV (C_{tsv}) is equivalent to parallel of C_{dep} and C_{tsv}. Therefore, the C_{tsv} can be expressed by formula (1). The C_{die} and C_{dep} are given by [15], as shown in (2) and (3).

$$C_{tsv} = \frac{1}{\frac{1}{C_{die}} + \frac{1}{C_{dep}}} \tag{1}$$

$$C_{die} = \frac{2\pi\varepsilon_{die}h}{\sin(\alpha)\cdot\ln\left(\frac{2(R_{tsv}+t_{die})+h\cot(\alpha)}{2R_{tsv}+h\cot(\alpha)}\right)} \tag{2}$$

$$C_{dep} = \frac{2\pi\varepsilon_{si}h}{\sin(\alpha)\cdot\ln\left(\frac{2(R_{tsv}+t_{die}+w_{dep})+h\cot(\alpha)}{2(R_{tsv}+t_{die})+h\cot(\alpha)}\right)} \tag{3}$$

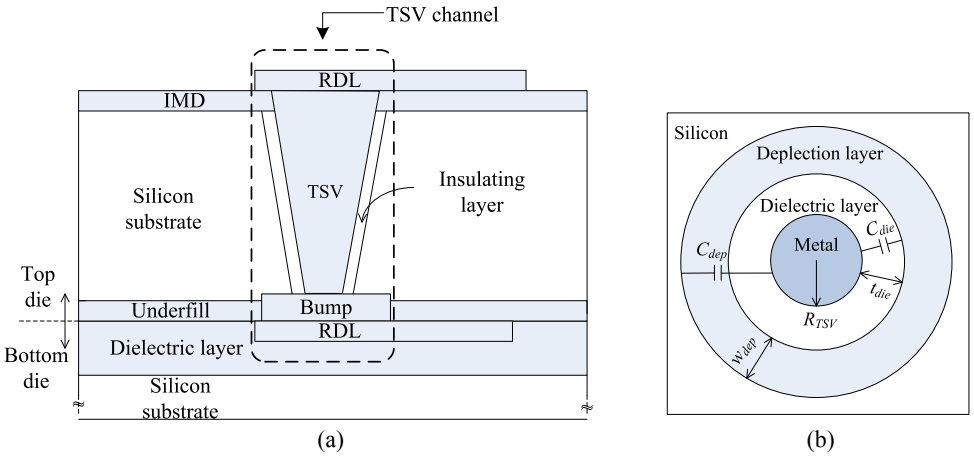

Fig. 1. Diagram of TSV structure (a) cross-sectional view (b) bottom view

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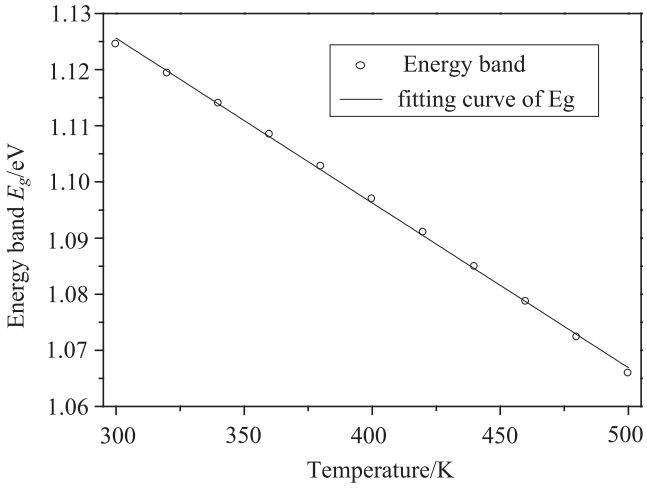

Fig. 2. Variation of energy band E_g on temperature

Where α is the slope angle of the wall, h is the height of TSV, R_{tsv} is the TSV bottom radius, t_{die} is the thickness of dielectric layer, w_{dep} is the depletion thickness. For high frequency signals, the minimum C_{tsv} is desired for the circuit performance, thus the TSV should operate in the maximum depletion w_{max}.

The expression of w_{max} and n_i are shown in (4) and (5). For silicon substrate, the energy band (E_g) can be regarded as a function of temperature, that is shown in (6). For the temperature variation of 300 K to 500 K, E_g is be fitted as a first order polynomial for T which is shown in (7) and Fig. 2. The β is -2.94×10^{-4} and the $E_g(0)$ is 1.21 eV. Thus the expression of n_i can be written as formula (8).

$$w_{\max} = \left[\frac{4\varepsilon_{si}k_0T}{q^2Na}\ln\left(\frac{Na}{n_i}\right)\right]^{1/2} \tag{4}$$

$$n_i = 4.82 \times 10^{15}\left(\frac{m_n{}^* m_p{}^*}{{m_0}^2}\right)^{3/4} T^{3/2}\exp\left[-\frac{Eg}{2k_0T}\right] \tag{5}$$

$$E_g = 1.17 - \frac{4.73 \times 10^{-4} \times T^2}{T + 636} \tag{6}$$

$$E_g = E_g(0) + \beta T \tag{7}$$

$$n_i = 4.82 \times 10^{15}\left(\frac{m_n{}^* m_p{}^*}{{m_0}^2}\right)^{3/4} T^{3/2}\exp\left(\frac{-\beta}{2k_0}\right)\exp\left[-\frac{Eg(0)}{2k_0T}\right] \tag{8}$$

Considering the substrate p-doping concentration N_a is 1.25×10^{15} cm^{-3}, the TSV radius R_{tsv} is 5 µm, the height is 50 µm, the dielectric thickness t_{die} is 0.1 µm, respectively. The minimum C_{tsv} with the T-TSV angle from 70° to 90° are shown in Fig. 3.

It can be seen that the temperature has significant impact on C_{tsv}, which shows a tendency of increase as the temperature goes up. When the temperature increases from 300 K to 500 K, the C_{tsv} increases from 0.457 pF to 0.691 pF for TSV angle is 70°, and from 0.294 pF to 0.35 pF for TSV angle is 80°. The increments are about 50% for all TSV geometrical dimensions.

Therefore, in order to model the sensitive of TSV capacitance to temperature, the concept of the *TCC* for a copper TSV is defined as (9–12).

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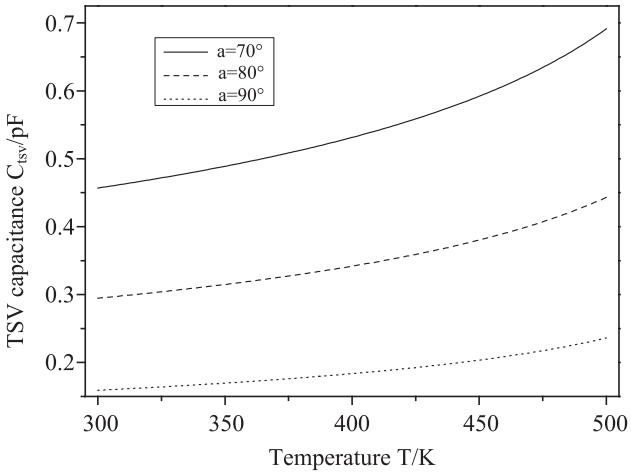

Fig. 3. Variation of C_{tsv} with temperature

$$TCC(\mathrm{T}^*) = \frac{\partial C_{TSV}/C_{TSV}}{\partial T}\bigg|\mathrm{T} = \mathrm{T}^* \tag{9}$$

$$TCC(\mathrm{T}^*) = \left(\frac{C_{die}}{C_{dep}\cdot(C_{die}+C_{dep})}\right)\cdot\frac{\partial C_{dep}}{\partial T} \tag{10}$$

$$\frac{\partial C_{dep}}{\partial T} = \frac{\partial C_{dep}}{\partial w_{\max}}\cdot\frac{\partial w_{\max}}{\partial T} \tag{11}$$

$$\frac{\partial C_{dep}}{\partial w_{\max}} = -\frac{2\pi\varepsilon_{si}h}{\sin(\alpha)}\cdot\frac{1}{R_{die}+w_{\max}+\cot(\alpha)h/2}\left[\ln\frac{2(R_{die}+w_{\max}+R_{die})+h\cot(\alpha)}{2R_{die}+h\cot(\alpha)}\right]^{-2} \tag{12}$$

Where $R_{die} = R_{TSV} + t_{die}$, the $\partial w_{\max}/\partial T$ can be derived from (4):

$$\frac{\partial w_{\max}}{\partial T} = \frac{1}{2}\left(\frac{4\pi\varepsilon_{si}k_0h}{q^2N_a}\right)^{-1/2}\left[T\cdot\ln\left(\frac{Na}{ni}\right)\right]^{-1/2}\left[\ln\left(\frac{Na}{ni}\right)-\frac{T}{n_i}\cdot\frac{\partial n_i}{\partial T}\right] \tag{13}$$

Where the $\partial n_i/\partial T$ can be derived from (8):

$$\frac{\partial n_i}{\partial T} = 4.82\times10^{15}\exp\left(-\frac{E_g(0)}{2k_0T}\right)\exp\left(-\frac{\beta}{2k_0}\right)\left(\frac{\mathrm{m_n}^*\mathrm{m_p}^*}{{m_0}^2}\right)^{3/4}\cdot\left(\frac{3}{2}T^{1/2}+\frac{1}{2}\frac{E_g(0)}{k_0}T^{-1/2}\right) \tag{14}$$

3 Temperature affections on *TCC*

For a fixed TSV geometrical dimension, it can be seen from formula (3) that the C_{dep} depends on w_{dep}, and the w_{dep} has strong relationship with temperature from Eq. (4)–(8). Submitting the R_{tsv} is 5 µm, t_{die} is 0.1 µm into Eq. (9)–(14), the dependence of *TCC* on temperature are shown in Fig. 4. It can be seen that the *TCC* increase gradually with elevated temperature. This can be explained by the following phenomenon.

Under high frequency application, the TSV operates at w_{max}, which leads to the fact that TSV capacitance mainly depends on C_{dep}. With the temperature increasing, the intrinsic carrier density n_i increases exponentially, therefore, the w_{max} decided by Eq. (4) decreased sharply with elevated operating temperatures. The C_{dep} capacitance in cylinder TSV likes the parallel plate capacitor which increases

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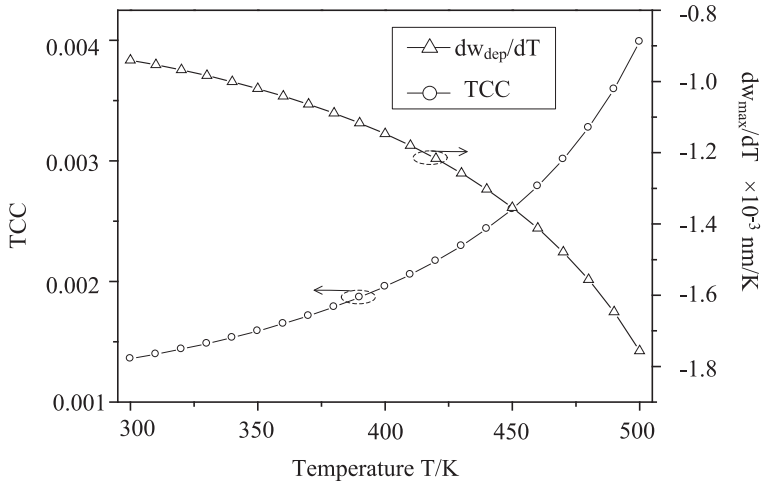

Fig. 4. Variation of *TCC* and $\partial w_{\max}/\partial T$ with temperature

sharply as the w_{max} decreases, the variation of $\partial w_{\max}/\partial T$ is shown in Fig. 4 on right axis. Therefore, the *TCC* increases with the elevated temperature.

4 TSV dimensions affections on *TCC*

Eq. (2)–(3) indicated that the TSV dimensions have effect on calculation of *TCC*. In order to research the effect of TSV dimensions on *TCC*, we fixed the operating temperature at 400 K, the variation of *TCC* and $\partial C_{tsv}/\partial T$ with TSV radius ranging from 1 to 10 µm and fixed dielectric layer thickness of 0.1 µm are shown in Fig. 5. It is shown that as the radius of TSV increase, the $\partial C_{tsv}/\partial T$ increases at a almost constant rate, the *TCC* increase rapidly at first and then beginning to stabilize when the radius of TSV is large enough. T-TSV degenerates to cylindrical TSV when α is 90°. It can be seen that the tapered TSV has obvious large *TCC* compared with cylindrical TSV. This suggests that the cylindrical TSV has more thermal stability. This is because, for the same radius and temperature, the increase of w_{dep} is uniform for per unit temperature, and the equivalent surface area of the tapered TSV is larger than the cylinder one, while capacitance value is proportional to its surface area, thus the cylinder has better temperature stability.

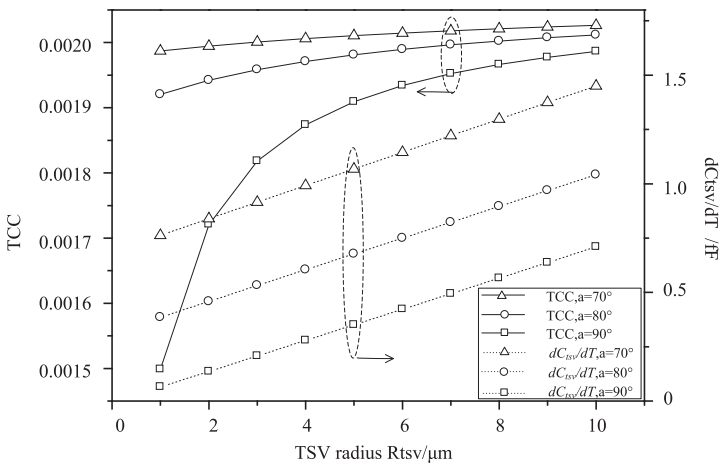

Fig. 5. Variation of *TCC* and $\partial C_{tsv}/\partial T$ with TSV radius

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Furthermore, we analysis the impact of dielectric layer thickness on *TCC*. The variation of *TCC* and $\partial C_{tsv}/\partial T$ with dielectric layer thickness ranging from 0.05 to 0.2 µm and fixed TSV radius of 5 µm are shown in Fig. 6 and Fig. 7. It can be seen that the *TCC* and $\partial C_{tsv}/\partial T$ decrease as the dielectric layer thickness increases. The TSV capacitance shows the same thermal stability tendency that cylindrical TSV is more stable. The discussion of TSV dimensions affections on *TCC* provides basis for TSV design considering the temperature effect.

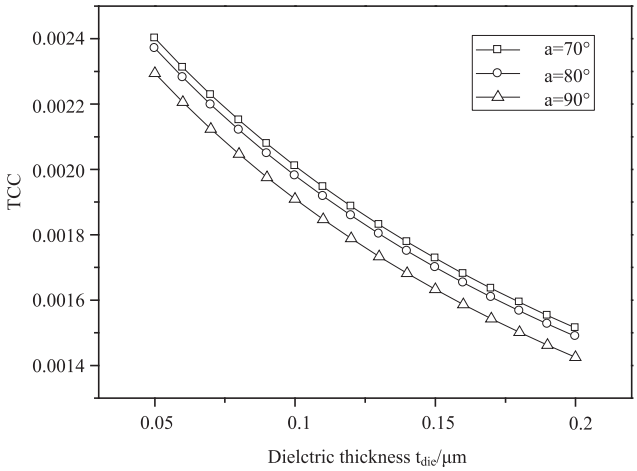

Fig. 6. Variation of *TCC* with dielectric layer thickness

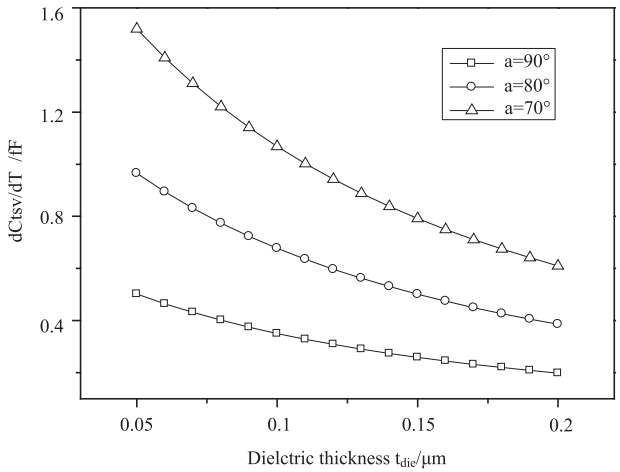

Fig. 7. Variation of $\partial C_{tsv}/\partial T$ with dielectric layer thickness

5 Conclusion and perspectives

Since the thermal management is perceived to be one of the major bottlenecks for the 3-D ICs, this paper studied the temperature effect on capacitance of TSV in high frequency by exploiting the concept of the Temperature Coefficient of Capacitance (*TCC*). The *TCC* is derived from semiconductor physics equation and taken the MOS capacitance into account. Further more, the temperature and TSV dimensions affections on *TCC* are discussed. It is found that temperature is the main influence factor, the *TCC* increase as the temperature goes up. The *TCC* increases gradually with the TSV radius increases, while the impact of dielectric layer is the opposite.

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Through the comparison of tapered TSV capacitance with different slope wall angle, it is shown than the cylinder TSV has more thermal stability.

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