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Study on scalability of hybrid junctionless FinFET and multi-stacked nanowire FET by TCAD simulation

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Abstract: This work studied the electrical characteristics of silicon-on-insulator (SOI) multi-stacked nanowire junctionless FET (NW-JL-FET) and SOI hybrid junctionless FinFET (H-JL-FET) using TCAD simulation. The scalability of the above two structures was investigated by simulating device performance with gate lengths from 30 nm to 5 nm. Results show that NW-JL-FET has better performance than that of H-JL-FET due to gate all around structure. However, H-JL-FET still has good performance under ultra-small gate length indicating FinFET still could be a competitor for 5 nm and beyond technique nodes.

Keywords: hybrid, junctionless, nanowire, simulation

Classification: Electron devices, circuits and modules

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1 Introduction

Fin field effect transistor (FinFET) is currently widely used in as low as 7 nm technique nodes in foundries. Various device structures are proposed to reduce the leakage current and improve device performance in order to push FinFET to smaller technique nodes. Among the multiple operation modes of FinFET, the junctionless (JL) mode has shown greater potential than the traditional inverted modes [1, 2]. A 3D stacked hybrid JL FinFET was recently put forward by [3, 4, 5] to combine the advantages of the traditional silicon-on-insulator (SOI) and bulk structures which has better performance than traditional FinFET for large gate length. However, the device structure for 5 nm and below technology node is not decided yet. Nanowire field effect transistor (NW-FET) has long been known for better gate controllability than FinFET due to its gate all around (GAA) structure. Recently, multi-stacked nanowire FET is fabricated which can provide large ON current [6, 7, 8]. However, complicated structure brings about a number of process issues which hinders entry of nanowire FET into industrial fabrications. The investigation of performance and operation mechanisms for FinFET and NW-FET is highly desired for academic and industrial purposes. In this work, two newly proposed FinFET and NW-FET structures were selected to investigate the scalability using TCAD simulation. The two structures are SOI multi-stacked nanowire junctionless FET (NW-JL-FET) and SOI hybrid junctionless FinFET (H-JL-FET) and their performances were studied with gate lengths from 30 nm to 5 nm.

2 Device structure and simulation approach

Figs. 1(a) and (b) show the schematic diagrams of two structures, in which both the height (FH) and width (FW) of the fin are 10 nm. Both structures use three-layer stacked structure to boost the output current of the device. Fig. 1(c) is the cross-section diagram of NW-JL-FET along AA′, cutting channel 1 to 3 (CH1–CH3)

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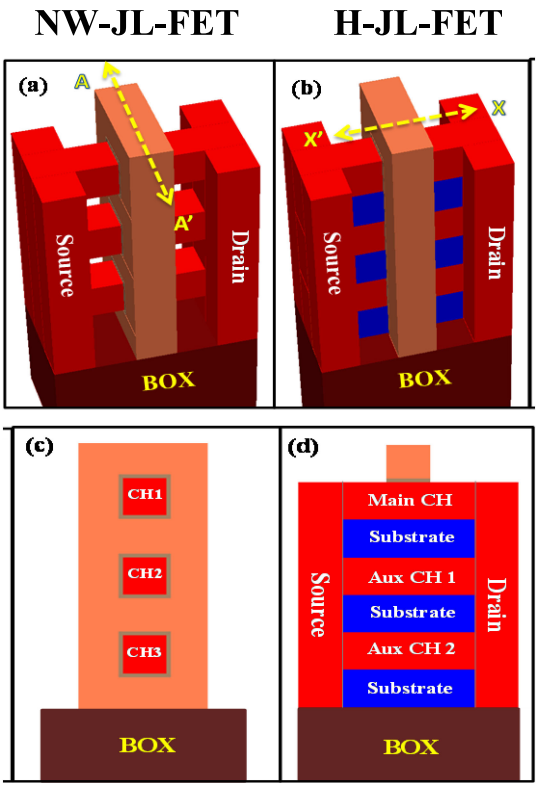

Fig. 1. Different structures of the JL-FETs including: (a) NW-JL-FET; (b) H-JL-FET structure; (c) cross sectional AA′ direction in the NW-JL-FET and (d) cross sectional XX′ direction in the H-JL-FET structure.

from the top to bottom. All the channels have GAA structure with the spacing of 10 nm. Fig. 1(d) is the cross-section diagram of H-JL-FET along XX′, cutting one main channel and two auxiliary channels (Aux-CH1 and Aux-CH2) from the top to the bottom. The substrates are used as the isolations between channels, and the sectional areas of channels and substrates are all 10 nm × 10 nm. The gate material for both structures is TiN and the gate dielectric material is HfO2 with the thickness (TOX) of 1 nm in this simulation. The work functions of n-FET and p-FET are fixed on 4.7 eV and 4.58 eV respectively. The n and p channel doping concentrations of NW-JL-FET and H-JL-FET are all fixed to 1019 cm-3. We used 3D Sentaurus TCAD to perform the simulation [9]. In addition to essential quantum effects, hydrodynamic (HD) model combined with density gradient (DG) model was used in the carrier transport model.

3 Results and discussion

Fig. 2 shows transfer I-V characteristic for H-JL-FET and NW-JL-FET with gate length of 10 nm. Due to better gate controllability of GAA structure, IOFF of NW-JL-FET is smaller than that of H-JL-FET. The ION of the two structures is comparable and the ION/IOFF are larger than 105 for both structures. It is worthwhile to note that IOFF of H-JL-FET is rather small which is in the order of 10-9A. Generally speaking, there are two kinds of substrate for a FinFET, that is, bulk and SOI. SOI FinFET possesses better IOFF but worse ION than bulk FinFET, therefore the ION/IOFF is not satisfied for both SOI and bulk FinFET. To combine

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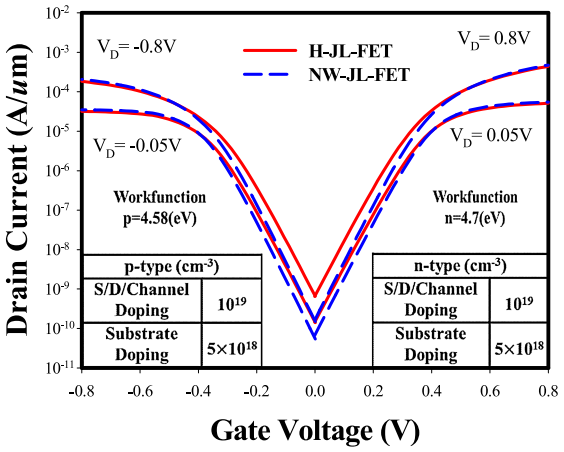

Fig. 2. I_D-V_G curves of the n-FET and p-FET, with a 10 nm gate length, and simulation parameters for the different structures.

the advantages of SOI and bulk structures, a doping layer used as substrate is inserted between SOI substrate and channel for a SOI FinFET, which forms the hybrid structure. Also the hybrid structure can be stacked to multiple layers to improve ION shown in Figs. 1(b) and (d). For H-JL-FET, the space-charge regions paralleling to channels are generated from PN junction of channel and substrate interfaces, reducing the effective thickness of channels and inhibit the IOFF [10, 11].

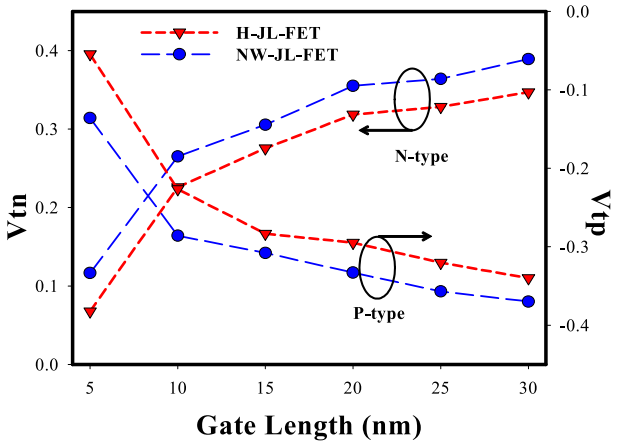

Fig. 3. Threshold voltage (V_T) of n-FET and p-FET for different L_G.

To verify the ability of suppressing short channel effect (SCE), the threshold voltage (VT) roll-off for different gate length was calculated and is shown in Fig. 3. Results indicate that the gate controllability decreases as the reduction of gate length. Especially in the case of LG = 5 nm, VT of both structures are about 0.1 V. For NW-JL-FET and H-JL-FET, VT can be adjusted by work function difference between gate and channel which is not easy to implement. However, the substrate concentration of H-JL-FET can provide a different method to adjust VT. To mitigate the tendency of VT roll-off, for H-JL-FET, substrate concentration is increased to improve VT, and therefore improve the device performance. Fig. 4 shows that as the substrate doping concentration increases for H-JL-FET, the

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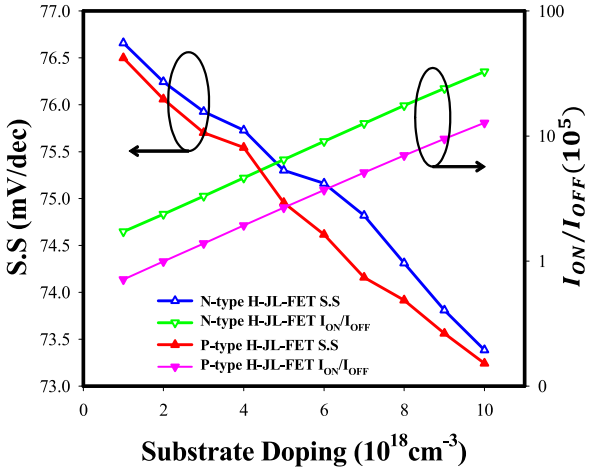

Fig. 4. S.S and I_{ON}/I_{OFF} current ratios of H-JL-FET for different substrate doping concentrations with $F_H = F_W = 10$ nm and channel doping = 10^{19} cm^{-3}.

subthreshold slope (S.S) and IOFF are reduced [11]. Although ION is slightly declined, the overall ION/IOFF is enhanced.

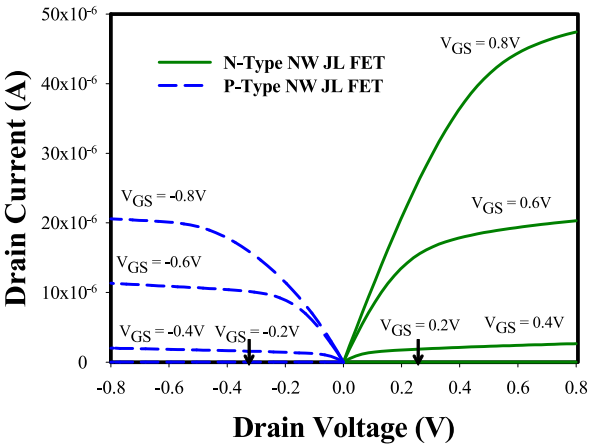

Fig. 5. I_D-V_D curves of the n-type and p-type, with a 10 nm gate length, for the NW-JL-FET structures. The left and right arrows indicate V_T for p- and n-FET, respectively.

Fig. 5 shows the ID-VD curve of NW-JL-FET with gate length of 10 nm. The curve shows good saturation properties. The saturation drain current of n-type NW-JL-FET is about 2.5 times of that of p-type NW-JL-FET due to different carrier mobility of electrons and holes. Similar tendency appears in H-JL-FET.

Fig. 6 shows the electron density of n-FET in the channel for both structures with gate length of 10 nm. When the device is in OFF state (Fig. 6(a)), carriers are centralized to all the channels. NW-JL-FET inhibits the IOFF using the work function difference [12]. Three channels can be considered to operate independently. As shown in Fig. 7, H-JL-FET is able to inhibit IOFF effectively due to the effective thickness of channel modulated by the space-charge region induced by PN junction between channel and substrate. The substrates that are above and below a Aux-CH restrict current to the effective channel functioning like top and bottom

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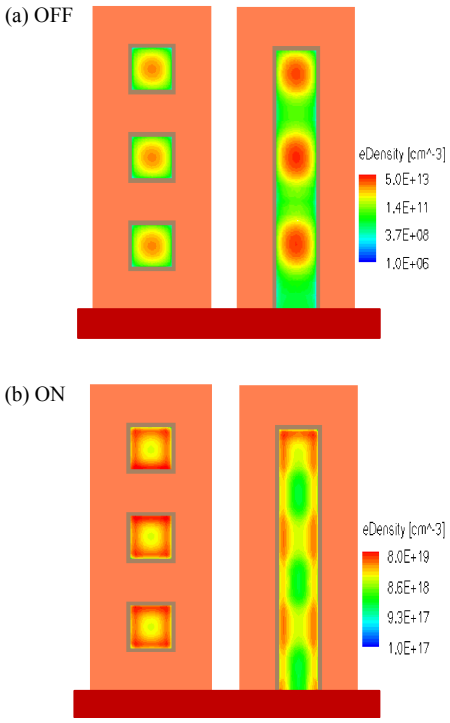

Fig. 6. Electron density distributions at the channel of n-FET at (a) $V_G = 0$ V, $V_{DS} = 50$ mV and; (b) $V_G = 0.8$ V, $V_{DS} = 50$ mV for gate length = 10 nm, and $T_{OX} = 1$ nm. The cross section is along AA′ shown in Fig. 1(a).

gates. Note that the electron concentration in the channel for H-JL-FET is about one order of magnitude larger than NW-JL-FET indicating the substrate restriction is not good as a true gate, but it takes better effect to suppress IOFF than other FinFET structures.

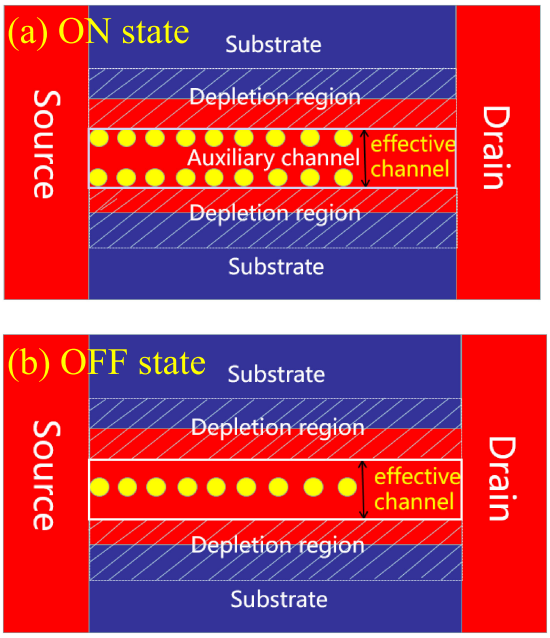

Fig. 7. Carrier distribution in Aux-CHs of H-JL-FET for (a) ON state and (b) OFF state. The cross section is along the XX′ shown in Fig. 1(b) and the small yellow balls denote carriers.

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Fig. 7(a) shows that carriers locate close to the interface between the channel and the oxide layer due to attraction of gates when the device is in ON state. The current of H-JL-FET is hardly influenced by the depletion region, resulting large ON current compared to NW-JL-FET. For OFF state shown in Fig. 7(b), the carrier is centralized in the channel and the OFF current is modulated by the effective channel width. However, the substrate concentration should not be higher than that in channels, for the Aux-CHs could be completely depleted by the substrate and incapable of providing current to improve ION. To mitigate this issue, the concentration of substrate and channel must be carefully designed.

Table I. Performance comparison between H-JL-FET and NW-JL-FET

Device Structure	DIBL (mV/V)	S.S (mV/dec)	I_{ON}/I_{OFF}
H-JL-FET	N:54.82 P:58.35	N:74.81 P:74.61	N:6.47×10^5 P:2.68×10^5
NW-JL-FET	N:35.11 P:44.12	N:71.09 P:70.24	N:2.82×10^5 P:1.31×10^5

The performance comparisons of two structures for gate length of 10 nm are list Table I. Although NW-JL-FET possesses better electrical characteristics than H-JL-FET, H-JL-FET is still comparable in some indexes indicating its potential in future applications.

4 Conclusion

This work studied on NW-JL-FET and H-JL-FET with different gate lengths. The two structures can be considered as representative of NW-FET and FinFET, respectively. NW-JL-FET has better performance due to its strong gate controllability originated from the GAA structure. However, the complicated fabrication process and high cost may hinder its application in practical use. In addition to adjustable VT by the substrate doping, H-JL-FET can still maintain comparable performance such as ION as NW-JL-FET in short channel due to the unique structure and operation mechanism. However, in order to acquire optimal performance, the structure and doping of H-JL-FET must be carefully selected.

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