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The impact of heat loss paths on the electrothermal models of self-heating effects in nanoscale tri-gate SOI MOSFETs

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Abstract: Nanoscale tri-gate SOI MOSFETs attract much attention in terms of the significance of self-heating effects (SHEs) which severely influence the operation stability and device reliability. Here, the impacts of the heat loss paths associated with the SHEs in nanoscale tri-gate SOI MOSFETs are comprehensively analyzed considering the gate dissipation channels (GDCs). The thermal resistance network model and thermal resistance model are presented to illustrate the heat dissipation mechanisms. 3D electro-thermal TCAD simulation results show that the heat flux through the GDCs occupies most part of the total heat dissipation. The static peak temperature can be decreased by decreasing the gate oxide thickness and increasing the cross-section of Fin area of tri-gate devices.

Keywords: tri-gate SOI MOSFETs, self-heating effects (SHEs), gate dissipation channels

Classification: Electron devices, circuits and modules

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1 Introduction

Multi-gate silicon-on-insulator (SOI) MOSFETs which have been considered as a promising option to replace planar devices on bulk or SOI substrate beyond technology nodes bellow 22 nm will suffer significant self-heating effects (SHEs) problems [1, 2]. Although there are different measurement methodologies [3, 4, 5] used to estimate the affection of SHEs on device performance, numerical simulation as well as physics modeling are still efficient ways to study the SHEs and validate the measurements [5, 6, 7]. It is a great challenge to solve the power dissipation problems in the nanoscale device with complex 3-D geometrical structure, particularly because it is an undefinable process in analytical terms [8]. The heat generation and diffusion mechanisms which are essential to describe the SHEs in SOI MOSFETs are rather complex to be modeled to estimate the maximum temperature and predicting the temperature distribution in nanoscale SOI device [9].

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The effects of steady-state self-heating in multi-fin devices on performance were analyzed based on the ultra-thin body (UTB) SOI thermal model [10]. A flared channel extension thermal model of each individual fin is presented to account for multiple fins. Xu et al. [11] presents an accurate analytical thermal model for estimating self-heating in FinFETs (or Tri-gate FETs) under both steady-state and transient conditions. The complicated heat generation and diffusion behaviors in the SOI MOSFETs were described by the model with equivalent heat source for the application of design engineers instead of the obscure solve of Boltzmann Transport Equation and heat diffusion equation. Thermal-resistance-network-based model and networks taking account of various heat flux paths and thermal coupling between the various regions or blocks have been established by Shrivastava et al. for accurate electrothermal simulation of nanoscale FinFET devices [12]. An electro-thermal model presented by Cheng et al. [13] based on the concept of characteristic thermal lengths representing various heat loss paths for heat conduction along each segment of the fins, channel, and metal/poly wires for multi-Fin devices. Since the high thermal conductivity of the gate material provides the least resistive path for heat to flow out of the device, the small thermal conductivity of the oxide will restrict the heat flow from the channel to the gate.

Here, the impacts of the heat loss paths associated with the SHEs in nanoscale tri-gate SOI MOSFETs are comprehensively analyzed considering the gate dissipation channels (GDCs) using 3-D electro-thermal TCAD simulation. Thermal resistance network model and Thermal resistance model are presented to illustrate the heat dissipation mechanisms. Furthermore, we also investigated the impact of the nanoscale on the temperature gradient and the equivalent heat source (hot spot) location in the Fin region of the tri-gate SOI MOSFETs, which are critical factors of thermal modeling.

2 Heat dissipation mechanism analysis for the tri-gate SOI MOSFETs

2.1 Device structure and boundary conditions

The SHEs characteristic of the SOI MOSFETs with source/drain extension was studied using the Sentaurus TCAD 3-D electro-thermal simulation. Fig. 1 demonstrates a coordinate system of 3-D triple gate SOI MOSFET structure. The X, Y and Z coordinates are along the channel length, width and height directions respectively. The channel is surrounded by a very thin oxide layer which enclosed with a fin-shaped gate. The source/drain extensions are packaged with a Si_3N_4 layer which marked as spacer. It adopts a High-k gate dielectric, HfO_2, as the gate oxide because of its high dielectric constant κ and excellent thermal characteristic in sub-45 nm regime. As shown in Fig. 1, L_g, H_{fin}, W_{fin}, L_{ex}, t_{ox}, H_{Box} is respectively the length of channel, fin height, fin width, source/drain extension, gate oxide thickness and buried-oxide thickness (BOX) of the device. During the thermal simulation, a constant voltage was applied on the gate while a linear increasing signal was applied on the drain to monitor the dependence of the temperature with heating power or simulation times. Therefore, the temperature, current and heat flux changes affected by SHEs could be observed in a time domain.

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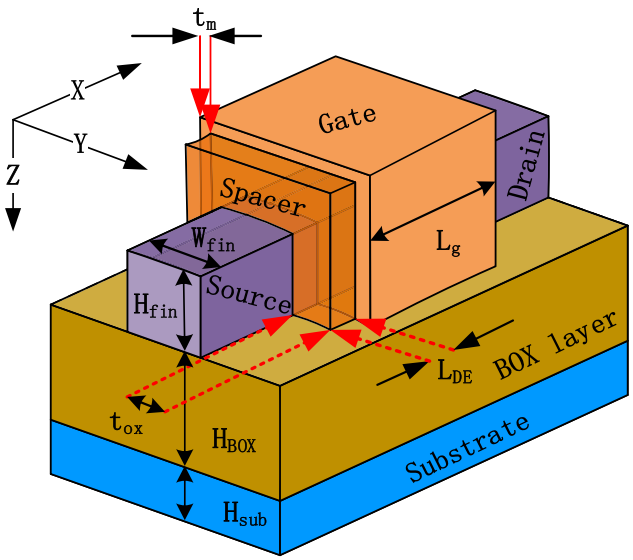

Fig. 1. 3D device structure used in the electro-thermal simulation

When the size of triple gate SOI MOSFETs decreases into nanoscale regime, the maximum heat generation and the Hot-spot in the device transferred into the drain extension region [14]. The channel heat source is replaced by the drain extension heat source. The thermal resistance and the networks which are greatly influenced by the mainly heat loss paths are significant indicators of SHEs.

In order to study the heat dissipation mechanism of the SOI MOSFETs, special thermal boundary conditions were set in electro-thermal simulations for the different heat loss paths assumption. The surface thermal resistance boundary condition is applied to the four pads for SHEs modeling as in [15]. Other surfaces are applied with adiabatic boundary due to the deposited thick oxide layer. Initially, the metal pads were set to ambient temperature. Thus, all the pads were treated as the same thermal point. And then the heat flow paths occur in the device shown in Fig. 2. There are six heat loss paths (A, B, C, D, E and F) from hot spot which is marked by red arrow. A, B and C are the gate dissipation channels along oxide layer (R_{gr}, R_{gl} and R_{gt}) and gate metal (R_{mr}, R_{ml} and R_{mt}). D is the drain heat sink including drain region (R_{drain}) and drain metal pad (R_{dm}). F is the source heat sink which contains channel region ($R_{channel}$), source extension (R_{SE}), source (R_{source}) and metal pad (R_{sm}). E is the body sink along the BOX (R_{box}), bulk (R_{bulk}) and the surface (R_{bulk_surf}).

2.2 Thermal resistance network model

The Fig. 3 represents the thermal resistance network in the channel region which indicates the mechanism of the heat flow out from the channel through the triple gate and BOX layer. The heat flux leads to the maximum temperature gradient along the X direction in the silicon Fin region, which entails the complex electro-thermal and thermo-electric coupling effects. Because of the narrow Fin and the high thermal conductivity of the silicon, the heat flow along the Y direction can be ignored, and that along the X and Z directions can be described by the following equations:

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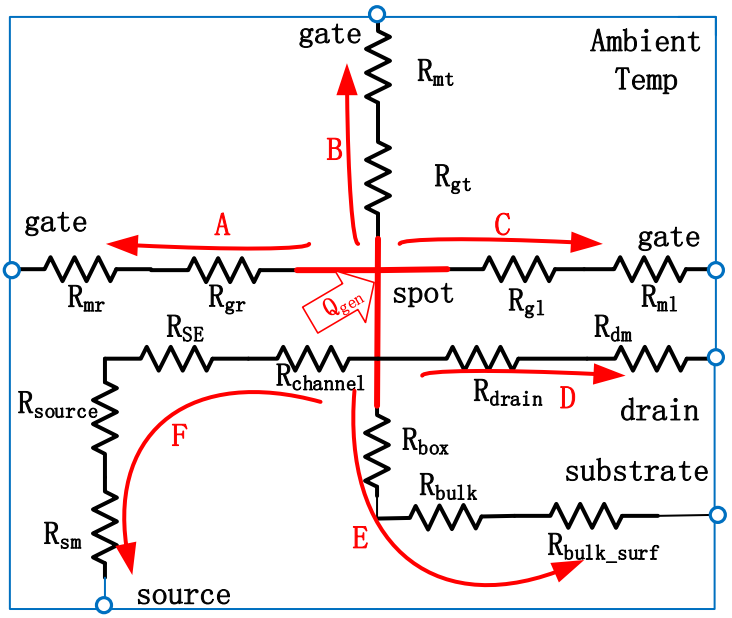

Fig. 2. Main heat loss paths resulted by the thermal boundary conditions for nanoscale SOI MOSFET

$$q_x = -\lambda_{si}\frac{\partial T(x,z)}{\partial x} \tag{1}$$

$$q_z = -\lambda_{si}\frac{\partial T(x,z)}{\partial z} \tag{2}$$

where q_x and q_z are the heat flux per unit time which vertically go through unit area along the X and Z directions respectively. The temperature gradient determines the heat flux through the heat loss path. Using Finite Element Method (FEM), the temperature difference can be explained by Eq. (3):

$$\Delta T = \frac{q \cdot \Delta l}{\lambda_{si}} \tag{3}$$

where Δl is the finite element length along the channel.

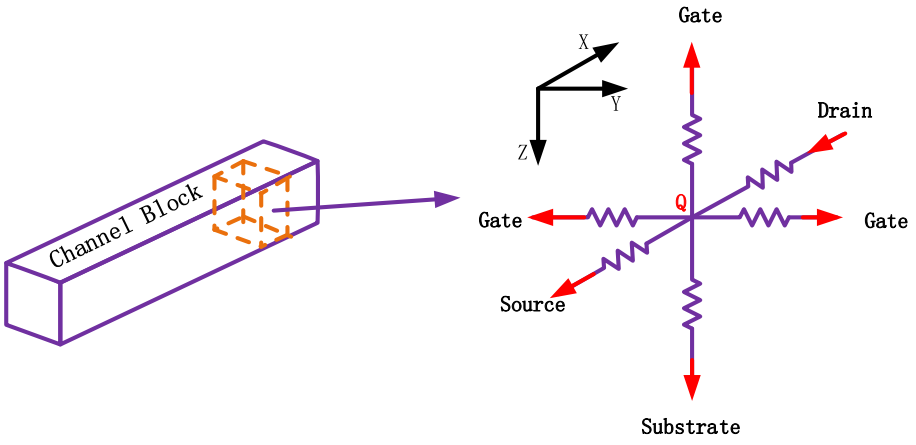

Fig. 3. The heat generated in the drain extension heat source dissipation paths

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2.3 Thermal resistance model

The thermal resistance is determined by the heat flow paths inside the device. Considering the heat flux path associated with buried-oxide, the thermal resistance of the triple gate SOI MOSFETs is calculated by the following equation [14]:

$$R_{th\_SOI} = \frac{1}{2W_{fin}}\sqrt{\frac{H_{BOX}}{\lambda_{ox}\lambda_{si}H_{fin}}} \tag{4}$$

where λ_{ox} and λ_{si} are the thermal conductivity of the buried oxide and the Silicon, respectively.

Heat dissipation is sensitive to the dimensions of the pads. The heat removal process along the buried oxide in nanoscale SOI device is not as efficient as that along the gate oxide. Thinner oxide and larger area metal pads with higher thermal conductivity will account for most part of heat flux dissipation. Therefore, when neglecting the heat flux GDCs, the thermal conductance dramatically decreases which lead to the enormous error in SHEs prediction. Thus, the heat transfer at the interface of the Fin with the gate oxide forming the GDCs should be considered in the thermal resistance model. In triple gate SOI MOSFETs, heat dissipates through the surrounding oxide to the substrate and three gates where the equivalent heat diffusion perimeter could be calculated by Eq. (5):

$$W_{ef} = 2H_{fin} + W_{fin} \tag{5}$$

The heat diffusing from high temperature region to low temperature region, exponentially attenuates over a distance above the BOX layer which described by the cooling length. When the heat diffusion perimeter is determined, the heat loss cross-sectional area is defined by the cooling length related to the characteristic of the dielectric layer material including the thermal conductivity and the size. Thin gate dielectric and long heat diffusion perimeter result in the much small GDCs thermal resistance which is expressed by the following equation:

$$R_{th\_gates} = \frac{1}{2W_{ef}}\sqrt{\frac{t_{ox}}{\lambda_{ox}\lambda_{si}H_{fin}}} \tag{6}$$

In tri-gate SOI MOSFETs, according to the main heat loss paths resulted by the thermal boundary conditions shown in Fig. 2, the BOX thermal resistance and GDCs thermal resistance are considered as parameters of parallel executions, and the heat diffusion ability of the triple gate SOI MOSFETs with GDCs is evaluated by equation (4):

$$R_{th} = \frac{R_{th\_gates} + R_{th\_SOI}}{R_{th\_gates} \cdot R_{th\_SOI}} \tag{7}$$

Generally, the gate oxide thickness (t_{ox}) is much smaller than the one of the BOX, therefore results in a larger thermal conductance. That means most of the heat flux flows through the gate oxide rather than the BOX. The total SOI thermal resistance depends on the gate thermal resistance in the Nano-SOI device.

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Table I. Classic dimensions, doping and material thermal parameters

L_g (Channel Length)	45 nm
H_{fin} (Fin Height)	26 nm
W_{fin} (Fin Width)	12 nm
H_{BOX} (Buried oxide thickness)	30 nm
t_{ox} (Equivalent gate oxide thickness)	1.25 nm
N_A (Channel natural doping)	10^{15} atoms/cm^3
N_D (Source/Drain Gauss doping)	With 10^{20} atoms/cm^3 peak value
k_{BOX} (BOX thermal conductivity)	1.4 W/mK
k_{Si} (Silicon thermal conductivity)	$1/(a+bT+cT^2)$ (a = 0.03 cm KW^{-1}, b = 1.56×10^{-3} cm W^{-1}, c = 1.65×10^{-6} cm W^{-1} K-1)

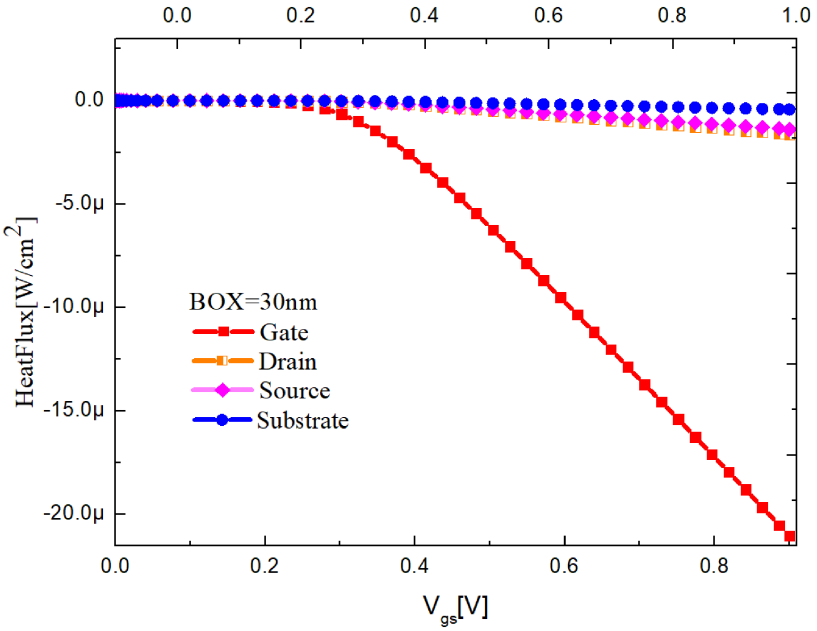

Fig. 4. Heat flux versus gate voltage for the four terminal electro-node

3 Result and discussion

The triple gate SOI MOSFET with the parameters listed in Table I was simulated to investigate the heat flux along the possible dissipation channels using the coupled 3-D electro-thermal model.

Fig. 4 shows the effect of heat flux versus V_{gs} at V_{ds} = 0.9 V. As shown in the figure, when increasing V_{gs}, the heat flux through the substrate, source, drain and gate terminals increasing from 0 (V_{gs} = 0) to 0.427μ, 1.38μ, 1.62μ and 21μ (W/cm^2, V_{gs} = 0.9 V), respectively. The heat flux dissipated through the triple gates occupies 86% of total heat at Vgs = 0.9 V. and the heat flows out the drain, source and substrate account for 6.61%, 5.64% and 1.75%, respectively. Most of the heat flows through the gate interconnects, which is determined by the heat loss thermal resistance with dimensions of the path shown in Eq. (8).

$$R_{path} = L/\lambda S \tag{8}$$

where L is the length along the heat loss direction, λ is the thermal conductivity of the material, S is cross-section area vertical the heat flux. It shows that the thin

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oxide and the large surface area lead to large gate thermal conduction which dominates device thermal conduction. The thin buried oxide increases heat dissipation and makes the BOX path non-negligible.

Fig. 5 represents the temperature distribution along the Fin in the SOI devices with BOX = 30 nm and BOX = 65 nm with/without considering the influence of the GDCs. The static peak temperature is dramatically decreased due to the heat flux dissipation considering GDCs. The temperature gradient around the Fin area changes greatly which can be illustrated by the variation of R_{th_gates} and R_{th_SOI} described in Eq. (7). The results indicate that the definition of the heat loss paths is a critical factor for establishing the thermal models. If the GDCs were not taken into consideration, the device will suffer higher temperature. It can be also seen from the figure that the temperature associated with SHEs are varied with different buried-oxide thickness. Compared with thicker buried-oxide layer, the temperature rising is smaller in the device with thinner buried-oxide layer. It can be concluded that thin buried-oxide is beneficial to dissipate the heat flux generated inside the device.

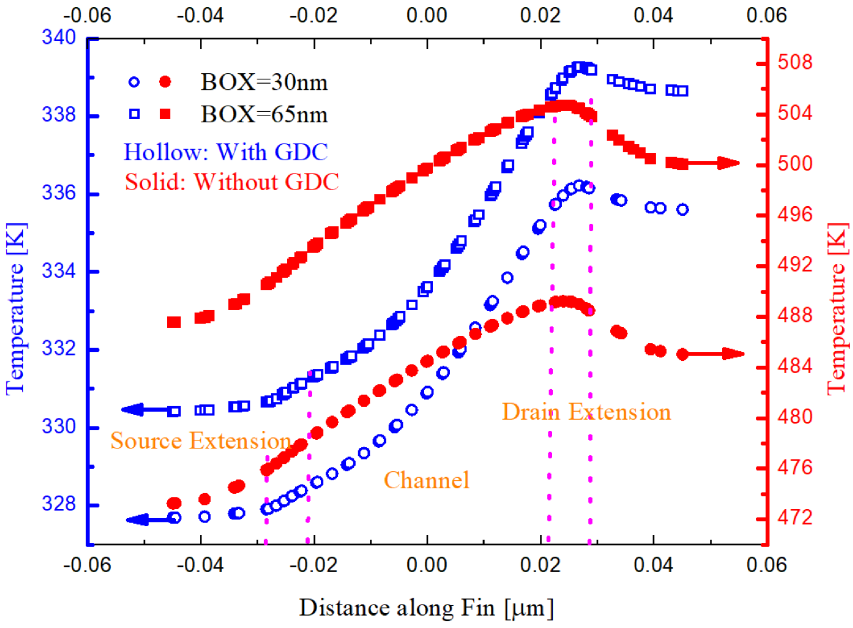

Fig. 5. Temperature distribution along the Fin with different BOX thickness

Fig. 6 shows the temperature distribution and the thermal resistance associated with different Fin cross-section areas along. The thermal resistance which is defined by $\Delta T/Power$ of the device with 24 nm Fin widths is smaller than that of the one with 8 nm Fin widths based on the analysis which described in the Eq. (6). The peak value of temperature in device with 24 nm-Fin widths is larger than that of another one. A smaller thermal resistance means that the heat diffusion could be enhanced by changing the dimension of the device. However, the operation current under a certain voltage application will be increased. The power will be also increased which will significantly result in the temperature increasing.

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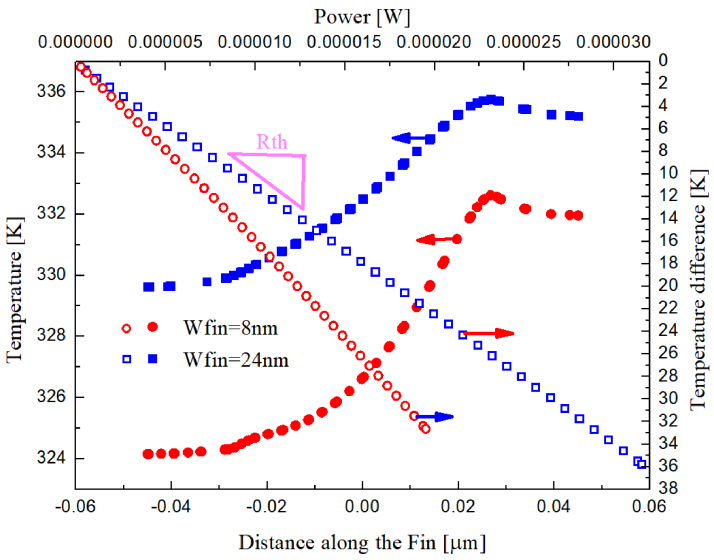

Fig. 6. Thermal resistance and temperature distribution along the Fin with different cross-section area of the GDCs.

4 Conclusion

The self-heating effects severely influence the stability and reliability of nanoscale tri-gate SOI MOSFETs. 3D electro-thermal TCAD simulation study has been done to investigate the impacts of the heat loss paths on the heat flux dissipation and temperature distribution considering the gate dissipation channels. The heat flux through the GDCs occupies most part of the total heat dissipation. The static peak temperature can be decreased by decreasing the gate oxide thickness and increasing the cross-section of Fin area of tri-gate devices. The diverse electro-thermal models with different heat loss paths will lead to different prediction of the temperature distribution and temperature gradient caused by the SHEs. Thus, for avoiding the huge deviation in the assessment of self-heating effects, the parallel relationship between GDCs and BOX heat loss path cannot be ignored.

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