ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.16, No.4, 1–9

A high-precision coarse-fine time-to-digital converter with the analog-digital hybrid interpolation

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Abstract: An innovative high-precision coarse-fine time-to-digital converter (TDC) is presented. The TDC architecture mainly consists of a coarse counter and a delay-line-based analog-digital hybrid interpolator. In order to improve the precision, the key timing control of the interpolator is provided by a novel customized synchronizer. Comparing to the traditional delay-line-based interpolator, the proposed analog-digital hybrid interpolator using the multi-voltage sampling technique improves the resolution significantly. A prototype chip has been fabricated in a 0.35 µm CMOS process. After the calibration and calculation based on fitting algorithms, the TDC prototype reaches a dynamic range of 512 ns and a single-channel single-shot precision of 6 ps using the external look-up table (LUT) for the interpolator.

Keywords: time interval measurement, time-to-digital converter (TDC), coarse-fine architecture, analog-digital hybrid interpolation, calibration

Classification: Integrated circuits

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DOI: 10.1587/elex.16.20181062
Received November 30, 2018
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1 Introduction

Time-to-digital converter (TDC), a device used for measuring time interval, converts the time interval to the digital output. Due to its superior time resolution, TDC is highly demanded in various applications, including laser range finding [1], time-of-flight (ToF) measurement [2], fluorescence lifetime imaging microscopy (FLIM) [3, 4], high energy particle detectors [5, 6] and all-digital phase-locked loop (ADPLL) [7, 8].

TDCs can be classified into two categories based on analog techniques or digital techniques. The analog-type converter, also called time-to-amplitude converter (TAC), converts the time information to a corresponding voltage amplitude by charging or discharging a capacitor with constant current [1, 4, 5, 6, 9]. Then the voltage is digitalized by a high-resolution analog-to-digital converter (ADC). This TDC structure usually has advantages of high-resolution, high-linearity and low area requirement, and is often implemented in area-sensitive applications like within pixel array chips. However, it suffers low scalability and large process, voltage and temperature (PVT) variations. In the other TDC type, based on digital techniques, a delay line consisting of successive buffers is employed in high resolution required applications [3, 8, 9]. A start pulse propagates through the delay line, and its statuses along the delay line will be recorded by flip-flops triggered upon the arrival of a stop pulse. Then, the time interval between the start and stop pulse is obtained by decoding the statuses. The resolution of the tapped delay line is limited by the propagation delay of one single delay unit, which makes the delay-line-based TDC also sensitive to the delay jitter, noise and mismatch of the delay units. The TDC presented in this paper adopts the basic delay line structure, but combines the analog and digital methods for the delay unit readout. With the novel analog-digital hybrid interpolation by multi-voltage sampling, the resolution of the delay-line-based TDC is significantly improved. The impacts of the mismatch from delay cells on the resolution are also minimized by a dedicated look-up table (LUT) calibration method.

In this paper, Section 2 explains the principle of the traditional coarse-fine TDC based on the delay line. The proposed TDC structure is introduced in Section 3. The chip test setup, measurement methods and test results are discussed in Section 4, and the work is summarized in Section 5.

DOI: 10.1587/elex.16.20181062
Received November 30, 2018
Accepted December 11, 2018
Publicized January 18, 2019
Copyedited February 25, 2019

2 Traditional coarse-fine TDC based on delay line

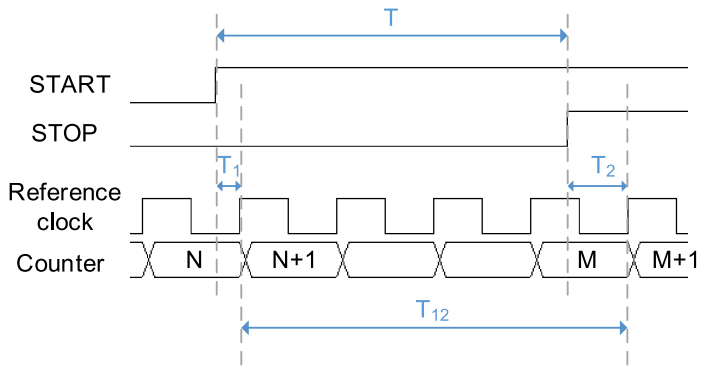

Fig. 1. Timing diagram of the coarse-fine TDC

A typical digital timing diagram of the traditional coarse-fine TDC is shown in Fig. 1. A coarse counter is used to count the number of the rising edge of the reference clock within the time interval between two electrical pulses (START and STOP). The output of the coarse counter (M-N) is proportional to the time T_{12}. The fine interpolator is implemented with the circuits shown in Fig. 2. It is used to resolve the time interval (T_1 and T_2 in Fig. 1) between the rising edge of START (or STOP) and the next reference clock rising edge. The two input events (START and STOP) are donated as HIT hereafter, since they are totally identical to the circuits. The HIT signal propagates through the delay line composed of identical buffers with a unit delay time of T_d. The output of each buffer is latched by a register when the next rising edge of the CLK (Trigger) arrives. Finally, all the register outputs constitute a thermometer code, indicating the amount of transmitted buffers. The total time interval T can be expressed as Eq. (1), where D_1 and D_2 are the digital outputs of the delay-line-based fine interpolators for START and STOP respectively, and T_{CLK} is the reference clock period.

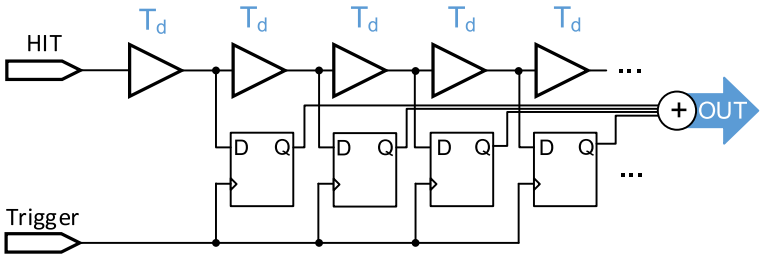

Fig. 2. Block diagram of the delay-line-based interpolator

$$\begin{aligned} T &= T_{12} + T_1 - T_2 \\ &= (M - N) \bullet T_{CLK} + (D_1 - D_2) \bullet T_d \end{aligned} \tag{1}$$

Thus, the dynamic range of the traditional delay-line-based coarse-fine TDC, namely the maximum time interval the TDC can measure, depends on the bits of the coarse counter. And the resolution depends on the propagation delay of the delay unit, which is about tens of picoseconds typically and limited by the process [7]. In order to further improve the resolution performance, an innovative analog-

DOI: 10.1587/elex.16.20181062
Received November 30, 2018
Accepted December 11, 2018
Publicized January 18, 2019
Copyedited February 25, 2019

digital hybrid interpolation based on the multi-voltage sampling in delay line is proposed in the following section.

3 Proposed TDC architecture

The block diagram of the proposed TDC is shown in Fig. 3. It consists of an 8-bit coarse counter, an analog-digital hybrid fine interpolator, a readout controller, a synchronizer and an analog output buffer. The synchronizer generates a low-jitter rising edge signal S1 synchronous with the next rising edge of the reference clock after the HIT pulse. The time interval between the rising edge of HIT and S1 (T_1, T_2 in Fig. 1) is resolved in the delay-line-based fine interpolator with the multi-voltage sampling technique. The readout controller is a 32-bit shift register composed of 32 D-type flip-flops. It generates 32-bit signals which control the analog readout of the fine interpolator according to the external SDAT and SCLK signals. The analog output buffer reads out the voltage generated by the fine interpolator to an off-chip ADC. Meanwhile, the coarse counter outputs 8-bit digital result (M, N in Eq. (1)) when S1 turns high.

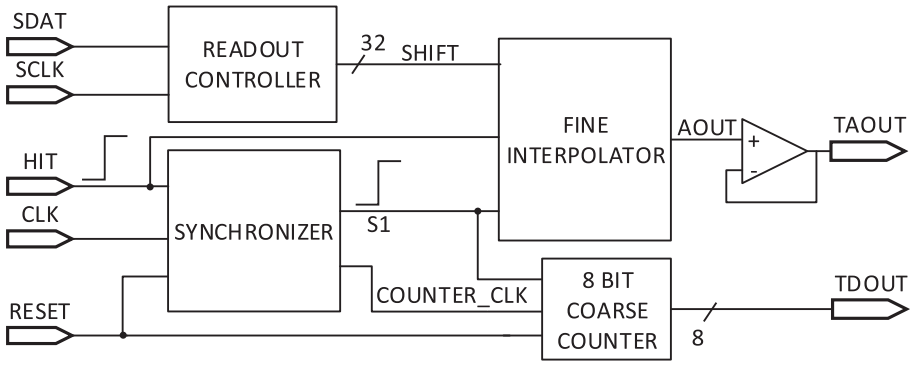

Fig. 3. Block diagram of the proposed TDC

3.1 Synchronizer

The synchronizer is used to generate the reference clock for the coarse counter and the S1 signal, which is synchronous to the reference clock CLK for sampling the fine interpolator and latching the coarse counter. A stable and low-jitter S1 signal is required for the analog-digital hybrid interpolation described in Section 3.2 to achieve a high-resolution performance. A pulse signal SW synchronous to CLK can be generated in the logic circuit as shown in the left of Fig. 4. The timing diagram of signals is shown in the right of Fig. 4. The rising edge of CLK_DELAY passes the switch when SW is high, and constitutes the output S1. Therefore, the timing of S1 inherits from the original clock edge instead of using logic circuits and flip-flops to avoid extra jitter injection. Moreover, the rising edge of the synchronous signal S1 is ensured to be in the middle phase of the counter clock, which eliminates the potential metastability.

3.2 Analog-digital hybrid fine interpolator

The fine interpolator adopts the basic delay line structure with analog readout methods. The proposed delay unit in the delay line includes an inverter, a switch

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Received November 30, 2018
Accepted December 11, 2018
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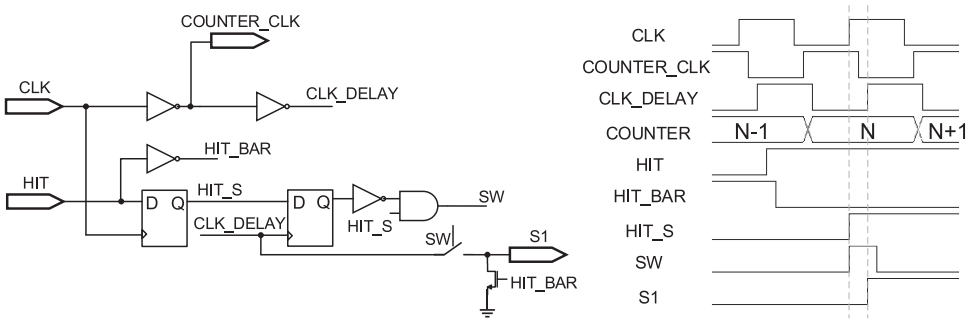

Fig. 4. Block diagram of the synchronizer

and a capacitor derived from the input parasitic of the analog buffer as shown in Fig. 5. The output of each inverter is marked as node 0 ~ node 31 in the delay line. The switches and capacitors are employed to sample the analog voltages of each node instead of using digital flip-flops in the conventional digital way as shown in Fig. 2. The sampling time is then controlled by the signal S1 illustrated in the last subsection. When S1 is low, the voltages of the capacitors follow the outputs of all inverters. Once S1 turns high and the switches are off, the voltages of all nodes are kept on the capacitors, and then read out through the analog buffer one by one under the control of SHIFT switches.

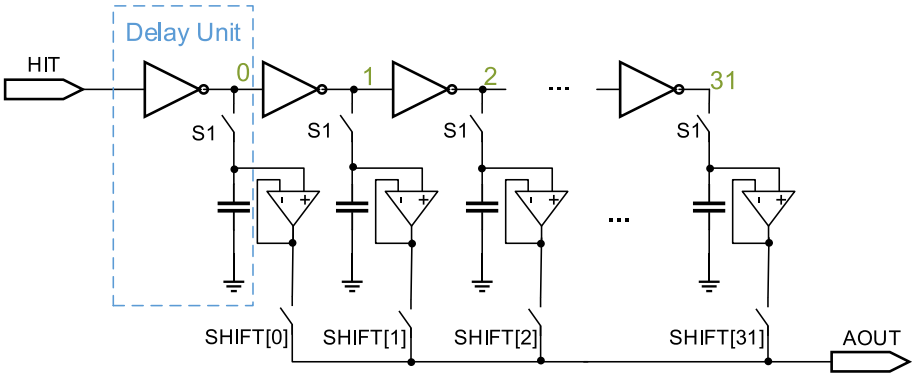

Fig. 5. Analog interpolated delay line

Fig. 6 shows the output voltage of each node along the delay line. The rise-time/fall-time T_E of the inverter is assumed to be larger than the propagation delay T_D of an inverter. So when the sampling is triggered (S1 rising edge), output voltages of some inverters have reached 0 or 3.3 V (VDD), while some inverters (node 2, 3, 4) output specific voltages between 0 ~ VDD. For each node that gives the voltage between 0 ~ VDD, the time interval T between HIT and S1 can be calculated once using Eq. (2).

$$T = N \bullet T_D + \alpha \bullet T_E, \quad 0 < \alpha < 1 \tag{2}$$

In Eq. (2), N is amount of delay units before the node, α equals to V_N/V_R if N is even, otherwise $(1 - V_N/V_R)$. V_N is the node voltage and V_R is 3.3 V. In Fig. 6, for example, the time interval T can be calculated using node 2 as $3 \times T_D + (1 - V_{N2}/3.3) \times T_E$, or calculated using node 3 as $4 \times T_D + (V_{N3}/3.3) \times T_E$. In this paper, all potential nodes are used to calculate the time interval T respectively, and the final result is obtained by averaging the calculation results. The resolution

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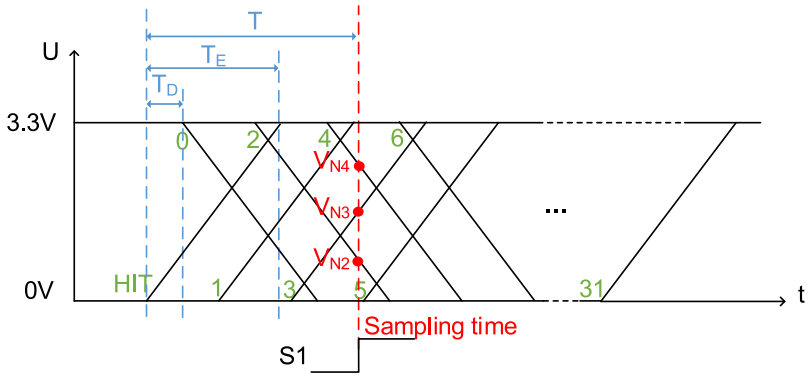

Fig. 6. Node voltages along the interpolator delay line

of the proposed interpolator is significantly improved with the analog readout method. The impact of the delay mismatch and the noise, which are the limitations to the precision of TDC, also can be effectively reduced by multi-voltage sampling.

4 Experimental results

A prototype of the proposed TDC has been fabricated in a 0.35 µm CMOS process. Fig. 7 shows a microphotograph of the TDC. The active area is 290 µm × 1045 µm including a fine interpolator, an analog output buffer, a counter and a synchronizer. The complete output format of the TDC contains the 8-bit digital word from the coarse counter and the analog output voltages of the fine interpolator. The analog outputs are digitalized by an off-chip commercial 8-bit ADC. The TDC works under a power supply of 3.3 V with a total power consumption of 54 mW.

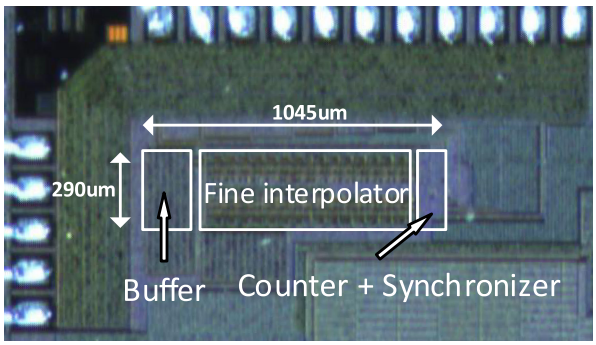

Fig. 7. Microphotograph of the prototype TDC chip

4.1 Measurement setup

The diagram of the measurement setup is shown in Fig. 8. Two TDC chips (TDC1, TDC2) are used as a START channel and a STOP channel, and are bonded to the test carrier boards, respectively. The Xilinx Kintex-7 FPGA evaluation board receives the digital outputs of two TDCs and ADC, then transmits the raw data to the host computer. A 500 MHz external reference clock is provided to two TDCs, and the START/STOP input signals are generated from FPGA by splitting one original signal into two coaxial cables with the adjustable delay box.

4.2 Calibration

Due to the mismatch, the nonlinearity of the delay chain is inevitable. However, the

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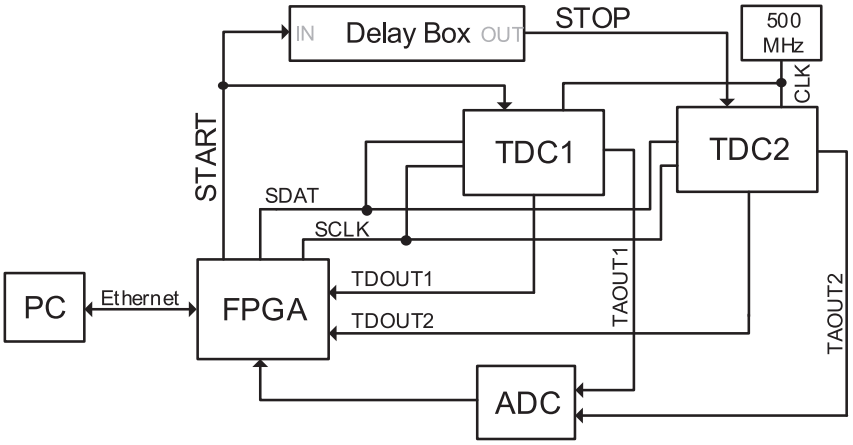

Fig. 8. Diagram of the measurement setup

nonlinearity can be minimized for a specific delay line by using a LUT containing the known error [10]. To acquire the LUT, the TDC analog output voltages of every two units are used to simplify the analysis, since they have the same trend from "1" to "0". Fig. 9 shows an example of the analog outputs and the diagram of each node output variation from the fine interpolators in two TDCs. The time information can be described as a U-n curve which reveals the relationship between the voltage and the node number, as shown in the left of Fig. 9. But the real voltage curve is not as ideal as the right of Fig. 9. Thus, a typical S curve formula, Eq. (3) is used to fit the U-n curve.

$$U = \frac{\mathrm{k}}{1 + \mathrm{a} \times e^{n+b}} + \mathrm{c} \tag{3}$$

The input time controlled through a delay box is changed by 10 ps per step in the range of 2 ns for the calibration measurements. Because of identical delay units in the fine interpolator of a certain TDC, k, a and c in Eq. (3) are all constant. Hence, a parameter b can be calculated by fitting the known analog outputs according to Eq. (3) for each input time. Finally, the input time and the parameter b constitute the LUT.

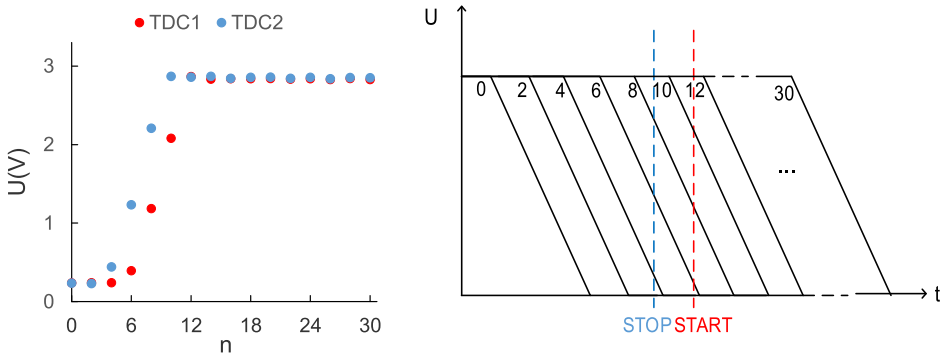

Fig. 9. Example of START and STOP channels analog outputs

4.3 Precision measurement

When the input time interval to a TDC is kept fixed during the measurement, the standard deviation (sigma) of the output distribution is taken as the precision [7].

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Received November 30, 2018
Accepted December 11, 2018
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Copyedited February 25, 2019

The maximum time interval the proposed TDC can measure is $1/500\,\mathrm{M} * 256 = 512\,\mathrm{ns}$. Due to the limited range of the delay box, the precision of TDC is measured at three specific delays with the LUT calibration. A parameter b_t can be calculated in every event according to the analog output and the fitting algorithm. Then, the parameter b_t is used to acquire the fine time result with the linear interpolation of the LUT. The results are shown in Fig. 10. The bin width is 10 ps and the standard deviation is calculated with 10^4 measurements of the same input time interval. The worst standard deviation based on the two-channel experiment is 8.43 ps. So the single-channel single-shot precision is $8.43/\sqrt{2} = 6\,\mathrm{ps}$, which is also the effective resolution of the prototype TDC in this case. The tested precision performance benefits from the multi-voltage sampling technique and the LUT calibration.

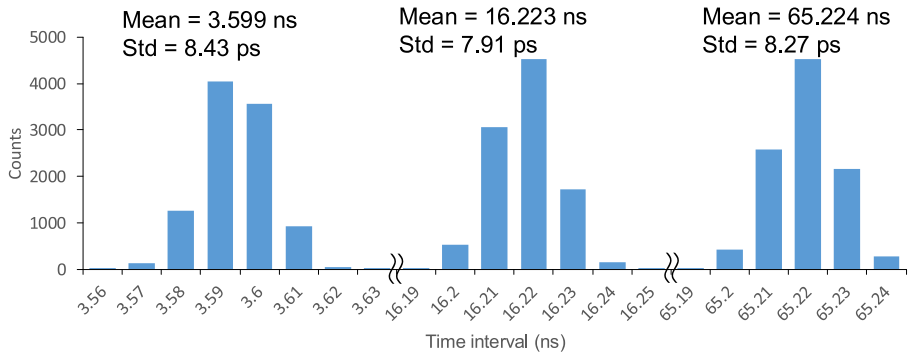

Fig. 10. TDC precision measurements with the LUT calibration

Table I gives a brief comparison of several reported works using analog or hybrid architecture. The proposed converter achieves a state-of-the-art high precision of 6 ps under the standard 0.35 µm CMOS technology with low area occupation. Compared to the published works of TAC structures using an external 14-bit ADC [4, 5, 6], this TDC works with an external 8-bit ADC, and has a great improvement on precision. However, compared to [9] with the internal digitalization, this work complicates external circuits and off-chip analysis but improves the resolution performance with the multi-voltage sampling technique and the LUT calibration.

Table I. Comparison to previous works

	This work	[4]	[5]	[6]	[9]**
Architecture	Hybrid interpolation	TAC	TAC	TAC	DLL+TAC
Technology (nm)	350	130	350	350	180
Dynamic range (ns)	512	50	45	50	10000
Resolution (ps)	6 (RMS)	6.66 (LSB)	17* (RMS)	25.5* (RMS)	10 (LSB)
Precision (ps)	6	368	17	25.5	-
Core area	0.3 mm^2	64 $\mu\mathrm{m}^2$	0.25 mm^2	1.68 mm^2	0.22 mm^2
Power (mW)	54	-	50	60	44

*conversion from FWHM values **with an internal 3-bit ADC

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Received November 30, 2018
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5 Conclusions

A high-precision coarse-fine TDC with an analog-digital hybrid interpolator is designed and fabricated in a 0.35 µm CMOS technology. The dedicated fitting algorithm and look-up table are used for the TDC outputs to minimize the nonlinearity. The TDC precision is tested to be 6 ps with the novel analog-digital hybrid interpolation using multi-voltage sampling at the delay line outputs. A coarse counter is employed to extend the TDC dynamic range to 512 ns.

Acknowledgments

This work is supported by the National Natural Science Foundation of China under Grant No. 11420101004 and the National Program on Key Basic Research Project of China under Grant No. 2015CB856906.

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