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An inverter chain with parallel output nodes for eliminating single-event transient pulse

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Abstract: The current paper presents an inverter chain with parallel output nodes design for the purpose of eliminating the single-event transient (SET) pulse. The structure of parallel output nodes combined with the layout utilizing isolation approach can eliminate the SET pulse substantially. As compared with the conventional inverter chain as well as the inverter chain of source-isolation approach and the duplicated inverter chains with C-element, the simulation results illustrate that the proposed inverter chain manifests an effective improvement of immunity to SET. With regard to P-hit, the proposed inverter chain is capable of attaining a stable output irrespective of the state of the struck PMOS being OFF or ON. With regard to N-hit, the proposed inverter chain can also maintain the final output steadily. As long as the SET pulse is not generated at the eventual output node, the pulse can be eliminated by the proposed inverter chain. Besides that, the proposed approach is also applicable to the circuits with the structure like inverter chain.

Keywords: inverter chain, N-hit, P-hit, single-event transient

Classification: Integrated circuits

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1 Introduction

In the outer space environment, when highly energy particles strike sensitive regions of integrated circuits in spaceflight systems, it is likely to lead to single-event effects (SEE) [1]. With the shrinkage in the device feature sizes, the SEEs are presenting a major challenge to the reliable operations of integrated circuits, and SETs in the digital circuits are emerging as the leading single event soft error phenomenon [1, 2, 3, 4, 5]. In particular, in high clock frequency circuits, the SET pulse width (W_{SET}) and the clock pulse width are likely to be in the same order of magnitude [2, 4]. So, the SET pulse would propagate through the circuit easily and lead to a soft error.

Previous experimental research works have illustrated the fact that SETs have always occurred in combinational logic [4]. Inverter chain is common in combinational logic. Sadly, inverter has been proved that is susceptible to SET [6, 7, 8, 9].

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For the common two-transistor inverters, when ions strike the sensitive area, the SET pulse may occur [6, 7]. The low-pass filter can be used in the inverter chain to attenuate the narrow SET pulse, but it can not eliminate the SET pulse that has a large width. As for the duplicated inverter chains with C-element, if the signals of the original inverter chain and the duplicated inverter chain are both disturbed by the ion striking, the final output is likely to be incorrect. It is possible to make use of the source-isolation approach in the inverter for P-hit SET mitigation [9, 10]. In reference [10], the authors divided the PMOS of inverter into two serial PMOSs. With the use of the shallow trench isolation (STI), the two PMOSs are isolated, and the bipolar effect can be substantially lowered. So, the SET pulse can be mitigated if an ion struck at an OFF PMOS. Nevertheless, there exists a flaw in the inverter that utilizing source-isolation approach, the SET negative pulse may occur when an ON PMOS is hit by particles [11]. If the drain of the PMOS of isolation technique is hit by a heavy ion, there will be numerous electron-hole pairs generated along the penetration path. The potential of N-well will drop since the electrons will be constrained by the N-well. The P-N junction that is caused by the N-well and the drain of struck PMOS will drive the electrons in the N-well to the drain. If the energy of ion striking is sufficiently large, the potential of the drain of the struck PMOS will decrease to even logic “0”.

In this paper, a parallel output nodes design of inverter chain is put forward. As compared with the three existing designs of inverter chain, the proposed design can maintain a stable and correct output irrespective of an ion striking at the OFF or ON PMOS. Besides that, it also works better in SET mitigation when an ion hits at an NMOS. In addition, as long as the SET pulse is not generated at the eventual output node, the proposed inverter chain can eliminate it.

2 The proposed design

Fig. 1 shows the schematic of the proposed design. The input signal is n1. The outputs of the foremost stage inverter are n2 and n3, which connect to the gates of the PMOSs as well as the NMOSs at the second stage inverter, respectively. The remaining inverters are connected likewise, and n13 is termed as the final output. Unlike the conventional inverter chain as well as the inverter chain of isolation approach, the proposed structure has two output nodes in every stage inverter, and the two parallel nodes control the PMOSs and the NMOSs of the next stage individually. The topological structure design, in combine with the layout design, can enhance the SET immune of the proposed inverter chain significantly. We are going to clarify it with the analysis of the second stage inverter.

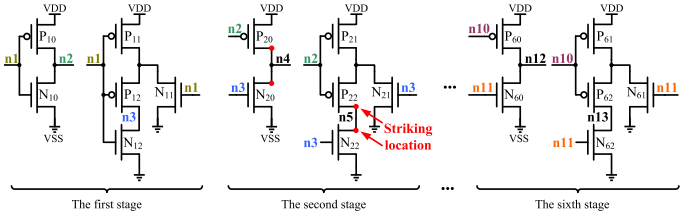

Fig. 1. Schematic of the proposed inverter chain.

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The ion striking can be divided into two situations.

Situation 1: P-hit

1) If the input n1 is logic "0", signal n2 and n3 are at high level. P_{20} and P_{22} are turned off, and the signal n4 and n5 are low.

In a case where the struck PMOS is P_{20}, the signal n4 might change to high level. So, the PMOSs at the posterior stage inverter will be turned off. But the signal n5 still stays at logic "0", thus the NMOSs at the posterior stage inverter will not be conducted on. So, the output nodes at the next stage inverter can not be discharged, and the potential of the output nodes can be hold. Therefore, the following stages of the inverter chain can keep the outputs steadily.

In a case where the struck PMOS is P_{22}, the voltage of n5 will be disturbed, but the logic level will not change to high level. That is because we make use of stacked PMOSs with isolation for the purpose of hardening the drain of P_{22}. The STI between P_{21} and P_{22} can break the parasitic bipolar junction transistor (BJT), so the bipolar effect can be weakened efficiently, and the quantity of holes, which could be absorbed by the drain of P_{22}, is substantially lowered. In addition, we make use of N_{21} to discharge the source of P_{22}, so that the disturbance to the voltage of the drain of P_{22} could be further lessened, which suggests that the SET amplitude will be lowered effectively. So, the voltage of n5 will be stay at logic "0" subsequent to ion striking, and then the output nodes at the next stage inverter can hold the potential. Thus, the following stages of the inverter chain will output correctly.

2) If the input n1 is logic "1", signal n2 and n3 are at low level. P_{20} and P_{22} are on, and the signal n4 and n5 are high.

In a case where the struck PMOS is P_{20}, because P_{20} is at ON state and the source of P_{20} is connected to VDD, the voltage of the drain of P_{20} will be at high level stably. Thus, the inverter chain will keep the outputs steadily.

In a case where the struck PMOS is P_{22}, the voltage of n5 may decrease because of the drawback results from making use of stacked PMOSs with isolation approach. We make an assumption that the logic level of n5 drops to low level because of the ion striking with large energy. Thus, the NMOSs at the posterior stage inverter will be at OFF state. Nevertheless, signal n4 still stays at high level, so the PMOSs at the posterior stage inverter will not change to ON state. For the output nodes at the posterior stage inverter, VDD will have no path to charge them. So, the outputs of the posterior stage to the last stage are expected to be stable.

Situation 2: N-hit

When the NMOS of an inverter is hit by an energetic particle, the voltage of struck node is temporarily lowered. If the voltage of struck node is logic "0", an ion striking will pull the voltage lower than VSS, but the logic level will not change. Nonetheless, if the voltage of the struck node is logic "1", an ion striking may change the logic level to logic "0" [12]. Therefore, we mainly consider the case when the voltage of the struck node is at logic "1", i.e., the signal n4 and n5 are high.

In a case where the struck NMOS is N_{20}, the voltage of n4 may decrease to low level rapidly. It will turn on the PMOSs of the third stage inverter. But those conducting on PMOSs will not cause a full-swing transient at the output node,

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which is because the signal n5 is high and the corresponding pull-down NMOSs are also at the ON state. The transient pulse amplitude will attenuate with it propagating away.

In a case where the struck NMOS is N_{22}, the voltage of n5 may decrease to logic "0". The low level n5 will turn off the NMOSs at the posterior stage inverter. However, the signal n4 still stays at high level, so the PMOSs at the posterior stage inverter will keep at OFF state. The output nodes at the posterior stage will not be charged, so the following stages can maintain the correct outputs.

On the basis of the above analysis, we can see that the proposed design can mitigate the SET effectively. For an ion striking at a PMOS, a minimum of one output node can keep at the proper logic level. The MOSFETs at the posterior stage might be all turned off after striking, which is able to make the transient caused by an ion striking no longer propagating away. So, the last output of the proposed structure will be correct, irrespective of the struck PMOS is turned off or conducted on. With regard to an ion striking at a NMOS, the proposed inverter chain can also achieve an effective SET mitigation. Owing to the parallel output nodes design, the transient can not turn on the PMOSs and turn off the NMOSs at the posterior stage at the same time. So, it will be filtered out. The final output can be correct steadily.

In addition to the above, the proposed design can prevent the SET pulse generated at any stage from disturbing the eventual output of the inverter chain, as long as the pulse is not generated at the eventual output node.

3 Simulation details

Sentaurus TCAD from Synopsys is adopted to perform the layout design and device simulation in the present work. The 65 nm bulk CMOS technology is used in this work. The W/L ratios of NMOSs and PMOSs which we made use for simulation are both 140 nm/65 nm. Besides, the doping profiles of the devices are calibrated to the 65 nm commercial process for well matched electrical characteristics, and the calibration results have been presented in Fig. 2.

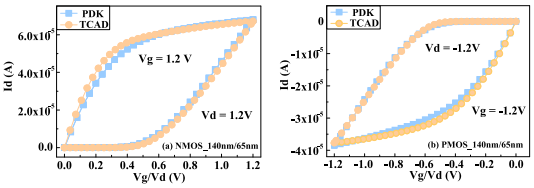

Fig. 2. Id-Vg and Id-Vd curves of commercial process design kit (PDK) and TCAD. (Id is the current of the drain, Vg is a representation of the voltage of the gate, and Vd means the voltage of the drain.)

The devices are built on a $20 \times 20 \times 20\ \mu m^3$ substrate having a constant doping of $1 \times 10^{16}\ cm^{-3}$. The doping profile of the P+ deep well shows the Gaussian distribution and the peak doping concentration is $1 \times 10^{18}\ cm^{-3}$.

Different structures of six stages inverter chain are made for comparison in the simulations, which are the conventional inverter chain, in addition to the inverter chain of source-isolation approach, the duplicated inverter chain with C-element and the proposed parallel output nodes inverter chain design. The modeling of the

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transistors in the second stage of the four inverter chains is performed with the help of a TCAD numerical model, and the other transistors made use of the SPICE model. The ion strikes the sensitive MOSFET of the second stage at the center of the drain. And the LET value being kept constant along the heavy ion track is assumed in the present work. The ion track length and the radius are set to 10 μm and 0.05 μm, correspondingly. The striking time is set to 50 ps.

The MOSFETs placement of the second stage inverter of the proposed approach is shown in Fig. 3. The x-z plain and the +y-axis are parallel and vertical to the surface of the cell, respectively. Although the proposed design has area penalty, it can mitigate the SET effectively.

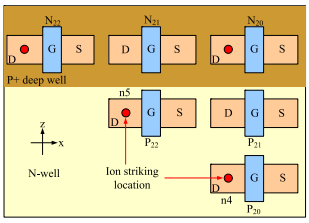

Fig. 3. The MOSFETs placement of the second stage inverter of the proposed design.

4 Simulation results

4.1 P-hit

1) We assume that the input signal n1 is at low level, thus, the outputs of the second stage are at low level. With an ion that has LET of 40 MeV·cm^2/mg striking at the PMOS vertically, the simulation results of three designs are shown in Fig. 4.

For conventional inverter chain, from Fig. 4(a) we can see that the voltage transient occurs immediately after an ion striking, and the transient pulse propagates through the chain completely. For the inverter chain of source-isolation approach, as shown in Fig. 4(b), the ion striking still causes voltage variation at the struck node. But the amplitude of the pulse is basically below VDD/2, which means the logic level is not changed. Thus, the eventual output is stable.

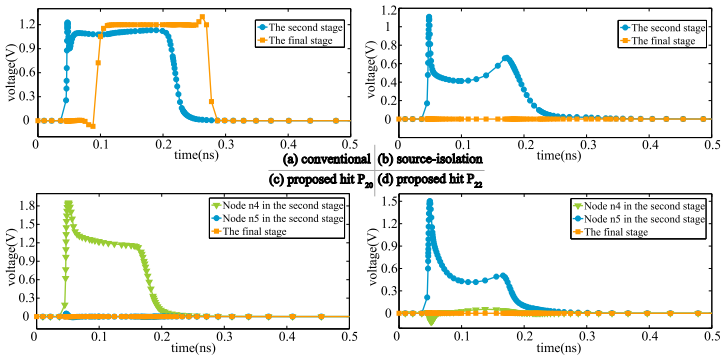

Fig. 4. SET pulse waveforms at output nodes of the second stage and the final stage when an ion strikes at the OFF PMOS.

With regard to the proposed design, in a case where the struck PMOS is P_{20}, the SET pulse is generated as shown in Fig. 4(c). So, the PMOSs at the posterior stage

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inverter are changed to OFF state. However, owing to the parallel output nodes structure, the voltage of node n5 stays at logic "0", so the NMOSs at the posterior stage inverter continue to be at OFF state. The output nodes at the posterior stage inverter can hold the potential. The stable final output indicates that the proposed structure is an effective design for SET pulse mitigation.

In a case where the struck PMOS is P_{22}, because of the stacked PMOSs and isolation technique that used in layout, the parasitic BJT is broken, and the bipolar effect is lowered significantly. Besides, N_{21} is turning on, and it can discharge the source of P_{22}, so the amplitude of SET pulse is decreased further. From Fig. 4(d) we can see that the amplitude of transient pulse is lowered substantially after striking. The ion striking can not change the logic level of node n5. The posterior stage to the last stage can keep correct outputs.

We assume that the ion with different LET values strikes the PMOS vertically. Fig. 5 summarizes the W_{SET} at the terminal of the inverter chains. With the increase in the LET value of the ion striking, the disturbance to the conventional inverter chain caused by SET gets progressively greater, but the proposed inverter chain can maintain a correct output throughout.

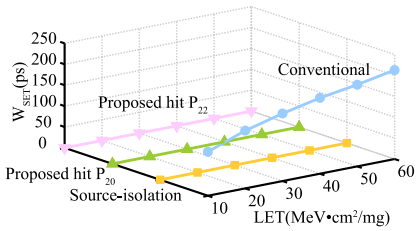

Fig. 5. W_{SET} of the final outputs for the inverter chains when the ion strikes at the OFF PMOS vertically.

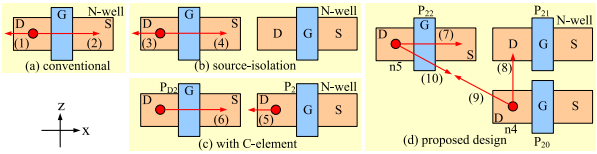

Fig. 6. The projection directions of the ion striking in the x-z plane.

We also study the impact of the ion strike angles on the circuits. Angle 60° is widely used in simulations to evaluate the dependence of ion striking angle on SET [13, 14, 15]. So, in the angle striking simulations, the angle between the direction of ion striking and the +y-axis is set to 60°. Fig. 6 shows the projection directions of the incident ion in the x-z plane. For the conventional inverter chain, striking (1) and striking (2) mean the projection direction of ion striking in the x-z plane are along with the −x-axis and the +x-axis, respectively. Striking (3) and striking (4) of the inverter chain of source-isolation approach as well as striking (5) and striking (6) of the duplicated inverter chains with C-element have the same meanings. In Fig. 6(c), P_2 and P_{D2} represent the PMOS of the second stage of the original inverter chain and the duplicated inverter chain, respectively. For the proposed design, striking (7) and striking (8) mean the projection direction of ion striking in the x-z plane are along with the +x-axis and the +z-axis, respectively. Striking (9) represents that the projection direction of ion striking in the x-z plane is from the

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center of drain of P_{20} to the center of drain of P_{22}. The projection direction of ion striking in the x-z plane that is from the center of drain of P_{22} to the center of drain of P_{20} is marked as striking (10).

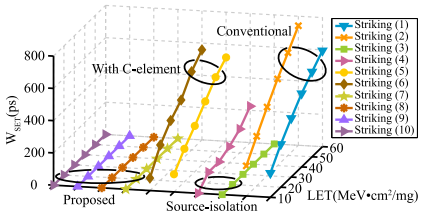

Fig. 7. W_{SET} of the final outputs for the inverter chains when the ion strikes at the OFF PMOS with angle 60°.

Fig. 7 compares the W_{SET} at the terminal of different structures for the simulations of ion striking with angle 60°. We can see that the conventional structure has a bad performance when the ion strikes with angle 60°, and the W_{SET} gets wider owing to the rise of the LET value. As for the inverter chain of source-isolation approach, the simulation results of striking (4) are disappointed. The SET pulse occurs at the final output. With regard to the duplicated inverter chains with C-element, the ion striking with angle 60° disturbs both the signals of the original inverter chain and the duplicated inverter chain. The disturbance propagates to the final output, and the SET pulse gets wider with the increase in the LET value. But the proposed design can eliminate the SET pulse and maintain a stable output all along.

2) We assume that the input signal n1 is at high level, thus, the outputs of the second stage are at high level. With an ion that has LET of 50 MeV·cm^2/mg striking at the PMOS vertically, the simulation results of three designs are shown in Fig. 8.

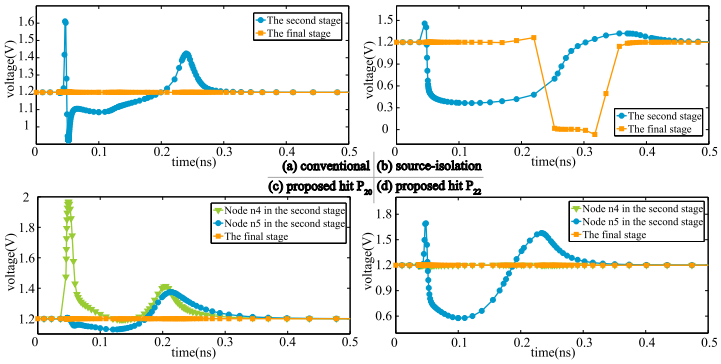

Fig. 8. SET pulse waveforms at output nodes of the second stage and the final stage when an ion strikes at the ON PMOS.

For conventional inverter chain, as presented in Fig. 8(a), the ion striking causes voltage variation at the struck node, but the logic level is not changed. Thus, the final output of conventional inverter chain is stable. With regard to the inverter chain of source-isolation approach, the potential of the struck drain decreased to low level rapidly. As shown in Fig. 8(b), the negative pulse propagates to the final stage with no doubt.

However, for the proposed inverter chain, in a case where the struck PMOS is P_{20}, we can see that the voltage variation occurs in Fig. 8(c). But the logic level still

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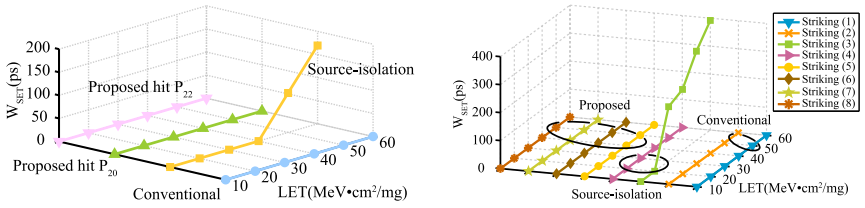
stays at "1", and the eventual output is stable, as might be expected. In a case where the struck PMOS is P_{22}, due to the drawback of isolation technique, from Fig. 8(d) we can see that the voltage of the struck node begins to drop after striking. Even if the voltage of node n5 manifests a decline to low level, node n4 keeps at high level. The NMOSs of the posterior inverter are turned off, but the corresponding PMOSs stay at OFF state, so the outputs of the posterior inverter can hold the logic level. The disturbance can not affect the eventual output.

We assume that the ion with different LET values strikes the PMOS vertically, and the simulation results are presented in Fig. 9(a). When the value of LET is 60 MeV·cm^2/mg, for the inverter chain of source-isolation approach, the width of negative pulse is 169.4 ps. But the proposed structure can eliminate the negative pulse all along.

The simulation results of ion striking with angle 60° are presented in Fig. 9(b). The simulation results of striking (3) show that the inverter chain of source-isolation approach has a bad performance. On the contrary, the proposed inverter chain can hold a correct output right along.



(a) vertically (b) with angle 60°

Fig. 9. W_{SET} of the final outputs for the inverter chains when the ion strikes at the ON PMOS.

4.2 N-hit

As mentioned above, if the ion strikes at the drain of NMOS while the potential of drain is at high level, the potential of drain will get lowered, and the logic level might change to logic "0". So, we mainly discuss that case.

We assume that the input signal n1 is high, thus, the outputs of the second stage are at high level. With an ion that has LET of 30 MeV·cm^2/mg striking at the NMOS vertically, the simulation results of three designs are shown in Fig. 10.

For the conventional inverter chain as well as the inverter chain of source-isolation approach, just as shown in Fig. 10(a) and Fig. 10(b), the voltage of the output of the second stage drops to low level immediately. The final outputs of the two structures are both disturbed badly.

As regards the proposed structure, if the ion hits the drain of N_{20}, the negative pulse also occurs at the struck node, which is shown in Fig. 10(c). Signal n4 drops to logic "0", it will conduct on the PMOSs of the posterior inverter. But the parallel output nodes design can keep signal n5 at high level, so the NMOSs of the posterior inverter will stay at ON state. Therefore, the amplitude of transient pulse, which is likely to occur at the output node of the posterior inverter, can be reduced significantly. The stable final output indicates that the voltage variation is eliminated as the transient propagates away. Fig. 10(d) presents the results of the ion

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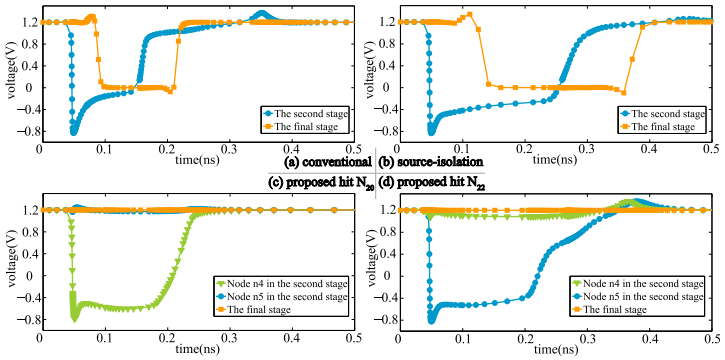

Fig. 10. SET pulse waveforms at output nodes of the second stage and the final stage when an ion strikes at the NMOS.

hitting the drain of N_{22}. The voltage of n5 manifests a decline to low level, which will turn off the NMOSs of the third stage. However, the high signal n4 can keep the corresponding PMOSs at OFF state. Thus, the outputs of the third stage can hold the potential. And the final output can be correct and stable as usual.

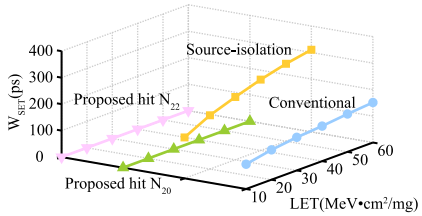

Fig. 11. W_{SET} of the final outputs for the inverter chains when the ion strikes at the NMOS vertically.

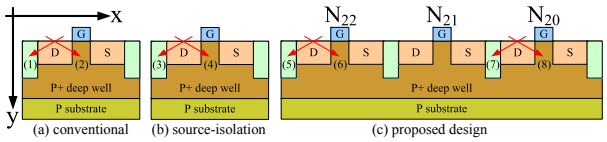

Fig. 12. The directions of the incident ion.

We assume that the ion with different LET values strikes the NMOS vertically, and the simulation results are presented in Fig. 11. We can see that the two existing techniques display disappointing performance. The final outputs are totally disturbed by the negative SET pulses, and the pulses get wider with the increase in the value of LET. But the proposed design is capable of eliminating the SET pulse effectively, and the results in Fig. 11 indicate that no pulse appears at the terminal of the proposed inverter chain.

The striking angle of N-hit is also studied. Fig. 12 presents the ion striking directions of the three designs, the angle between the direction of ion striking and the +y-axis is 60°. Fig. 13 compares the simulation results of this paper with the two existing techniques. We can see that the simulation results of the two existing techniques are disappointing, and the SET pulses of the final outputs of the two existing techniques are widened with the increase in the value of LET. But the proposed design shows a much better performance than the other designs, whose final output is stable all along.

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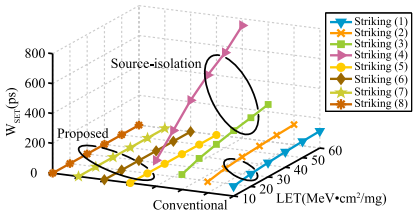
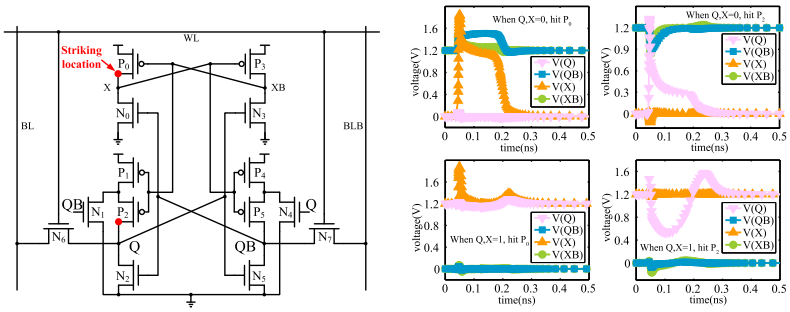


Fig. 13. W_{SET} of the final outputs for the inverter chains when the ion strikes at the NMOS with angle 60°.

5 Extension of the proposed approach

In the discussion done so far, the proposed approach was used to improve the inverter chain as regards the SET mitigation. In the extension, the proposed approach is also found to be effective in radiation hardening in the circuits with the structure like inverter chain. We design a SRAM cell whose storage structure is based on the proposed approach, and the schematic is shown in Fig. 14(a). We assume the voltage of WL is logic "0", then the nodes Q, QB, X, and XB can hold their states. With an ion that has LET of 60 MeV·cm^2/mg striking at the PMOS vertically, the simulation results are presented in Fig. 14(b). The ion striking still causes the voltage variation at the struck node, but the node can recover to the original state.



(a) schematic (b) simulation results

Fig. 14. SRAM bit-cell using the proposed approach.

6 Conclusion

This paper proposes a parallel output nodes inverter chain design to achieve SET pulse mitigation. The structure of parallel output nodes and layout-level optimization design can harden the output nodes and keep the final output from being disturbed by the SET pulse. The tolerance of SET is evaluated in 65 nm CMOS technology. Compared with the three existing designs of inverter chain, for P-hit simulations, the proposed inverter chain can maintain a correct and stable output no matter the potential of the struck node is at high level or low level. For N-hit simulations, the proposed inverter chain also performs better than the two existing approaches in suppressing the voltage variation that caused by ion striking. Moreover, for the SET pulse that is generated in any stage but the last stage, the proposed design is capable of eliminating it effectively. In addition, the proposed approach is also observed as being effective in the circuits with the structure similar to inverter chain.

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