

LETTER

A charge pump system with new regulation and clocking scheme

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Abstract A novel charge pump system with new regulation and clock generating techniques is proposed and verified in a 0.13 μm CMOS process. Rather than generating the reference voltage by band-gap reference (BGR) and the detected voltage by high voltage divider in the conventional regulation, both voltage reference and division of proposed pump system are implemented by single new circuit. Besides, the conventional oscillator for clock input of charge pump system is removed while an adaptive clock generation scheme is introduced to reduce the power consumption and shrink the system size. The experiment results show that the pump system can produce a stable and smooth output with a small ripple, and the high output accuracy is comparable to the conventional solution equipped with BGR. Moreover, the power consumption of the pump controlling is reduced by about 80% while the size of pump system is decreased by about 25%. Therefore, the proposed regulated charge pump (RCP) is very suitable for ultra-low power and high precision applications, for example, the embedded nonvolatile memories (eNVMs).

Keywords: charge pump, nonvolatile memory, clock generator, high voltage generating

Classification: Integrated circuits

1. Introduction

The common solid-state nonvolatile memories require charge pump system to generate high voltage for read and write operations, *e.g.* the split-gate embedded Flash memory requires 2.8V voltage for read operation, 8V voltage supply for program operation and 12V for erase operation [1, 2, 3]. However, the area and power of eNVMs are mainly consumed by internal charge pump system [4, 5, 6]. And the needs of small chip area and ultra-low power eNVMs, which increases battery lifetime and reduces the cost, have become the key design aspects for portable equipment and internet-of-things (IoT) [7, 8, 9]. As a result, the advanced pump structures with smaller size and higher efficiency have been extensively researched [10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. Meanwhile more attentions are paid to the regulation techniques [20, 21, 22, 23, 24, 25] or the clock inputs [26, 27, 28, 29, 30, 31] of charge pumps, since the regulation and clocking schemes

have also become more and more crucial to reduce power and chip size of pump system [4, 22].

Fig. 1(a) and Fig. 1(b) show the circuit diagram of a conventional regulated charge pump (RCP) system including a three-stage CMOS charge pump and a controller. And the conventional controller is composed of oscillator, voltage divider, band-gap reference and voltage comparator [32]. The oscillator generates the clock for the charge pump. Meanwhile, the BGR provides an accuracy voltage reference which will be compared to the detected voltage of charge pump output. As displayed in Fig. 1(b), the voltage V_{DET} detected via voltage divider can be expressed as $V_{OUT}R_7/(R_7 + R_8 + R_9)$. Fig. 1(c) shows the waveforms of conventional RCP system. When the pump system is enabled and V_{DET} is lower than V_{REF} , the comparator output EN will be high to enable RCP and oscillator. By contrast, when V_{DET} is higher than V_{REF} , EN will be low to stop RCP and oscillator. As a result, V_{DET} is stabilized around V_{REF} and RCP output V_{OUT} approximately equals to $V_{REF}(R_7 + R_8 + R_9)/R_7$. In addition, a large decoupling capacitor C_{dcap} is required to reduce output ripple.

When it comes to low power consumption applications (low pump loading), the BGR and the oscillator (pump controlling) consume the majority of power and area of charge pump system. And, it is much difficult to reduce both of their power consumption and circuit size at same time. However, it is observed that sophisticated oscillator is not necessary, because the RCP is not frequently driven by clock and CMOS pump is not sensitive to clock duty cycle [19, 31]. In addition, the operational amplifier of comparator and the amplifier inside BGR are redundant in the closed loop of charge pump system. Hence, optimizing the regulation and clocking strategies may be a potential solution to reduce the power and area of pump system. In this paper, a new charge pump system with novel regulation and new clock generating schemes is proposed to reduce the chip size and power consumption. While, the precision of pump output is kept and the small output ripple is achieved. The rest of the paper is organized as follows. Section 2 presents the circuit structure, regulation and clocking strategies of the new pump system. In Section 3, experiment results are presented and analyzed. Conclusions are then given in Section 4.

2. Proposed charge pump system

2.1 Circuit structure and regulation scheme

Fig. 2(a) illustrates the structure of the proposed charge pump system and Fig. 2(b) summaries the different regulation solutions between the conventional RCP and the

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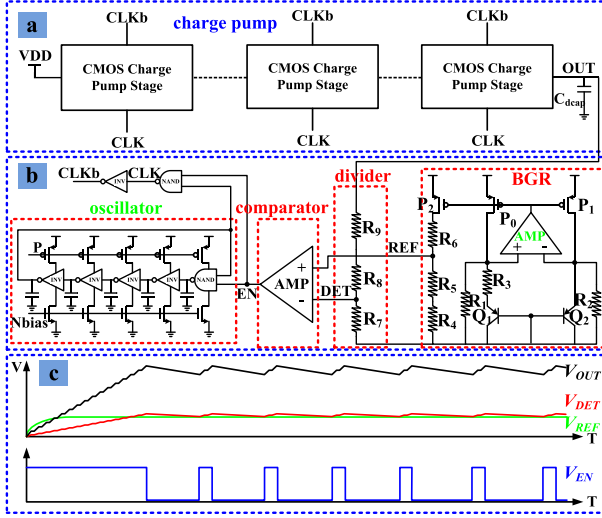


Fig. 1. Conventional regulated charge pump system: (a) three-stage CMOS charge pump; (b) The conventional pump controller circuit; (c) Voltage waveforms of conventional charge pump system.

proposal. Rather than generating the reference voltage (V_{REF}) by the dedicated BGR and the pump output division (V_{DET}) by the dedicated voltage divider, the proposed PCP system use single circuit to implement both the voltage division and reference with one comparator (amplifier). In addition, the oscillator is no longer required in this system. But, an easy pulse generating circuit is introduced to provide the clock for this low-power charge pump system (its detailed operations are described in section 2.2). Compared with conventional solution shown in Fig. 1, the new system area is reduced by the size of one amplifier (inside the BGR) and the oscillator.

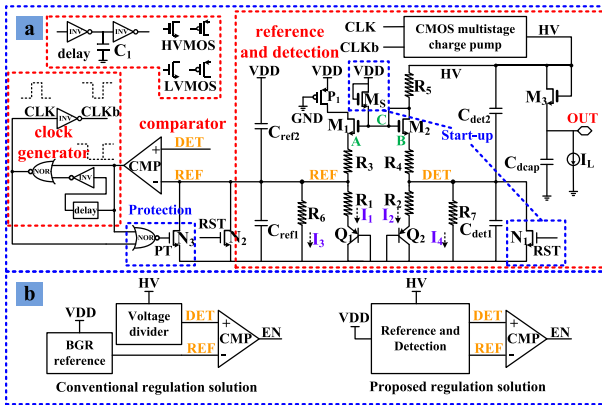


Fig. 2. Proposed charge pump system: (a) The proposed charge pump system circuit; (b) The comparison of regulation solutions.

As presented in Fig. 2(b), both of the voltages at node DET and REF (V_{DET} and V_{REF}) of proposed pump system are determined by the pump output. The detailed relation between V_{DET} and V_{REF} depending on pump output V_{OUT} is demonstrated below. According to Fig. 2(a), if the system is active, V_{DET} and V_{REF} can be expressed as

$$V_{REF} = I_1 R_1 + V_{BE1} = I_1 R_1 + V_T \ln(n I_1 / I_S) \quad (1)$$

$$V_{DET} = I_2 R_2 + V_{BE2} = I_2 R_2 + V_T \ln(I_2 / I_S) \quad (2)$$

where V_{BE} is base-emitter voltage of bipolar, I_S is saturation current of bipolar Q_2 , $V_T = KT/q$ and $nQ_1 = Q_2$ (n is 16 in this design). Pump output HV is much higher than supply V_{DD} in normal operation, while V_C is designed close to V_{DD} . Therefore, M_1 and M_2 are both operated at saturation region and currents can be presented as

$$I_1 + I_3 = \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} (V_C - V_A - V_{th1})^2 \quad (3)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} [V_C - V_{REF} - (I_1 + I_3) R_3 - V_{th1}]^2$$

$$I_2 + I_4 = \frac{1}{2} \mu_n C_{ox} \frac{W_2}{L_2} (V_C - V_B - V_{th2})^2 \quad (4)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W_2}{L_2} [V_C - V_{DET} - (I_2 + I_4) R_4 - V_{th2}]^2$$

$$I_3 = \frac{V_{REF}}{R_6} = \frac{I_1 R_1 + V_{BE1}}{R_6} \quad (5)$$

$$I_4 = \frac{V_{DET}}{R_7} = \frac{I_2 R_2 + V_{BE2}}{R_7} \quad (6)$$

where μ_n , C_{ox} , V_{th} , W and L with subscript denote the electrons mobility, gate oxide capacitance, threshold voltage, width and length of M_1 and M_2 . The pump output voltage is the sum of voltage drop on R_5 , M_2 , R_4 , R_2 and Q_2 . And the pump output HV minus the voltage drop on M_3 ($V_{GS,M3}$) equals the system output V_{OUT} , which can be written as

$$V_{OUT} = V_{BE2} + I_2 R_2 + (I_2 + I_4)(R_4 + R_5) + (V_C - V_B) - V_{GS,M3} \quad (7)$$

In equation (7), $(V_C - V_B)$ could be simplified to V_{th2} and $V_{GS,M3}$ is simplified to V_{th3} , since M_1 , M_2 and M_3 are selected with large width-to-length ratio. And the difference between V_{th2} and V_{th3} , induced by mismatch and body effect, can be further ignored compared to the large value of V_{OUT} . Therefore, V_{OUT} can be rearranged as

$$V_{OUT} = V_{BE2} + I_2 R_2 + \left(I_2 + \frac{I_2 R_2 + V_{BE2}}{R_7} \right) (R_4 + R_5) \quad (8)$$

In this design, $M_1 = M_2$, $R_1 < R_2$, $R_3 = R_4$ and $R_6 = R_7$. When $V_{DET} = V_{REF}$, $I_3 = I_4$ can be easily derived from (5) and (6). And then, $I_1 = I_2$ can be derived from (3) and (4). Defining $\Delta R = R_2 - R_1$, $I_0 = I_2$ and $V_{OUT0} = V_{OUT}$ under the condition of $V_{DET} = V_{REF}$, I_0 and V_{OUT0} can be then calculated as

$$I_0 = \frac{V_T \ln n}{R_2 - R_1} = \frac{V_T \ln n}{\Delta R} \quad (9)$$

$$V_{OUT0} = \left(\frac{R_4 + R_5}{R_7} \frac{R_2}{\Delta R} + \frac{R_4 + R_5}{\Delta R} + \frac{R_2}{\Delta R} \right) V_T \ln n + \left(\frac{R_4 + R_5}{R_7} + 1 \right) V_{BE2} \quad (10)$$

When $V_{DET} < V_{REF}$, $(I_1 + I_3) < (I_2 + I_4)$ and $I_3 > I_4$ can be demonstrated by (3) to (6). Taking these inequations into account, we can then get $I_1 < I_2$. Next, $I_2 < I_0$ can be obtained by substituting $V_{DET} < V_{REF}$ and $I_1 < I_2$ into (1) and (2). Finally, $V_{OUT} < V_{OUT0}$ can be concluded from (9) and (10). If $V_{DET} > V_{REF}$, on the contrary, $V_{OUT} > V_{OUT0}$ could also be proved by similar derivation. In this design, the value of V_{DET} and V_{REF} is determined by V_{OUT} . Thus, the relation between V_{DET} and V_{REF} can be concluded as: a) $V_{DET} = V_{REF}$ when $V_{OUT} = V_{OUT0}$; b) $V_{DET} < V_{REF}$ when $V_{OUT} < V_{OUT0}$; and c) $V_{DET} > V_{REF}$ when $V_{OUT} > V_{OUT0}$.

According to above conclusions (a)–(c), by comparing V_{DET} with V_{REF} to control the clock generator and charge pump, the pump system output is regulated around V_{OUT0} . Therefore, the proposed regulation solution is functional, and the circuit size is smaller than conventional solution with divider and BGR. Furthermore, the resistor R_5 , R_6 and R_7 (R_6 is kept same to R_7) can be trimmed at the same time to achieve the desired value of pump output, according to (10). Meanwhile, negative or positive temperature coefficient can be effectively compensated to obtain temperature independent output. Also, V_{OUT0} could be independent on V_{DD} , since the voltage of node C (V_C) is designed close to V_{DD} to reduce the mismatch between M_1 and M_2 . Therefore, the proposed charge pump can provide precise and wide-range voltage according to different $R_5 \sim R_7$ values. For example, Table I displays some output voltages with corresponding resistance values.

Table I. Default resistance for different output voltage.

Output voltage	R_2	R_3, R_4	R_5	R_6, R_7
2.5 V	2 Δ R	4 Δ R	15 Δ R	Unuesd
8 V	2 Δ R	4 Δ R	39.5 Δ R	9.5 Δ R
12 V	2 Δ R	4 Δ R	62.5 Δ R	8.5 Δ R

2.2 Self-adaptive clock generating scheme

No dedicated oscillator circuit is used in the proposed charge pump system, while a new clock generator is introduced with an easy delay circuit and some logic gates (Fig. 2). Fig. 3 shows the transient waveform of proposed RCP system including start-up, normal operation and protection phases controlled by the new clocking scheme. During normal operation, pump output drops with the time due to the pump loading I_L . Because the comparator is designed with high precision to detect the minute difference between V_{REF} and V_{DET} , the comparator output switches to low once V_{OUT} drops to slightly lower than V_{OUT0} . As displayed in Fig. 2(a), the falling edge of the comparator will produce a positive pulse at node CLK and a negative pulse at node CLKb by the clock generator. The charge pump is then driven by the pulse to boost the output voltage to be higher than V_{OUT0} (comparator output recovers to high). Thus, V_{OUT} is dynamically stabilized around V_{OUT0} (normal operation phase of Fig. 3). Because the clock is triggered when V_{OUT} drops to V_{OUT0} , the equivalent frequency of clock is adapted to the output loading.

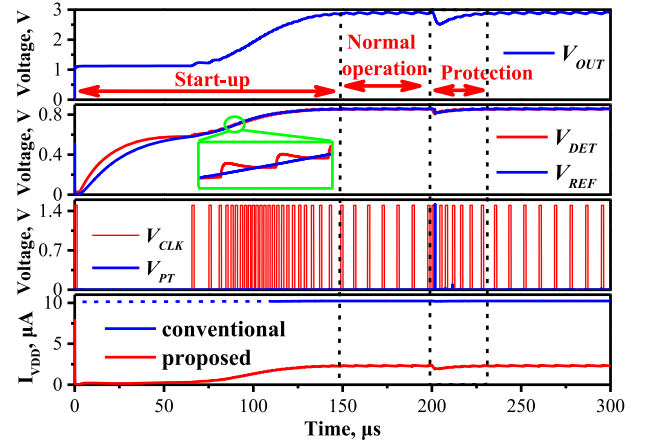


Fig. 3. Transient waveform of the proposed charge pump system.

During the start-up phase, a reset pulse is firstly applied to N_1 and N_2 to set $V_{REF} = V_{DET} = 0$. Then, the diode-connected transistor M_S provides a current path to turn on M_1 and M_2 . And the currents flowing through M_1 and M_2 charge the nodes REF and DET, respectively. Due to the fact that C_{det1} and C_{det2} are set much smaller than C_{ref1} and C_{ref2} , V_{DET} is increased much faster than V_{REF} (charging currents through M_1 and M_2 are similar). However, V_{DET} is finally lower than V_{REF} under the condition $V_{OUT} < V_{OUT0}$, as derived in previous section. Thus, comparator output firstly switches to high level and then turns to low level. The falling edge of the comparator will generate a clock pulse to raise the pump output. Next, V_{DET} and V_{REF} are further increased by V_{OUT} rising, with the process where V_{DET} firstly exceeds V_{REF} and then lags behind V_{REF} . The clock pulse is produced again for the charge pump. Because of the differences between V_{DET} and V_{REF} on the rising speed and final value, the above process will be repeated until $V_{OUT} > V_{OUT0}$ (start-up phase in Fig. 3).

By adopting N_3 in Fig. 2, a protection strategy is introduced to prevent the system entering false state when there is an instantaneous large loading at OUT. As shown in Fig. 3, the false state means that V_{OUT} drops to lower than V_{OUT0} but could not be boosted to V_{OUT0} within one clock pulse. As a result, the comparator will keep low and no more clock pulse will be generated. In this case, N_3 will be turned on to discharge the node REF until $V_{DET} > V_{REF}$. Next, similar to the procedure of start-up, V_{OUT} will then recover to V_{OUT0} .

Besides the small area and ultra-low power, another advantage of this clock generating circuit is the small pump output ripple. The standard expression for output ripple ΔV can be given by

$$\Delta V = \frac{I_L \Delta t}{C_L} \quad (11)$$

where C_L is the capacitance loading of pump output including decoupling capacitor C_{decap} , I_L is the output loading, and Δt is the period of the ripple [30]. As displayed in Fig. 2(a), the clock for pump is immediately generated at the falling edge of the comparator. By com-

parison, the conventional solution needs additional time to turn on the oscillator, resulting in a longer Δt and a larger ripple. Therefore, the proposed RCP is able to achieve a smooth output with a small decoupling capacitor C_{dcap} .

3. Experiment results

An eFlash memory testing chip was fabricated in HHGrace 130 nm CMOS process to demonstrate the proposed RCP system. Fig. 4 shows the microphotograph of the eFlash testing chip and the summary of power and area of pump system. The size of proposed RCP system is 0.026 mm^2 , which is decreased by 25% compared to conventional RCP system with same pump size. The power consumed by the pump controlling (excluding pump) is about $2.2 \mu\text{A}$, which is decreased by 80% compared to conventional RCP with the same current loading on pump output. Fig. 5 shows the measured waveform of the RCP output during read operation including start-up stage and normal operation stage. The start-up time is about $100 \mu\text{s}$ owing to the low-power feature of this RCP system. Also, the stable output (2.83 V) reaches the design targets of read operation ($2.7 \text{ V} \sim 3 \text{ V}$), when the RCP system works at normal operation stage. Fig. 6 presents the output voltage of the conventional and the new RCP for program operation ($8 \text{ V} \sim 8.2 \text{ V}$) after the calibration of $R_5 \sim R_7$. Measurement results show that the output voltage of proposed pump system has a low temperature coefficient of $85 \text{ ppm}/^\circ\text{C}$ with the temperature range from -40°C to $+125^\circ\text{C}$. Meanwhile, the line sensitivity of the output is $3.6\%/V$ only with supply range from 1.35 V to 1.65 V . The precise RCP output is suitable for the eFlash memory and comparable to the conventional RCP with BGR.

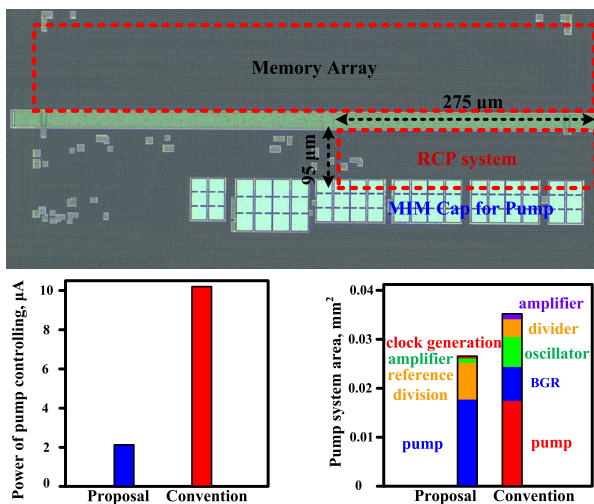


Fig. 4. Microphotograph of eFlash testing chip and the summary of power and area of pump system.

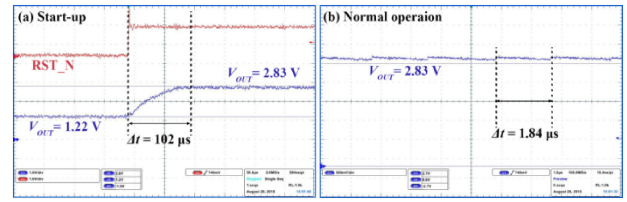


Fig. 5. Measured waveform of proposed RCP output for read operation: (a) Start-up stage; (b) Normal operation

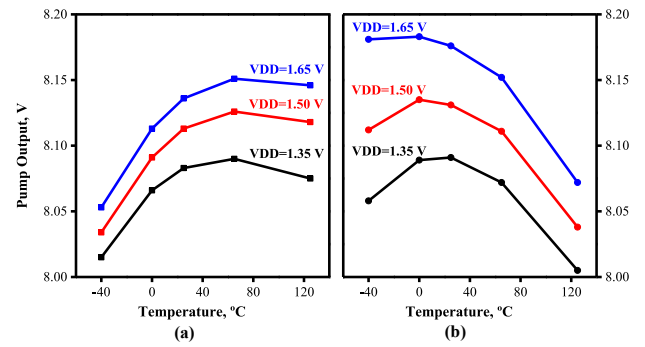


Fig. 6. Measured program voltage related with temperature and supply: (a) conventional RCP output; (b) proposed RCP output

Table II. Comparison of regulated high-voltage charge pump.

	Luo [31]	Tsai [12]	Brandon [30]	Ravi [13]	This Work
Process (μm)	0.18	0.18	0.35	0.16	0.13
V_{IN} (V)	3.3	1	2.5	3.3	1.5
V_{OUT} (V)	10.5	3–6	7.5–16	16	2.7–12
Stage	3	6	6	—	3–10
Size (mm^2)	1.3	0.5	0.069	1.65	0.026
Efficiency	69%	52%	34%	70%	49%
Ripple (mV)	260	39	18	160	36

Table II lists the performance comparisons among our regulated charge pump with the prior works [12, 13, 30, 31], which are capable of producing output voltages to higher than twice the supply voltage (*i.e.*, $V_{\text{OUT}} > 2V_{\text{DD}}$). The proposed RCP is realized by CMOS charge pump with bulk switching technique to achieve high power efficiency [14]. The results show the maximum output capability is 12 V and $0.6 \mu\text{A}$ with the high power efficiency of 49%, which is very suitable to eFlash memory in low-power applications. Additionally, a very small output ripple of 36 mV ($C_{\text{out}} \approx 20 \text{ pF}$) is obtained owing to the new clock generating scheme. Among these works, the proposed charge pump system has the smallest size while obtains a high power efficiency and a low output ripple.

4. Conclusions

In this paper, we have presented the design and results of a novel charge pump system for generating high voltage. New regulation and clocking schemes are introduced to cut down the power consumption and reduce the pump size. Experiment results show the proposed pump system can produce the stable and smooth output with a small ripple, and the precision of output voltage is comparable to the conventional RCP. Moreover, the power consumption of the RCP controlling is reduced by about 80% while the pump system size is decreased by about 25%.

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