

LETTER

A 140 GHz area-and-power-efficient VCO using frequency doubler in 65 nm CMOS

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Abstract This paper presents a compact, low-phase-noise and low-power D-band VCO with the tuning range from 140.1 to 143.5 GHz. To improve the area and power efficiency, we avoid using signal amplification and matching circuits in the VCO, where a 70 GHz LC oscillator is directly coupled to a frequency doubler. The layout of the transistors is optimized so that the signal loss and reflection are minimized. The proposed VCO fabricated in a 65 nm CMOS technology occupies the core area of 0.05 mm². It achieves the output power of –8 dBm and the phase noise of –108.2 dBc/Hz at 10 MHz offset with the power consumption of 24 mW from 1 V supply, which leads to the figure-of-merit (FoM) of –177.4 dBc/Hz.

Keywords: CMOS, D-band, frequency doubler, millimeterwave silicon RFICs, voltage-controlled oscillator (VCO)

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

Atmospheric attenuation shows several frequencies where radio-wave attenuation is minimized. The low atmospheric attenuation windows occur at around 35 GHz, 90 GHz, 140 GHz and 220 GHz in millimeter-band [1, 2]. Especially, the frequency around 140 GHz in D-band has a great potential and unique properties. This frequency band arises between two molecular absorption peaks of 119 GHz and 183 GHz and has low attenuation (1 dB/km), where the potential available bandwidth is large [1]. The frequency band from 141 to 148.5 GHz is allocated by the Federal Communications Commission (FCC) for fixed and mobile communication [3]. Thus this frequency band has been exploited for a lot of applications in various fields such as spectroscopy [4], radiometer [5], biosensor [6], imaging [7, 8], radar [9] and high-data-rate communication [10, 11, 12, 13].

For any of these systems, the oscillator that generates low-phase-noise millimeter-wave carrier is essential in order to efficiently transmit or receive the signal in D-band. At frequency higher than 100 GHz, however, a design of the CMOS voltage controlled oscillator (VCO) that realizes low phase noise with low power consumption is crucial to

have sufficient signal-to-noise ratio (SNR) requested by the system specifications. A fundamental VCO [14, 15, 16] is one of the straightforward choice to realize high power output with low power consumption. With a very simple structure its tuning range is often limited by parasitic capacitance of the transistors. Thus a varactor is usually used to maintain the tuning range, but its low quality factor (Q) at high frequency may heavily deteriorate the phase noise of the VCO. Several design techniques have been proposed to boost up the fundamental frequency of an oscillator. A VCO combining four coupled Colpitts oscillators was proposed in [17]. This circuit can generate high output power with increased power consumption. [18] proposed a VCO based on coupled oscillators in a loop configuration, which occupies a large area and tends to request a lot of power to generate a signal. One of the commonly-used methods to achieve better phase noise is to use a VCO for harmonic generation [19, 20]. The main drawback of these techniques is that the output power becomes low at higher harmonics and they often need more DC power to compensate it. A push-push architecture [21, 22] is also used to have more output power but it also leads to large area occupation due to the multiple VCOs. Though various other oscillation techniques such as frequency up-conversion [23] or quadrature coupling [24, 25] have been proposed to realize millimeter-wave output, to achieve low phase noise and low power consumption with a small area at high frequency is still challenging. One possible approach to overcome this is to use a VCO together with a multiplier. This topology has often been used in recent publications aiming for high efficiency and low phase noise [26, 27, 28, 29, 30].

In this paper, a compact 140 GHz VCO using frequency doubler that realizes low phase noise with low power consumption is proposed. We use a 70 GHz LC oscillator, which is directly coupled to a frequency doubler unlike the conventional VCO that uses matching networks in between the low-frequency oscillator and the multiplier. The prototype fabricated in 65 nm standard CMOS achieves the phase noise of –108.2 dBc/Hz at 10 MHz offset around 140 GHz with the power consumption of 24 mW from 1 V supply.

The rest of this paper is organized as follows. Section 2 presents the architecture and implementation of the proposed VCO. Then the measurement results of the D-band VCO is presented in Section 3. Finally, Section 4 concludes this paper.

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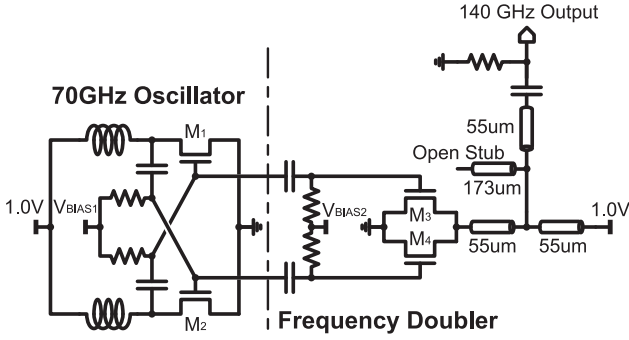


Fig. 1. Circuit diagram of the proposed D-band VCO.

2. Architecture of the proposed VCO

2.1 70-GHz fundamental LC VCO

The block diagram of the proposed VCO is shown in Fig. 1, where we use a 70 GHz fundamental LC oscillator, which is followed by a frequency doubler to generate 140 GHz. The 70 GHz oscillator has the RC biasing circuit for both M_1 and M_2 that enables us to tune their gate voltage V_G for frequency tuning. Although V_G and the drain voltage V_D are both assumed to be at the regulated supply through the inductors in the conventional cross-coupled VCO (CC-VCO), in this topology we can tune V_G and V_D independently. While all the transistors never leave the saturation region in the conventional CC-VCO, the transistors in our oscillator may operate in the triode region, which leads to class-C operation [31]. As a result, current noise from FETs can be greatly reduced. Here in this oscillator we use V_G to tune the oscillation frequency.

Figs. 2, 3, 4 and 5 summarize the simulated performance of the proposed oscillator, which is compared for reference with the conventional LC VCO using simple cross-coupled transistors without the biasing circuit. In these plots, to tune V_G of the cross-coupled transistors, V_{BIAS1} is swept in the proposed oscillator while V_{DD} is swept in the conventional one [26]. As shown in Fig. 2, both the oscillators are designed to have similar frequency tuning range for fair comparison. At the same time, the power consumption of them becomes roughly equal to each other as shown in Fig. 3. With this setup, Fig. 4 demonstrates that, by directly tuning V_G through the biasing circuit, the phase noise of the proposed oscillator is always lower than that of the conventional one. Clearly, the proposed oscillator achieves better Figure-of-Merit (FoM) throughout the frequency tuning range as shown in Fig. 5.

2.2 Entire architecture of 140-GHz VCO

For 140 GHz output, we employed a push-push frequency doubler with single-ended output followed by an output matching circuit as shown in Fig. 1. The transistors M_3 and M_4 are biased at around their threshold voltage through the dedicated biasing circuit to have the largest voltage amplitude at the 2nd harmonic frequency. The output matching circuit is composed of transmission lines and is tuned to pass signals around 140 GHz. A capacitor and a resistor at the output are used to cut DC component. The conventional D-band VCO based on a frequency doubler [26] used a

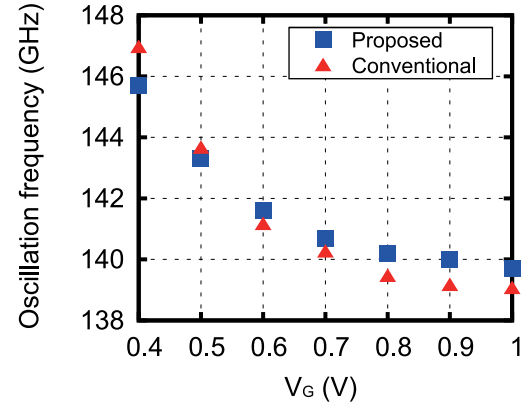


Fig. 2. Comparison of the simulated oscillation frequency between the VCOs with and without biasing circuit.

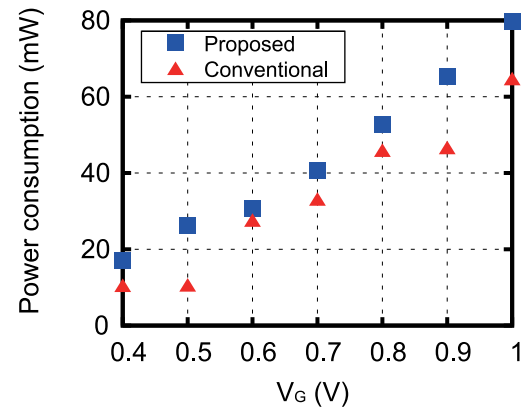


Fig. 3. Comparison of the simulated power consumption between the VCOs with and without biasing circuit.

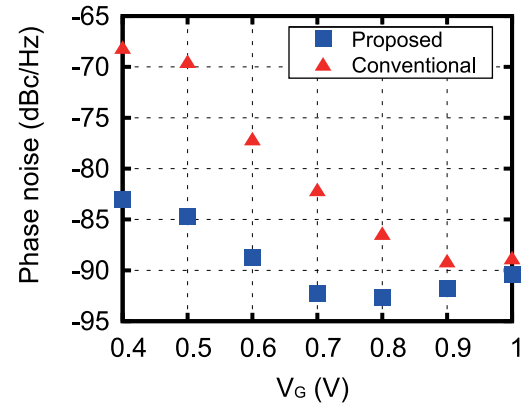


Fig. 4. Comparison of the simulated phase noise at 1 MHz offset between the VCOs with and without biasing circuit.

70 GHz oscillator whose differential outputs are amplified then supplied to the doubler. Since it requires an impedance matching circuit in-between each sub-circuit, it uses a total of 5 matching circuits that lead to a large area. In addition, signal loss through the on-chip passive components in the matching circuits has the non-negligible impact on the power efficiency. In the proposed VCO, on the other hand, VCO outputs are directly coupled to the doubler without internal signal amplification. With this structure, we can

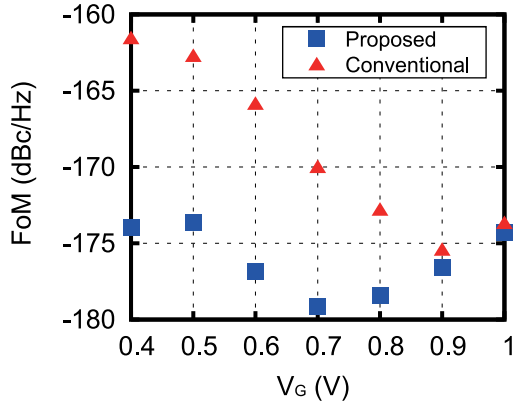


Fig. 5. Comparison of the simulated FoM between the VCOs with and without biasing circuit.

avoid area-consuming on-chip passive components for matching between sub-circuits as well as signal loss through them. In addition, since the 70 GHz VCO output nodes now do not see 50-Ohm loads, its power consumption can be drastically reduced while maintaining its oscillation frequency and amplitude. But to make this simple topology to be effective, we need careful design consideration for the signal transfer from the VCO to the doubler. To minimize signal reflection between these two blocks, we have integrated the transistors M_1 to M_4 including RC biasing circuits in close proximity. Figs. 6(a) and (b) show the placement and the layout of these devices, respectively. Especially for the 70 GHz signal paths, their placement and wirings are optimized to have minimum loss and reflection utilizing electromagnetic simulation with Integrand *EMX* [32, 33]. As a result, with a very simple structure, the proposed VCO realized D-band frequency with low power consumption and small area occupation.

3. Measurement result

Fig. 6(c) shows the chip micrograph of the proposed VCO, fabricated in a 65 nm standard CMOS. Due to the simplicity of the proposed VCO architecture, the core circuit, composed of the cross-coupled oscillator and the frequency doubler, occupies a compact area of $0.31 \times 0.16 \text{ mm}^2$.

The measurement setup is summarized in Fig. 7. First, the spectrum is measured with a signal analyzer Keysight N9030A through a frequency extension module VDI WR6.5SAX to find the oscillation frequency. The D-band 140 GHz output is successfully verified as shown in Fig. 8. As illustrated in Fig. 7(b), the phase noise is measured using a signal generator Keysight E8257D to supply 25 GHz LO signal for WR6.5SAX that works as a block down-conversion mode so that it down-converts the 140 GHz signal to ~ 10 GHz with minimum effect on the phase noise while maintaining sufficient signal power. Fig. 9 plots the measured frequency tuning range and phase noise at 10 MHz offset by changing V_{BIAS1} . This result confirms the frequency tuning range from 140.1 GHz to 143.5 GHz (2.4% tuning range). The measured phase noise plot at 140.4 GHz output is shown in Fig. 10. At 10 MHz offset, the phase noise of -108.2 dBc/Hz is

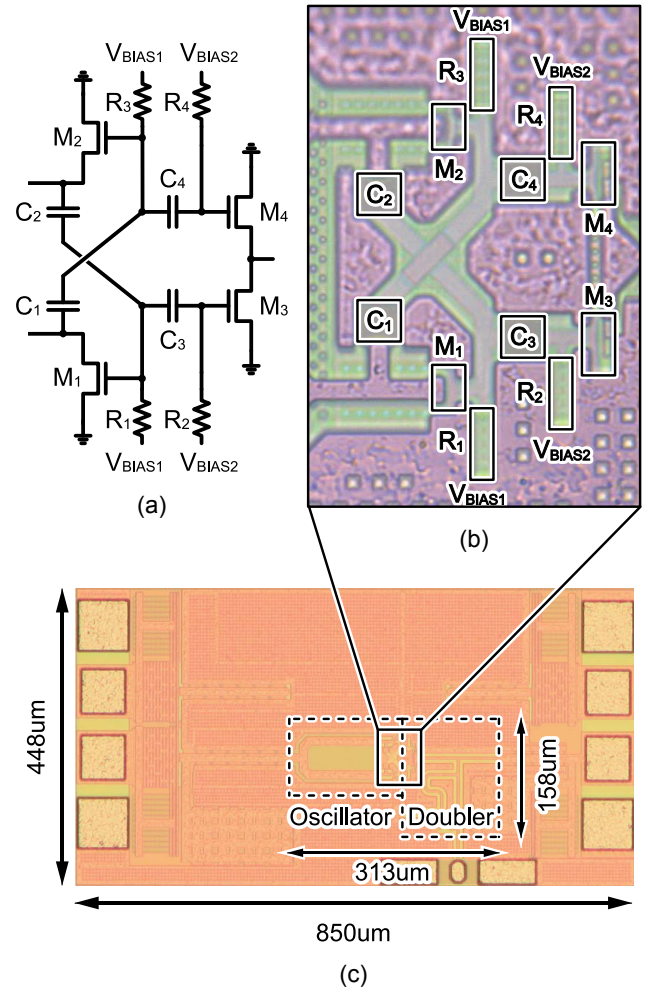


Fig. 6. (a) Layout configuration of the active and passive devices of the proposed VCO, (b) a micrograph of the devices and (c) the overall layout of the proposed VCO.

achieved. For the measurement of the output power, as shown in Fig. 7(c), we used a VDI Erickson PM4 power meter. As its sensor head has WR-10 waveguide, a taper is used to convert WR-6.5 from the waveguide probe to WR-10. The output power measured with this setup was -14 dBm . After compensating the insertion loss through an on-chip signal pad, a GSG probe and waveguides, the output power of the VCO is estimated to be -8 dBm . The total power consumption of the VCO is 24 mW from 1 V supply, where the 70 GHz oscillator and the doubler consume 15 mW and 9 mW, respectively. As a result, the proposed VCO achieves the FoM of -177.4 dBc/Hz . Table I compares the performance of the proposed VCO with state-of-the-art VCOs for the similar frequency range. Among them, thanks to the simple architecture of the proposed VCO with systematic design and careful layout optimization, it achieves the lowest power, low phase noise and a very small area at the same time.

4. Conclusion

In this paper we proposed the area-and-power-efficient 140 GHz VCO. In the proposed VCO, the LC oscillator outputs are directly coupled to the doubler without internal

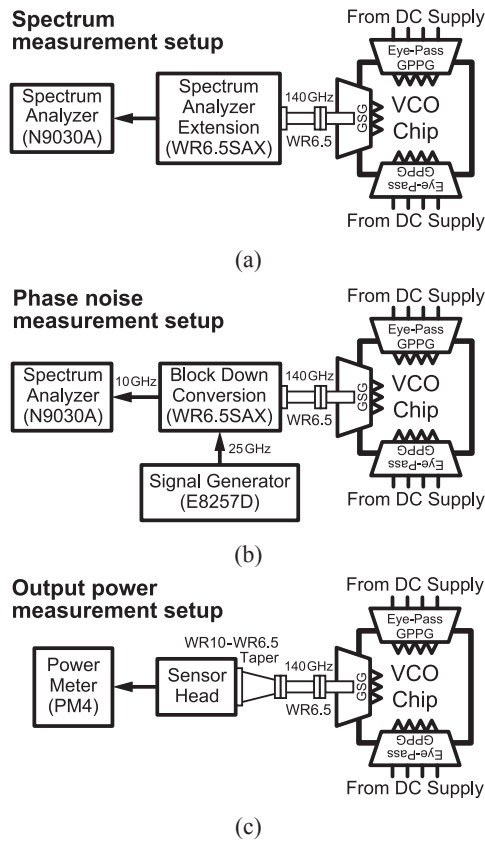


Fig. 7. Setups for (a) spectrum, (b) phase noise and (c) output power measurements.

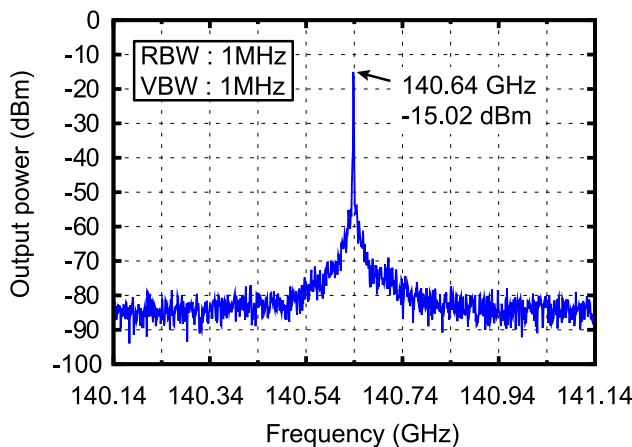


Fig. 8. Measured spectrum of the VCO output at 140 GHz.

signal amplifications or buffers, but with the optimized layout of the active and passive devices that minimizes the loss and reflection of the signal of interest. Fabricated in a 65 nm CMOS process, at 140 GHz, the VCO achieved the phase noise of -108.2 dBc/Hz at 10 MHz offset with low power consumption of 24 mW, which results in the FoM of -177.4 dBc/Hz.

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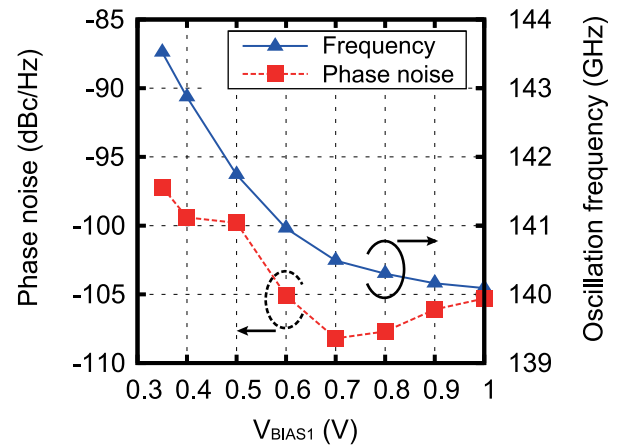


Fig. 9. Measured oscillation frequency and phase noise at 10 MHz offset by changing V_{BIAS1} .

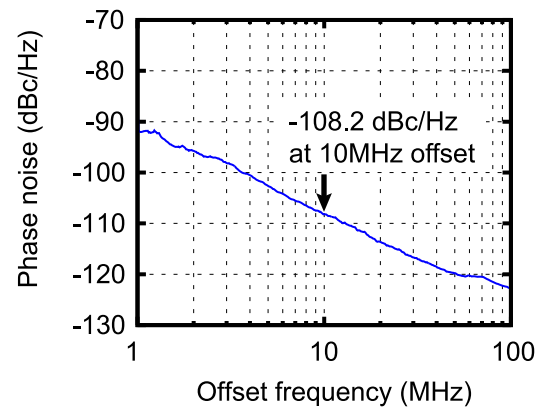


Fig. 10. Measured VCO phase noise at 140 GHz.

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Table I. Performance comparison with similar frequency oscillators.

Ref.	f_{osc} (GHz)	Process	P_{out} (dBm)	Tuning Range (%)	P_{diss} (mW)	PN@ f_{offset} (dBc/Hz)	FoM* (dBc/Hz)	Chip Size (mm ²)
[14]	175.6	130 nm SiGe	4.8	0.34	25.8	−101.7@1 MHz	−192.5	0.19**
[19]	190.5	130 nm SiGe	−2.1	20.7	183/294	−102.6@10 MHz	−165.6~	0.25
[20]	210	130 nm SiGe	1.4	10.6	26~61	−87.5@1 MHz	-	0.027
[23]	120	45 nm CMOS	-	13.5	64	−87@1 MHz	−170.5	0.2
[24]	106.7	65 nm CMOS	−15	39.4	45	−108.2@10 MHz	−172.2	0.55**
[25]	99.1	65 nm CMOS	-	11.9	30	−93.8@1 MHz	−178.6	-
[26]	140	45 nm CMOS	−2	14.5	51	−96.5@1 MHz	−182.3	0.23
This work	140	65 nm CMOS	−8	2.4	24	−108.2@10 MHz	−177.4	0.05

$$*FoM = PN - 20 \log\left(\frac{f_{osc}}{f_{offset}}\right) + 10 \log\left(\frac{P_{diss}}{1 \text{ mW}}\right), **\text{including the pads}$$

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