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LETTER

A low power wide tuning range two stage ring VCO with frequency enhancing

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Abstract A wide tuning range frequency enhanced two stage ring voltage controlled oscillator (VCO) is proposed in this letter. The proposed delay cell increases the transmission gain by inserting a resistor between input and output, which consumes lower power to generate same oscillating frequency. A rail-to-rail effective voltage tuning range is obtained by both tuning of tail current and the strength of cross coupled latch. It is important for advanced process, which has low standard supply voltage and high threshold voltage. The proposed VCO is fabricated in TSMC 40 nm CMOS technology. The measured phase noise of proposed VCO is −98.05 dBc/Hz at 1 MHz offset with 1.38 GHz carrier frequency while consuming 1.1 mW from a 1.1 V standard supply. The figure of merit (FoM) is 160.4 dBc/Hz.
Keywords: voltage controlled oscillator, wide tuning range, low power
Classification: Integrated circuits

1. Introduction

Voltage controlled oscillator (VCO) is an essential component in modern integrated circuit, such as radio-frequency (RF) transceivers [1, 2, 3, 4, 5, 6, 7, 8] and clock data recovery (CDR) systems [9, 10, 11, 12, 13, 14, 15, 16, 17]. LC VCO has much better jitter performance but limit tuning range. LC VCO can expand the tuning range by switched inductors or capacitors [1, 9], which really consumes unacceptable area in advanced process. Thus, area efficient ring VCOs are more preferred than LC VCO in advanced CMOS process. In previous works, the N-path filter enhanced ring VCO [10] and time-interleaved ring VCO [18] have achieved excellent phase noise performance. However, for low power radio frequency transceivers, the two stage ring VCOs are the preferred choice. Because it has the lowest power consumption and smallest chip area to generate quadrature local oscillating signals. Additionally, the ring VCO usually has small linear tuning voltage range and small power to frequency efficiency compared to LC VCOs. Therefore, how to extend the linear tuning voltage range and enhance the oscillation frequency without dissipating additional power are critical design issues. In previous works, many researchers have focused on low power consumption in two stage ring VCOs [19, 20, 21, 22] and others focused on linearly or wide frequency tuning

range of ring VCOs [23, 24, 25, 26, 27, 28]. The authors of [19, 20] designed the ring VCOs with low supply voltage to reduce power dissipation. However, the oscillating frequency in these architectures is more sensitive to supply voltage and the frequency tuning range is limited by the low supply voltage. Moreover, the bulk tuning technique in [20] required special process and it would lead latch-up problem with standard supply voltage. In [23, 24, 25], multiple varactors or voltage to current converter was employed to obtain constant voltage to frequency gain. However, these methods dissipate more current with generating same frequency. In [26], the effective voltage tuning range was only 0.4 V with 1.1 V supply. It deteriorates phase noise performance and increased the loop design complexity with same frequency tuning range.

This work presents a low power dissipation and wide tuning range two stage ring VCO. A resistor is inserted between input and output in proposed delay cell, which speeds up the transition of output. Moreover, the additional resistors increase the maximum current to the load capacitance for improving the phase noise performance according to impulse sensitivity function (ISF) [29]. The frequency tuning is realized by adjusting tail current and the resistance in cross couple routes. The tuning voltage is effective in the whole supply range.

This paper is organized as follows. In Section 2, the proposed ring VCO is analyzed. Section 3 gives the simulation and measurement results. Finally, a conclusion is provided in Section 4.
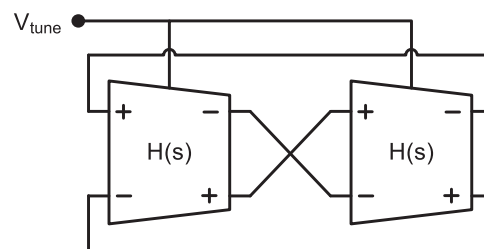

Fig. 1. Block diagram of differential two stage ring VCO

2. The proposed low power two stage ring VCO

The block diagram of a differential two stage ring VCO is shown in Fig. 1. The closed loop transfer function (TF) of two stage ring VCO can be expressed as:

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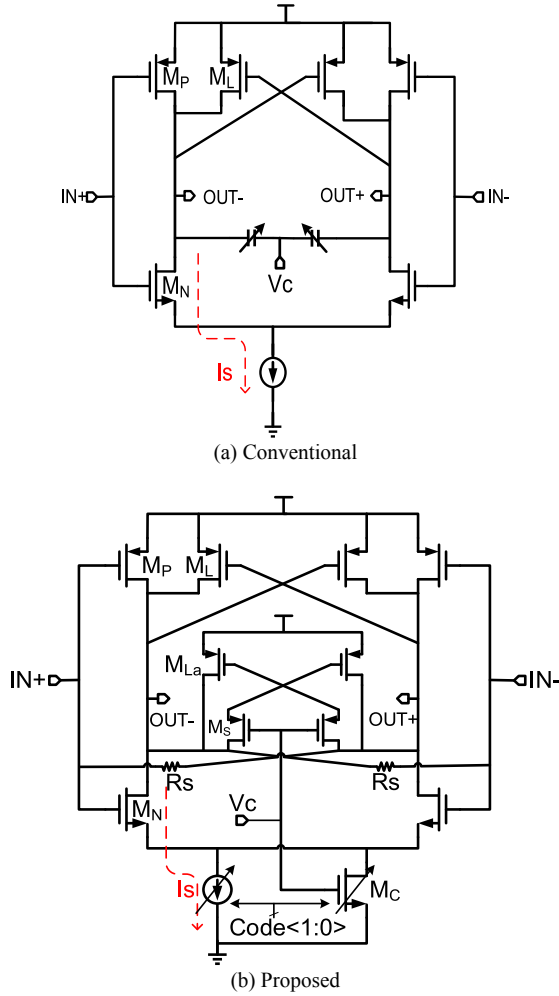(a) Conventional

(b) Proposed

Fig. 2. Schematic of delay cell in two stage ring VCO

$$H_{cl}(s) = \frac{[H(s)]^2}{1 + [H(s)]^2} \qquad (1)$$

Fig. 2(a) shows a conventional delay cell in two stage ring VCOs. The conventional delay cell is constituted of main inverter (M_N, M_P), cross coupled latch (M_L), varactors and tail current source (I_S). The transfer function of conventional delay cell is:

$$H_c(s) = \frac{G_m/C_L}{s + (G_{ds} - g_{ml})/C_L} \qquad (2)$$

where G_m is the sum of trans-conductance of M_N and M_P, which is determined by the size of transistors and the value of tail current I_S. g_{ml} is the trans-conductance of cross coupled transistor M_L. G_{ds} is the total conductance generated by channel length modulation and C_L denotes the total load capacitance at output node including varactors. Thus the oscillation frequency according to Barkhausen criteria can be expressed as follow:

$$f_{osc,c} = \frac{\sqrt{G_m^2 - (G_{ds} - g_{ml})^2}}{2\pi C_L} \qquad (3)$$

For robust oscillation start up, $G_{ds}-g_{ml}$ must be negative, which ensures the real part of complex-conjugate poles in

the closed-loop TF negative. Fig. 2(b) shows the proposed delay cells, which insert a resistor between input and output node to speed up the transition rate at output. The transfer function of proposed delay cell and the oscillation frequency of proposed two stage ring VCO can be expressed as below:

$$H_p(s) = \frac{(G_m + g_s)/C_L}{s + (G_{ds} - g_{ml} + g_s)/C_L} \qquad (4)$$

$$f_{osc,p} = \frac{\sqrt{(G_m + g_s)^2 - (G_{ds} - g_{ml} + g_s)^2}}{2\pi C_L} \qquad (5)$$

where g_s is the conductance generated by resistor R_s. Since G_{ds}-g_{ml} is negative, the first item in the root becomes larger and the second item becomes smaller after inserting resistor R_s. Additionally, the load capacitance C_L only contains parasitic capacitance. Thus, the oscillating frequency is enhanced with the same trans-conductance of main inverter and cross coupled transistors. In other words, the proposed two stage ring VCO can consume less power to generate same oscillating frequency. For the frequency tuning, a NMOS transistor paralleled with tail current source and two switch PMOS transistors connected additional cross coupled latch are controlled together for the rail to rail tuning range. When the control voltage $V_C < V_{THC}$ (the threshold voltage of M_C), the change of V_C only affects the on resistance of switch PMOS transistors M_S to tune the oscillating frequency. When $V_C > V_{DD} - V_{THS}$, the control voltage only impact on M_C. In the middle range, both branches can affect oscillating frequency. Thus, the frequency tuning can be more linear in the whole voltage range by optimally selecting the sizes of M_C and M_S. Additionally, the tail current and the size of tuning NMOS transistor Mc can be tuned with a two bits signal Code<1:0> to obtain larger tuning range.

3. Simulation and measurement results

The proposed two stage ring VCO is fabricated on TSMC 40 nm standard CMOS process. Fig. 3 shows the micrograph and layout details of proposed ring VCO. The active area of proposed two stage ring VCO without output buffer and guard ring is $0.0028\,\text{mm}^2$. The power consumption is 0.45 mW~1.1 mW with different control voltage and 2 bits tail current banks. In conventional methods, the frequency tuning usually realized by tuning the varactors or the strength of cross coupled transistors.

Nevertheless, the methods of tuning varactors add more load capacitance (C_L), which significantly decreases the oscillating frequency as shown in formula (3) and (5). Additionally, tuning the feedback strength of cross coupled transistors with inserting switch transistors avoid adding more load capacitance and have much larger tuning range. However, the tuning voltage only work when switch transistors turn on as shown in Fig. 4(a) (Tuning by M_S).

In our work, the frequency tuning combined tuning switch on resistance and tuning tail current to obtain a rail to tail effective voltage tuning range. Fig. 4(a) shows the simulated tuning curves of the three methods. Obviously, the proposed combined method can obtain a whole effec-

Table I. Performance comparison of VCOs

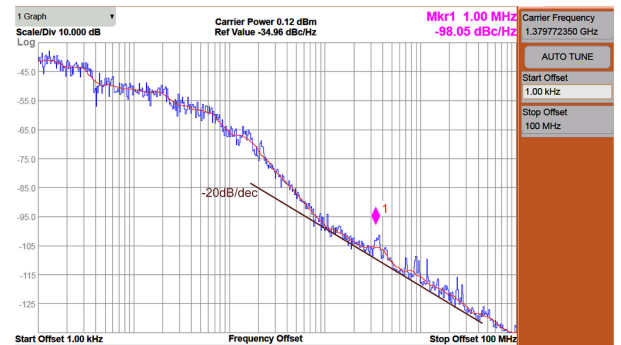| Ref.	[1]	[18]	[20]	[24]	[30]	[31]	This Work
Process (nm)	180	65	130	65	180	130	40
Supply (V)	1.8	1	0.5	1.2	1.8	1.2	1.1
Power (mW)	16.2	2.51	0.19	0.96	13.6	3.4	1.1
Frequency (GHz)	0.9/4.5	3.47	0.433	0.807	2.13	1.26	1.38
Tuning range (GHz)	0.9~4.5	1.7~3.47	0.16~2.5	0.5~0.8	1.57~2.76	1.1~1.45	0.86~1.38
Range of V_{tune} (V)	0~1.8	0.7~1	0~0.5	0~1.3	0~1.8	0.1~1.1	0~1.1
PN (dBc/Hz) @1 MHz	−133/−127	−98.7	−91.6	−88.6	−91.1	−88	−98.05
Quadrature	N	N	Y	Y	Y	Y	Y
Area (mm^2)	1.1	0.003	0.0025*	0.006	0.13	0.0028	0.0028
FoM (dBc/Hz)	180/188	161.7	151.6	146.9	149.7	145.8	160.4
FoMA (dBc/Hz)	179/187	186	178*	169	159	171	186

$\text{FoM} = 20\log(f_o/f_{offset}) - 10\log(P_{DC}/1\,\text{mW}) - \text{PN}(f_{offset})$ *The Area of VCO estimated from Microphotograph
$\text{FoMA} = 20\log(f_o/f_{offset}) - 10\log(P_{DC}/1\,\text{mW}) - \text{PN}(f_{offset}) - 10\log(\text{Area}/1\,\text{mm}^2)$
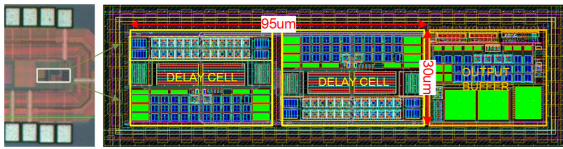
Fig. 3. Micrograph and layout of proposed two stage ring VCO

(a)

(b)
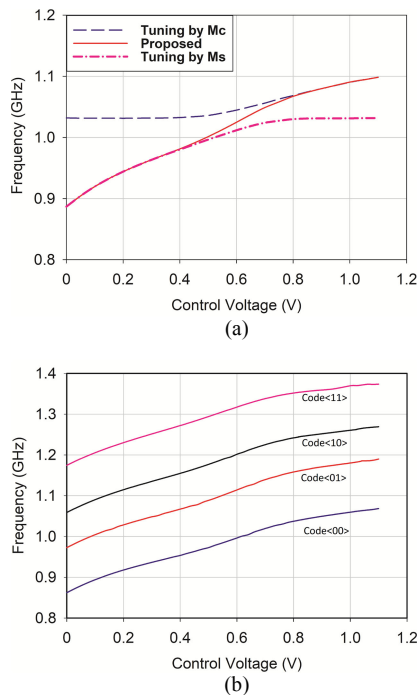
Fig. 4. (a) Simulated tuning curves of proposed method and conventional methods. (b) Measured tuning curves of proposed ring VCO swept Code<1:0>

Fig. 5. Measured phase noise of the proposed VCO at 1.38 GHz

each sub-band. The measured overall frequency-tuning range (FTR) of the proposed ring VCO is 0.86 GHz~ 1.38 GHz as shown in Fig. 4(b). Fig. 5 shows the measured phase noise of the proposed VCO at 1.38 GHz. The phase noise at 1 MHz offset is −98.05 dBc/Hz. Probably due to supply noise, a carrier instability is observed at low frequency offset (about 10 dB/decade phase noise slope below 100 KHz). And then a clear 30 dB/decade phase noise slope and 20 dB/decade phase noise slope are observed for frequency offsets between 100 KHz~2 MHz and above 2 MHz, respectively. Additionally, a short sampling time of spectrum analyser also limited the phase noise measured precision in low offset range. Table I shows the performance of our work and the comparison with previous VCOs. Obviously, the proposed ring VCO has much better FoM value than traditional quadrature ring VCOs. Although the TIRVCO in [18] achieved a little better FoM than the proposed VCO, it cannot generate quadrature signals and has limited voltage tuning range. And the proposed ring VCO obtain similar FoM with area (FoMA) with LC VCO in [1].

4. Conclusion

This letter presents a frequency enhanced two stage ring VCO, which has rail to rail effective voltage tuning range.

tive voltage tuning range, which is beneficial for phase noise performance and loop parameters design. The tail current can change from 0.4 mA~1 mA according to 2-bit control signal Code<1:0>. The size of tuning NMOS transistor Mc is also changed corresponding to the tail current to acquire approximate frequency tuning gain in

By inserting a resistor between input and output of delay cell, the oscillating frequency could be enhanced without consuming more current. The rail to rail voltage tuning range is obtained by combining tail current tuning and switch on resistance tuning. It could reduce the voltage to frequency gain for same frequency tuning range, which is beneficial for phase noise performance and phase locked loop parameters design. By employing these two techniques, the proposed two stage ring VCO obtain a fairly high FoM compared to previous differential ring VCOs.

Acknowledgments

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