

LETTER

A new snapback-free base resistance controlled thyristor with semi-superjunction

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Abstract A base resistance controlled thyristor with semi-superjunction (Semi-SJ BRT) is proposed in this paper. The highly doped P-pillar in drift region extracts injected holes into thyristor, then hole current density in thyristor will be improved and parasitic transistor is significantly suppressed. Meanwhile, highly doped drift region reduces drift resistance, then thyristor trigger current is enhanced. Snapback is greatly suppressed. In addition, much more minority carriers will be extracted due to charge coupling effect in drift region. Turn-off loss is reduced and trade-off performance is improved. Numerical simulation results show that, when the pillar doping level is higher than $1.0 \times 10^{15} \text{ cm}^{-3}$, snapback-free can be realized and turn-off loss can be reduced by 22.28%.

Keywords: semi-superjunction, BRT, snapback-free, turn-off

Classification: Power devices and circuits

1. Introduction

The MOS-gated thyristor [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13] has been widely studied in high power application due to its simplified gate drive requirement and desirable low on-state voltage drop when compared with insulated gate bipolar transistor (IGBT). Among these devices, base resistance controlled thyristor (BRT) [5, 6, 7, 8, 9, 13] attracts considerable attention because of its reduced forward voltage drop and double-diffusion process which compatible with IGBT [14, 15, 16]. However, snapback occurs during the transition from IGBT mode to thyristor mode in forward conducting state, which may results in current hogging [17] in multicell structures because of non-uniform turn-on. In [18, 19, 20, 21], self-aligned corrugated p-base is introduced into BRT, which increases resistance of P-base (R_{PB}) by lateral diffusion of boron. In this way, snapback phenomenon is effectively suppressed because latching current of thyristor is decreased which is determined by resistance R_{PB} [16].

In this paper, a new BRT structure with semi-superjunction [22, 23, 24, 25, 26, 27] in drift region (Semi-SJ BRT) is proposed. In the new structure, highly doped P-pillar in drift region will extract hole current from bottom

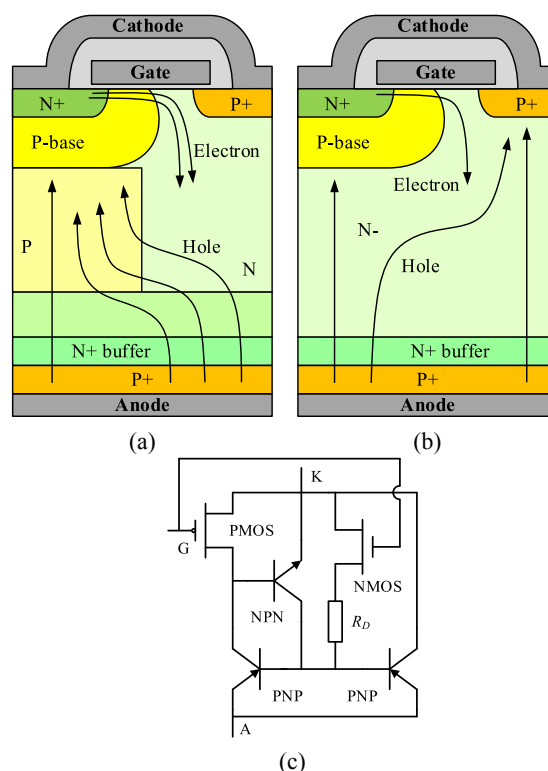


Fig. 1. Schematic cross section of (a) proposed Semi-SJ BRT and (b) conventional BRT structure. (c) Equivalent circuit of BRT device.

P+ anode into thyristor, then parasitic PNP region is greatly suppressed. Therefore, snapback is significantly suppressed. Meanwhile, turn-off loss is reduced and trade-off performance is improved.

2. Device structure and mechanism

Fig. 1 shows cross section of proposed Semi-SJ BRT and conventional BRT. Unlike conventional BRT, drift region of Semi-SJ BRT is composed by alternating P and N pillars. In BRT device, current of surface NMOS flows into N-drift region from N+ cathode, which serves as thyristor trigger current leading to strong injection of holes. The injected holes diffuse through N-drift region until collected at junction between P-base and N-drift, and then flow in P-base region to trigger latch up effect. Part of injected holes can also be directly swept into cathode by the reverse biased P+/N-drift junction of PNP transistor (i.e., P+ cathode, N-drift and P+ anode), as shown in

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Fig. 1(b). BRT therefore operates in IGBT mode at low current. As hole current increases, thyristor will be triggered to latch up, which results in a suddenly drop of resistance. Snapback phenomenon occurs in forward conducting state.

To eliminate snapback, it's very important to suppress parasitic PNP transistor [28]. In proposed BRT, highly doped P-pillar introduces a hole potential trap to extract injected holes from bottom into P-base, then the holes swept into P+ cathode will be decreased. Most of hole current flow into thyristor, only less go out through parasitic PNP transistor, as shown in Fig. 1(a). In that way, hole current density in P-base region is obviously improved and PNP transistor is greatly suppressed. Fig. 1(c) shows that drift resistance (R_D) between NMOS and anode seriously affects trigger current. Highly doped drift layer in Semi-SJ BRT greatly reduces resistance R_D , then thyristor trigger current is enhanced. The snapback therefore can be significantly suppressed.

During turn-off, minority carriers stored in drift region can be extracted into P+ cathode by surface PMOS (i.e., P-base, N-drift and P+ cathode). In the proposed BRT structure, depletion region will rapidly expand due to charge coupling effect in super junction [29, 30]. Much more minority carriers can be extracted to cathode by the horizontal electric field in alternating P and N pillars, then the switch off time is shortened. So the Semi-SJ BRT shows lower turn-off loss (E_{off}) and better trade-off performance compared with conventional BRT structure.

3. Results and discussion

Both of Semi-SJ BRT and conventional BRT with blocking voltage of 1400 V are analyzed by Sentaurus TCAD in this paper. The device parameters are listed in Table I. The forward conduction characteristics at gate voltage of 10.0 V are shown in Fig. 2. It's clearly that the undesirable snapback phenomenon occurs in output curve of conventional BRT, and snapback voltage (ΔV_{SB}) is 1.93 V. In proposed Semi-SJ BRT, snapback-free can be realized when pillar doping level is higher than $1.0 \times 10^{15} \text{ cm}^{-3}$. Consequently, the proposed structure is much more reliable than conventional device.

Table I. Device structure parameters

Parameter	Proposed	Conventional
Device active area, A	0.65 cm^2	0.65 cm^2
Pillar depth, D_{SJ}	$80.0 \mu\text{m}$	/
Pillar doping, N_{SJ}	$1.0 \times 10^{15} \text{ cm}^{-3}$	/
N-drift thickness, W_D	/	$110.0 \mu\text{m}$
N-drift doping, N_D	/	$1.0 \times 10^{13} \text{ cm}^{-3}$

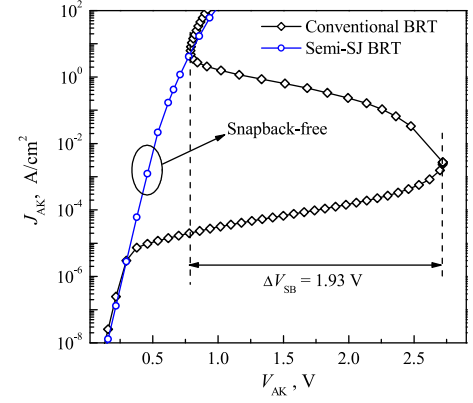


Fig. 2. Comparison of forward conduction characteristics of proposed Semi-SJ BRT and conventional BRT at the gate voltage of 10.0 V

Fig. 3 shows hole current flow lines at bottom region during forward conducting state. In the Semi-SJ BRT structure, most hole current is extracted into P-pillar, and then flow into P-base region to trigger thyristor. From Fig. 4(a) and Fig. 4(b), it can be seen that hole current density in P-base region of Semi-SJ BRT is $\sim 4.0 \times 10^{-2} \text{ A} \cdot \text{cm}^{-2}$, which is about 4 orders of magnitude higher than that of $\sim 3.0 \times 10^{-6} \text{ A} \cdot \text{cm}^{-2}$ for conventional BRT. So the hole current density in P-base is significant enhanced.

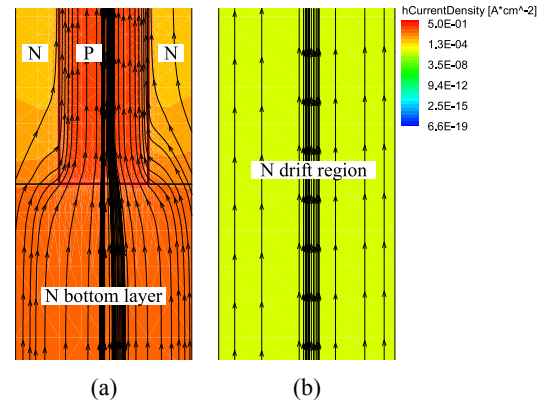


Fig. 3. Comparison of hole current flow lines: (a) Semi-SJ BRT and (b) conventional BRT

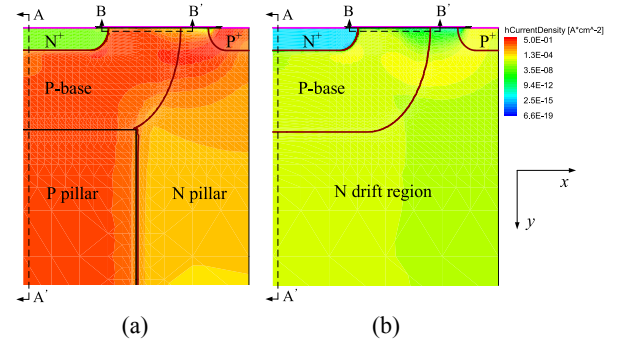


Fig. 4. The hole current distribution in P-base: (a) Semi-SJ BRT and (b) conventional BRT.

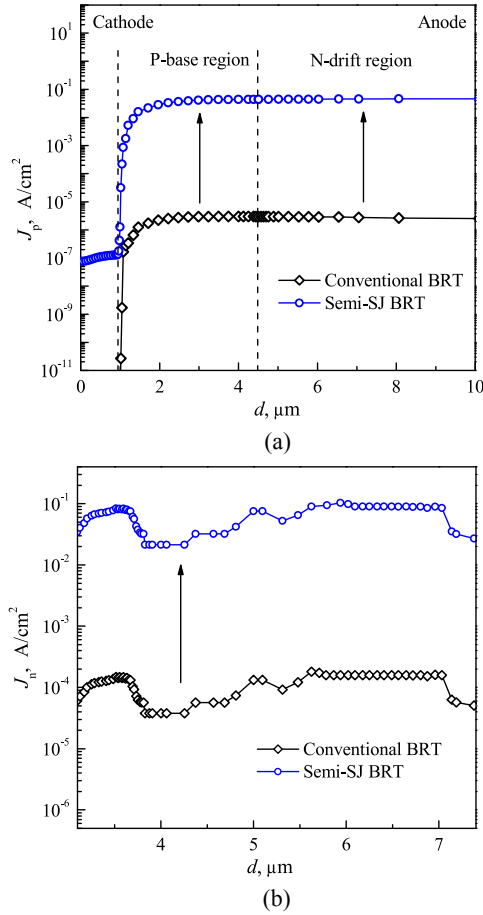


Fig. 5. (a) Hole current along line AA' and (b) NMOS trigger current along line BB'.

Fig. 5 shows hole current density along line AA' (see Fig. 4) and surface trigger current density along line BB' (see Fig. 4). Compared with conventional BRT, the hole current in thyristor of Semi-SJ BRT is improved by 4 orders of magnitude due to extraction of injected holes. As aforementioned, the highly doped drift region in proposed BRT reduces drift resistance R_D , then trigger current of thyristor is enhanced. Fig. 5(b) shows that the thyristor trigger current density of Semi-SJ BRT has been improved by 2 or 3 orders of magnitude compared with conventional BRT. Consequently, snapback can be completely eliminated.

The turn-off characteristics and trade-off curves are shown in Fig. 6(a) and Fig. 6(b), respectively. Super junction structure in Semi-SJ BRT extracts much more minority carrier because of charge coupling effect, and then turn-off energy loss (E_{off}) is reduced. In Fig. 6(a), turn-off loss of the proposed structure with pillar doping of $1.0 \times 10^{15} \text{ cm}^{-3}$ is 47.61 mJ, which is reduced by 22.28% compared with that of 61.26 mJ for conventional device at anode current of 50.0 A/cm^2 . Fig. 6(b) shows that trade-off curves of proposed Semi-SJ BRT lie below conventional BRT structure. So proposed structure has better trade-off performance than conventional device.

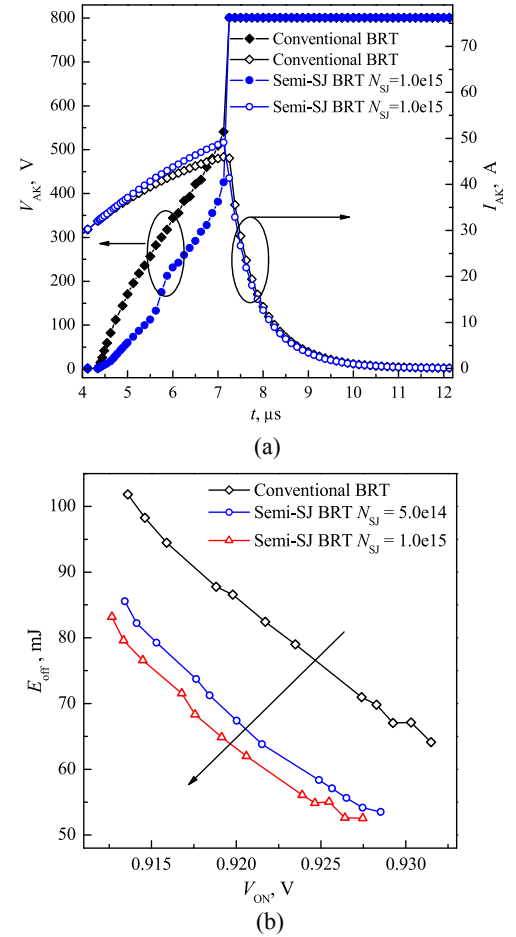


Fig. 6. (a) Turn-off characteristics with inductive load and (b) trade-off between forward voltage drop and turn-off energy loss

4. Conclusion

A new BRT structure with semi-superjunction in drift region is proposed in this paper. Highly doped P-pillar in thyristor region produces a hole potential trap to extract injected holes from bottom P+ anode into thyristor. And then, hole current density in P-base is dramatically improved, and parasitic PNP transistor is significantly suppressed. Meanwhile, highly doped drift layer reduces resistance, then thyristor trigger current is enhanced. Simulation results show that, for the proposed structure, snapback-free can be realized when the pillar doping is higher than $1.0 \times 10^{15} \text{ cm}^{-3}$. Much more minority carriers will be extracted into P-base region because of charge coupling effect in the alternation P and N pillars, then lower turn off loss and better trade-off performance can be realized compared with conventional BRT structure.

Acknowledgments

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References

- [1] B. J. Baliga: "Enhancement and depletion mode vertical channel MOS-gated thyristors," *Electron. Lett.* **15** (1979) 645 (DOI: 10.1049/el:19790459).
- [2] V. A. K. Temple: "MOS controlled thyristors (MCT's)," *IEDM* (1984) 282 (DOI: 10.1109/IEDM.1984.190702).
- [3] V. A. K. Temple: "MOS-controlled thyristors-A new class of power devices," *IEEE Trans. Electron Devices* **33** (1986) 1609 (DOI: 10.1109/T-ED.1986.22714).
- [4] M. Stoisiek and H. Strack: "MOS GTO-A turn off thyristor with MOS-controlled emitter shorts," *IEDM* (1985) 158 (DOI: 10.1109/IEDM.1985.190918).
- [5] M. Nandakumar, *et al.*: "A new MOS-gated power thyristor structure with turn-off achieved by controlling the base resistance," *IEEE Electron Device Lett.* **12** (1991) 227 (DOI: 10.1109/55.79565).
- [6] M. Nandakumar, *et al.*: "The base resistance controlled thyristor (BRT)-A new MOS gated power thyristor," *ISPSD* (1991) 138 (DOI: 10.1109/ISPSD.1991.146084).
- [7] M. Nandakumar, *et al.*: "Theoretical and experimental characteristics of the base resistance controlled thyristor (BRT)," *IEEE Trans. Electron Devices* **39** (1992) 1938 (DOI: 10.1109/16.144687).
- [8] B. J. Baliga: U.S. Patent 5099300 (1992).
- [9] B. J. Baliga: U.S. Patent 5198687 (1993).
- [10] D. N. Pattanayak and B. J. Baliga: U.S. Patent 4847671 (1989).
- [11] B. J. Baliga: "The MOS-gated emitter switched thyristor," *IEEE Electron Device Lett.* **11** (1990) 75 (DOI: 10.1109/55.46933).
- [12] M. S. Shekar, *et al.*: "Characteristics of the emitter switched thyristor," *IEEE Trans. Electron Devices* **38** (1991) 1619 (DOI: 10.1109/16.85158).
- [13] M. Nandakumar, *et al.*: "Fast switching power MOS-gated (EST and BRT) thyristors," *ISPSD* (1992) 256 (DOI: 10.1109/ISPSD.1992.991282).
- [14] B. J. Baliga: "Trends in power semiconductor devices," *IEEE Trans. Electron Devices* **43** (1996) 1717 (DOI: 10.1109/16.536818).
- [15] B. J. Baliga: *Fundamentals of Power Semiconductor Devices* (Springer, New York, 2008) 625–736.
- [16] B. J. Baliga: *Advanced High Voltage Power Device Concepts* (Springer, New York, 2011) 437–483.
- [17] V. Parthasarathy and T. P. Chow: "Theoretical and experimental investigation of 500 V p- and n-channel VDMOS-LIGBT transistors," *ISPSD* (1995) 241 (DOI: 10.1109/ISPSD.1995.515042).
- [18] D. S. Byeon, *et al.*: "CB-BRT: A new base resistance-controlled thyristor employing a self-aligned corrugated p-base," *IEEE Electron Device Lett.* **19** (1998) 493 (DOI: 10.1109/55.735757).
- [19] D. S. Byeon, *et al.*: "A base resistance controlled thyristor with the self-align corrugated p-base," *ISPSD* (1998) 209 (DOI: 10.1109/ISPSD.1998.702670).
- [20] D. S. Byeon, *et al.*: "The maximum controllable current of improved base resistance controlled thyristor employing a self-aligned corrugated p-base," *ISPSD* (1999) 229 (DOI: 10.1109/ISPSD.1999.764105).
- [21] O. Jae-Keun, *et al.*: "A new base resistance controlled thyristor employing trench gate and self-align corrugated p-base," *ISPSD* (2001) 207 (DOI: 10.1109/ISPSD.2001.934591).
- [22] W. Saito, *et al.*: "600 V semi-superjunction MOSFET," *ISPSD* (2003) 45 (DOI: 10.1109/ISPSD.2003.1225227).
- [23] W. Saito, *et al.*: "Semisuperjunction MOSFETs: New design concept for lower on-resistance and softer reverse-recovery body diode," *IEEE Trans. Electron Devices* **50** (2003) 1801 (DOI: 10.1109/TED.2003.815126).
- [24] W. Saito, *et al.*: "High breakdown voltage (>1000 V) semi-superjunction MOSFETs using 600-V class superjunction MOSFET process," *IEEE Trans. Electron Devices* **52** (2005) 2317 (DOI: 10.1109/TED.2005.856804).
- [25] W. Saito, *et al.*: "Over 1000 V semi-superjunction MOSFET with ultra-low on-resistance below the Si-limit," *ISPSD* (2005) 27 (DOI: 10.1109/ISPSD.2005.1487942).
- [26] S. Ono: "Design concept of n-buffer layer (n-bottom assist layer) for 600 V-class semi-super junction MOSFET," *ISPSD* (2007) 25 (DOI: 10.1109/ISPSD.2007.4294923).
- [27] H. Huang and X. Chen: "Optimization of specific on-resistance of semisuperjunction trench MOSFETs with charge balance," *IEEE Trans. Electron Devices* **60** (2013) 1195 (DOI: 10.1109/TED.2013.2242331).
- [28] F. Hu, *et al.*: "A base resistance controlled thyristor with N-type buried layer to suppress the snapback phenomenon," *ICSICT* (2018) 1 (DOI: 10.1109/ICSICT.2018.8565735).
- [29] M. Antoniou, *et al.*: "The 3.3 kV semi-superjunction IGBT for increased cosmic ray induced breakdown immunity," *ISPSD* (2009) 168 (DOI: 10.1109/ISPSD.2009.5158028).
- [30] M. Antoniou, *et al.*: "The semi-superjunction IGBT," *IEEE Electron Device Lett.* **31** (2010) 591 (DOI: 10.1109/LED.2010.2046132).