

Light-load efficiency improving boost converter with the hybrid modulation of hysteresis current mode and burst mode

Runyun Miao¹, Changchun Chai¹, Yuqian Liu^{1a)}, Hui Li¹, and Yintang Yang¹

Abstract This paper proposes a new method to improve the efficiency of boost converter under light load conditions by using the hybrid modulation of hysteresis current mode and burst mode (HCM-BM). A circuit is designed to satisfy the requirement of adaptive fast switching between HCM and BM. The whole circuit of proposed HCM-BM converter and conventional HCM converter have been built with a standard 0.18- μ m CMOS process, respectively. The simulation results show that the proposed converter provides a maximum efficiency improvement of 17% under light load compared with the conventional boost converter. Meantime, it can achieve up to 74% efficiency at 10 μ A load.

Keywords: light-load efficiency, boost converter, HCM-BM Classification: Integrated circuits

1. Introduction

Light-load efficiency is a major concern in applications where the digital load ICs spend the majority of their time in idle mode. Many techniques have been proposed to improve efficiency under light load conditions. The gate modulation technique was previously reported to dynamically scale the gate voltage swing with the load for reducing the gate-drive loss [1, 2, 3]. Scaling the size of power transistors with the load was applied to lower both the converter's gate-drive loss and switching loss [4, 5, 6, 7]. However, if the gate drive of the segmented transistor is not properly designed, there may be significant power loss of cross conductive short circuit in reference [4]. To address this given issue, cross-conduction-free width switching (CCF-WS) technique was developed to eliminate the short-circuit power loss associated with switching different segments of on-chip power transistors [8, 9, 10, 11]. These techniques related to power transistors improve the lightload efficiency without reducing the converter's operation frequency. Some variable frequency techniques are also available. A number of studies have focused on designing more accurate current detection modules to eliminate the reverse current of high-side switch in the energy release period [12, 13, 14, 15]. A frequency hopping technique applied to adaptive on-time (AOT) boost converter was reported to lessen the frequency in proportion according to the load change under light load conditions [16, 17, 18].

DOI: 10.1587/elex.16.20190108 Received February 26, 2019 Accepted April 3, 2019 Publicized April 24, 2019 Copyedited June 10, 2019 Besides, a technique can achieve high-efficiency at light load depending on its characteristic of the load-dependent switching frequencies [19, 20, 21]. Burst-Mode (BM) technique can change the operation frequency by periodically charging the output capacitor with burst of pulses [22, 23, 24, 25]. Although the above techniques reduce the power consumption to some extent, they ignore the influence of the quiescent current through the control circuits on the efficiency. In general, the quiescent current is negligible when the converter operates under high load conditions. However, many devices are usually under ultra-light load or standby conditions for a long time, the resulting power leak adds up to an enormous waste. Hence, HCM-BM control technique is proposed in this paper to reduce both switching frequency of power transistors and the average of quiescent current, thus it improves the light-load efficiency. Meantime, an innovative adaptive switching circuit is designed to achieve fast adaptive switching between HCM and BM.

The remainder of this paper is organized as follows. Section 2 describes the analysis of power consumption with BM. Section 3 describes the operation principle of HCM-BM control and the adaptive switching circuit. Section 4 presents the comparison of simulation results between proposed converter and conventional converter. And section 5 provides the conclusion.

2. Power consumption analysis

The synchronous boost converter has three types of power loss: conduction loss, switching loss and quiescent power dissipation. The conduction loss is generated by the current flowing through some resistances such as the direct current resistance (DCR) of inductor, conduction resistances of two power transistors and the equivalent series resistance (ESR) of output capacitor. The switching loss is mostly caused by the charge-discharge process of the parasitic capacitance and the voltage-current (V-I) overlap in two power transistors during the transitions from ON to OFF (or from OFF to ON). The quiescent power dissipation is mainly due to the quiescent current through the control circuits.

The equivalent circuit model of synchronous boost converter for analysis of power loss is shown in Fig. 1, where R_L is the DCR of inductor *L*. R_n and R_p are the conduction resistances of M_N transistor (low-side transistor) and M_P transistor (high-side transistor), respectively. R_C is the ESR of output capacitor *C*. C_{gsn} , C_{gdn} and C_{dsn} are the gate-source, gate-drain and drain-source parasitic capacitance of M_N , respectively. C_{gsp} , C_{gdp} and C_{dsp} are the

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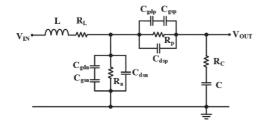


Fig. 1. The equivalent circuit model of synchronous boost converter for analysis of power loss.

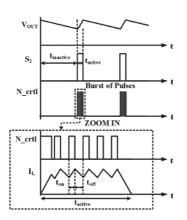


Fig. 2. The key waveforms of converter operating in BM.

gate-source, gate-drain and drain-source parasitic capacitance of M_P , respectively.

In BM, the power transistors of boost converter are cyclically switched ON and OFF during an active period while they are kept OFF-state during an inactive period. The burst of pulses energy can be transferred to output port within several switching cycles during active period while no energy is supplied to output port during inactive period. The key waveforms of BM are illustrated in Fig. 2 [26, 27]. The positive pulse of the switching signal S_2 represents that the related control circuits are enabled in active period. The signal *N_crtl* represents the drive pulse of the low-side transistor. The lower the load current, the longer the inactive period, hence, the lower the BM frequency. The power consumption in BM are analyzed. The power consumption in active period can be expressed as Eq. (1).

 $P_{active} = R_{eq,a}I_L^2 + f_s[C_{eq,a}V_{OUT}^2 + V_{OUT}I_Lt_{overlap}] + V_{OUT}I_{Q,a}$ (1) the power consumption in inactive period is modified as Eq. (2),

$$P_{inactive} = P_{conduct,i} + P_{static,i} = R_C I_{load}^2 + V_{OUT} I_{Q,i}$$
(2)

the average value of power loss over the whole period is given by Eq. (3),

$$P_{loss} = \frac{P_{active}t_{active} + P_{inactive}t_{inactive}}{t_{active} + t_{inactive}}$$
(3)

where f_s , $t_{overlap}$, I_L and $I_{Q,a}$ are the burst of pulses frequency, V-I overlapping time, the current through the inductor and the quiescent current through the control circuits when the boost converter operates in active period, respectively. $I_{Q,i}$ is the quiescent current through the control circuits when the boost converter operates in inactive period.

od. And $R_{eq,a}$ and $C_{eq,a}$ given by Eq. (4) and Eq. (5) are the equivalent resistance and the equivalent capacitance, respectively.

$$R_{eq,a} = R_L + R_n D + R_p (1 - D) + R_C D (1 - D)$$
(4)

$$C_{eq,a} = C_{gsn} + C_{dsn} + C_{gdn} + C_{gsp} + C_{gdp} + C_{dsp}$$
(5)

Where D is the duty ratio of burst of pulses.

3. Operating principle of proposed boost converter

The proportion of quiescent power dissipation and frequency-dependent consumption to total power consumption increases with the load current decreasing. Therefore, the light-load efficiency of boost converter can be improved effectively by lessening the quiescent current and reducing the switching frequency of converter. A method where the control circuits are open and close intermittently at light load is adopted, resulting in the decrease of the average quiescent current over every operation period. However, this method damages the performance of heavy-load due to the large output voltage ripple. Hence, a reasonable strategy for integrating HCM and BM simultaneously is taken with giving consideration of applications under a wide load. HCM can reduce the impact of output voltage ripple under heavy load by making the boost converter operate in CCM. [28, 29] In addition, both HCM and BM can realize automatic frequency adjustment under light load conditions. The block diagram of proposed HCM-BM control boost converter is illustrated in Fig. 3. The adaptive switching circuit is responsible for the fast adaptive switching between HCM and BM.

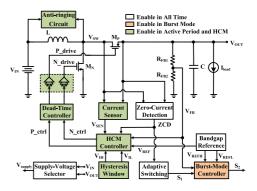


Fig. 3. The block diagram of proposed HCM-BM control boost converter.

The Burst-Mode controller consists of two low power comparators and a flip-flop. When the feedback voltage V_{FB} is lower than the pre-defined reference voltage V_{REFL} , the switching signal S_2 is set a high level, enabling the circuits in these green boxes. Otherwise, when the feedback voltage V_{FB} is higher than another pre-defined reference voltage V_{REFH} , the switching signal S_2 is set a low level, disabling the above circuits. BM period consists of active period and inactive period. In active period, the operation mode of the converter is CCM of HCM modulation in which the output voltage is in the rising state. In inactive period, the converter whose power transistors are turned off enters sleep mode and the output voltage is in a state of decline. Hence, the BM controller is essentially a switch on HCM.

The key waveforms of BM are shown in Fig. 4. The active period consisting of several HCM periods is the process of energy storage in output capacitor. In this process, the sampling signal of current through the inductor V_{SEN} is forced into the hysteresis window. In addition, the rising of feedback voltage V_{REF} results in the hysteresis window a slight decline. The inactive period is the process of energy release from output capacitor. As the variation of the voltage across output capacitor is constant during inactive period, the released energy is constant with different load current. The stored energy in active period provides not only the energy released in inactive period, but also the energy required for the load in active period. The output capacitor has the same energy at the beginning and end of each BM period. Therefore, the converter requires more time or more HCM periods for energy storage in active period with the load current increasing.

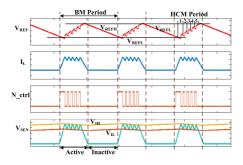


Fig. 4. The key waveforms of BM.

The zero current detection circuit schematic is shown in Fig. 5. The time for the signal ZCD kept at a low level in active period increases with the load current increasing. However, ZCD is kept at a high level in inactive period. This variation of ZCD can be used to capture the transition point from light load to heavy load. The converter can change from BM to HCM depending on this variation.

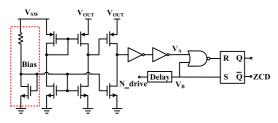


Fig. 5. The zero current detection circuit schematic.

The time for the signal *ZCD* kept at a high level in DCM of HCM modulation increases with the load current decreasing. This variation of *ZCD* can be used to capture the transition point from heavy load to light load. The converter can change from HCM to BM depending on this variation. The light load threshold of the converter can be obtained by deducing the variation of ZCD by formulas. The time when the low-side transistor is turned on and the high-side transistor is turned off is expressed by t_{on} .

The time when the low-side transistor is turned off and the high-side transistor is turned on is expressed by t_{off} . These two variables in DCM of HCM modulation are given by Eq. (6).

$$t_{on} = \frac{H}{MLV_{IN}} \quad t_{off} = \frac{H}{ML(V_{OUT} - V_{IN})} \tag{6}$$

where *H* is the hysteresis window voltage V_{IH} - V_{IL} , *M* is the sampling coefficient of current through the inductor. The time when the two power transistors are turned off is expressed by t_{DCM} . Eq. (7) can be obtained according to the law of conservation of energy.

$$\int_{0}^{t_{on}+t_{off}} V_{IN}i_{L}(t)dt = V_{OUT}I_{load}^{2}(t_{on} + t_{off} + t_{DCM})$$

$$+ \int_{0}^{t_{on}+t_{off}} R_{L}i_{L}^{2}(t)dt + \int_{0}^{t_{on}} R_{n}i_{L}^{2}(t)dt + \int_{t_{on}}^{t_{on}+t_{off}} R_{p}i_{L}^{2}(t)dt$$

$$+ \int_{t_{on}}^{t_{on}+t_{off}} R_{C}[i_{L}(t) - I_{load}]^{2} dt + R_{C}I_{laod}^{2}(t_{on} + t_{DCM})$$
(7)

hence, the time when the two power transistors are turned off can be obtained by Eq. (8).

$$t_{DCM} = \alpha t_{on} + \beta t_{off} = \frac{\alpha H}{MLV_{IN}} + \frac{\beta H}{ML(V_{OUT} - V_{IN})}$$
(8)

where α and β are given by Eq. (9) and Eq. (10), respectively.

$$\alpha = \frac{2M}{V_{IN}H} (V_{OUT}I_{load}^2 + R_C I_{laod}^2) + \frac{2(R_L + R_n)H}{3V_{IN}M} - 1 \quad (9)$$

$$\beta = \alpha + \frac{2R_pH}{3V_{IN}M} - \frac{2R_CI_{load}}{V_{IN}}$$
(10)

The adaptive switching circuit schematic is shown in Fig. 6. A simple charge and discharge technique is adopted in the circuit. When the time for the signal ZCD kept at a low level is long enough, the voltage across the capacitor C_{ch1} is greater than the threshold voltage of M_{6A} . So the switching signal S_1 is set at a low level and the converter is triggered to BM from HCM. When the time for the signal ZCD kept at a high level is long enough, the voltage across the capacitor C_{ch2} is greater than the threshold voltage of M_{6B} . So the switching signal S_1 is set at a high level and the converter is triggered to HCM from BM.

Hence, the value of t_{ZCD} in the transition point when the converter is changed from BM to HCM can be obtained by Eq. (11). Where V_{th1} is the threshold voltage of M_{6A} .

$$t_{ZCDTH1} = \frac{nV_{th1}C_{ch1}}{I_{1A}}$$
(11)

The value of t_{ZCD} in the transition point when the converter is changed from HCM to BM can be obtained by Eq. (12). Where V_{th2} is the threshold voltage of M_{6B} .

$$t_{ZCDTH2} = \frac{nV_{th2}C_{ch2}}{I_{1B}}$$
(12)

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According to Eq. (8), once the light load threshold of the converter is determined, the value of t_{ZCDTH2} can be adjusted by changing the hysteresis window voltage and the sampling coefficient of current through the inductor. Then the capacitor C_{ch2} and the current source I_{1B} are adjusted to satisfy Eq. (12). However, the value of t_{ZCDTH1} with different light load threshold is hard to be determined by formulas. The value of t_{ZCDTH1} with different light load threshold can be obtained by simulation. Then the capacitor C_{ch1} and the current source I_{1A} are adjusted to satisfy Eq. (11).

So there exists two kinds of light load threshold. One is related to the transition point when the converter is changed from HCM to BM, another is related to the transition point when the converter is changed from BM to HCM. One light load threshold is allowed to be unequal to another. But the two kinds of light load threshold can't be too far apart.

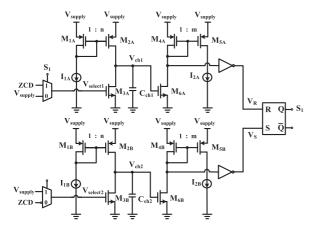


Fig. 6. The adaptive switching circuit schematic.

4. Simulation results

The whole circuits of proposed HCM-BM converter and conventional HCM converter have been built, respectively. The power stage of the two converters are identical. The value of inductor is $4.7 \,\mu\text{H}$ and its DCR is $15 \,\text{m}\Omega$. The value of output capacitor is $15 \,\mu\text{F}$ and its ESR is $10 \,\text{m}\Omega$. All parameters of two power transistors are identical. The rated output voltage is $5 \,\text{V}$ with full load from $10 \,\mu\text{A}$ to $400 \,\text{m}$ A. The sampling coefficient of the output voltage is 0.24, so the reference voltage V_{REF} and V_{FBH} is set as $1.2 \,\text{V}$. The other reference voltage V_{FBL} depends on the ripple of output voltage is set as $40 \,\text{mV}$, then V_{FBL} is set as $1.1904 \,\text{V}$.

The hopping of load between 30 mA and 60 mA with 3 V input voltage is simulated for different architectures. Simulation waveforms of proposed converter are shown in Fig. 7(a), which reveals the adaptive switching process of BM and HCM. Similarly, simulation waveforms of conventional converter are also given by Fig. 7(b), which describes the transition process of CCM and DCM. The simulation results show that the switching timing of the converter between different modes is consistent with the previous principle analysis. When the load is between 30 mA and 60 mA, the converter may switch between two modes many

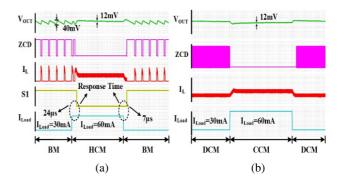


Fig. 7. Simulation waveforms of (a) proposed converter, (b) conventional converter with the hopping of load between 30 mA and 60 mA.

times due to the limitations of the adaptive switching circuit. However, it does not hinder the power consumption improvement. The ripple of output voltage in HCM is smaller than that in BM for proposed architecture. For example, the output voltage ripple is 40 mV in BM, but 12 mV in HCM. Generally, the time in active period is shorter than that in inactive period. Moreover, the inactive time is hundreds or even thousands of times the active time with the load decreasing to several microamperes, which causes the average quiescent current to drop rapidly. Compared with conventional converter, the proposed converter has identical operation mechanism in heavy load, but larger ripple of output voltage and smaller average quiescent current in light load. The transient response time is 24 us when the proposed converter changes from BM to HCM, but 7 us when it changes from HCM to BM.

Fig. 8 shows the efficiency comparison with identical input voltage (3 V) and different ripple voltage. The efficiency in heavy load has little difference for the proposed HCM-BM converter and conventional HCM converter. In BM, the output voltage ripple V_{ripple} which is pre-defined by the BM controller is equal to V_{REFH} - V_{REFL} . If the V_{ripple} is defined bigger, the proposed converter has improved efficiency greatly under light load conditions compared with the conventional converter. In addition, the proposed converter provides a maximum efficiency improvement of 17% under light load and achieve up to 74% efficiency at 10 μ A load. The comparison results between the other designs and this work is listed in Table I. The results demonstrate that the proposed converter has a high efficiency under ultra-light load conditions.

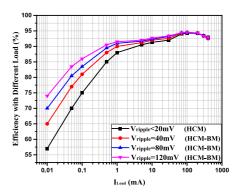


Fig. 8. Efficiency simulation with different output voltage ripple.

[30]	[4]	[29]	This work
CSC	CCF-WF	HCM	HCM-BM
0.3-µm	0.35-µm	0.18-µm	0.18-µm
Measurement	Measurement	Simulation	Simulation
2.5–4.2 V	>1.2 V	1.5–2.7 V	1.5-4.2 V
5.0 V	2.0 V	3.3 V	5.0 V
<50 mV	N/A	<30 mV	0–120 mV
1 µH	4.7 μΗ	2.35–7 μH	$4.7\mu\mathrm{H}/15\mathrm{m}\Omega$
10 µF	N/A	10–40 µF	$15\mu F/10m\Omega$
10-400 mA	20-200 mA	25-300 mA	10 µ-400 mA
78–90%	78–90.1%	85–96%	74–94.6%
	CSC 0.3-μm Measurement 2.5-4.2 V 5.0 V <50 mV 1 μH 10 μF 10-400 mA	CSC CCF-WF 0.3-µm 0.35-µm Measurement Measurement 2.5-4.2 V >1.2 V 5.0 V 2.0 V <50 mV	CSC CCF-WF HCM 0.3-μm 0.35-μm 0.18-μm Measurement Measurement Simulation 2.5-4.2 V >1.2 V 1.5-2.7 V 5.0 V 2.0 V 3.3 V <50 mV

Table I. Summary and comparison

5. Conclusion

This paper proposes a new method to improve the efficiency of boost converter under light load conditions by using the hybrid modulation of hysteresis current mode and burst mode (HCM-BM). Meantime, a circuit applied to adaptive switching between BM and HCM is designed. The proposed boost converter has a fast transient response of switching between different modes. The whole circuit of proposed converter and conventional converter are built, respectively. The simulation results verify that the proposed method can significantly improve the conversion efficiency of boost converter under light load conditions.

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