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LETTER

Novel method to optimize the column random telegraph signal performance in CMOS image sensor

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Abstract We present a methodology to define and distinguish the column random telegraph noise (RTS) derived from column bitline bias and comparator input transistors only based on the digital output data of each pixel. Many test experiments were conducted on the CMOS image sensor (CIS) chips fabricated with Dongbu 0.13 um, 1P5M process technology. According to the experiments, the threshold voltage and the channel length of the transistors have a significant influence on the intensity of the column RTS. Large channel length and proper threshold voltage, 0.15 V to 0.3 V for most cases, mean a low level of column RTS.

Keywords: column RTS, channel length, threshold voltage
Classification: Integrated circuits

1. Introduction

Complementary metal oxide semiconductor (CMOS) image sensor (CIS) is now extensively used in mobile phone, driver recorder and security camera due to its low process cost, low power cost, and high frame read-out speed compared with charge coupled device (CCD). Nevertheless, the CIS suffers from the more noise problems under many conditions, which restrict a wide application of CIS. As the size of the MOS transistor decreases with advanced process technology, the frequency flick noise, one type of the noise in CIS, would degenerate into random telegraph signal (RTS) noise which is difficult to be described into an ordinary function with parameters like time and voltage due to its uncertainty and unpredictability.

Many researches has been conducted to explain the reason and source of the RTS noise [1, 2]. The basic electron trapped and detrapped process is illustrated [3, 4, 5], and new source and location of RTS noise are presented [6, 7, 8, 9, 10, 11, 12]. The new analysis methods of RTS [13, 14, 15, 16, 17], and improvement methods of RTS [18, 19, 20, 21, 22], are also introduced. Moreover, not only the impact on CIS [23, 24, 25, 26], the effect of RTS existed in flash memories [27, 28] and resistive switching memories [29, 30] are also under research.

Although the theory of the RTS has been analyzed deeply, there are still a lack of consideration and measurement on the column readout circuit in the CIS. Besides the source follower transistors in the CIS pixel structure, which has been paid much attention to by many researchers, the transistors located at the end of each column of pixel array, including bitline bias transistors and input transistors of comparators which are shown in Fig. 1, also make a significant contribution to the noise level. Moreover, due to the special location, these transistors can influence all pixels in the same column, leading to a high noise level which would be observed finally as obvious column strip in the display image and is difficult to eliminate by image processing due to the random property. So it is necessary to detect and decrease the column RTS noise for the purpose of improving the image quality. Moreover, the RTS noise is confused with other noise such as thermal noise and fixed pattern noise, which leads to the difficulty to extract and analyze RTS noise behavior in the real sensor tests with the only acquirable output as digital brightness of each pixel in every frame after sensor chip package.

Aimed at these problems above, this paper illustrates some contributions shown as follow.

1) We present a method to define and detect the column RTS noise. The method, which is only based on the output data from the digital platform, can be used to precisely distinguish the column RTS noise from other noise such as thermal noise and fixed pattern noise.

2) Based on the different circuit connection between bitline bias transistor and comparator input transistor, we present a simple and convenient method using four channels output comparison to confirm the column RTS noise source.

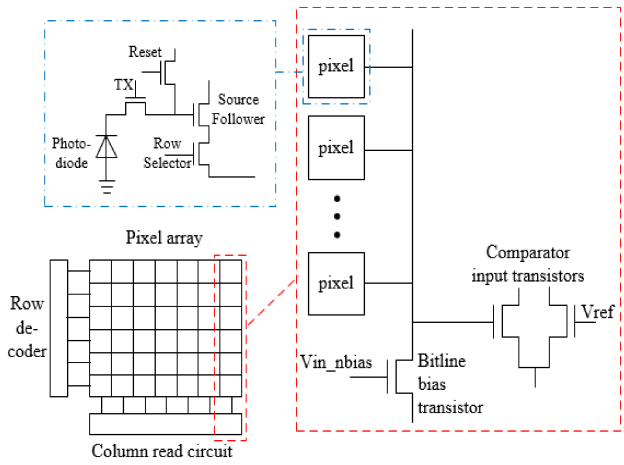

Fig. 1. Sketch of pixel and column bitline bias transistors and comparator input transistors.

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3) With the help of the method, we conduct many experiments and analyze the influence factor about RTS noise in the column transistors, analyze the reason to the experiment results, and present an optimization direction that the large gate length and proper threshold voltage of transistor could decrease column RTS noise.

2. Methodology

For the purpose of extracting the column RTS noise from the digital output of each pixel in real time, and distinguishing the RTS from other noise, a new output signal process method is proposed as follow. It is necessary to realize that the only output that can be acquired and measured from the actual sensor chip is the output data in digital display as pixel brightness in each frame. Moreover, the column RTS noise from bitline transistor and comparator input transistors need to be distinguished, which is also a challenge. A simple and simplified method to accurately extract and quantize column RTS noise intensity and determine the noise source location is proposed based on the RTS noise characteristic and readout circuit structure. All the calculation and experiments are based on the finite but effective digital display output data, and our method can be easily used to rapidly check and estimate the column RTS noise level of CIS sensor chips in large amount. The specific principle and methodology are introduced as follow.

2.1 Common theory of digital output

The relationship between the digital display brightness and voltage difference in column circuit can be described by the equations shown below.

$$V_o = V_{rst} - V_{sig} \tag{1}$$

$$V'_o = V_o + V_{col\ RTS} \tag{2}$$

$$DN = \frac{V_o \cdot Gain}{V_{step}} \cdot 255 \tag{3}$$

Among these equations, V_{rst} and V_{sig} are the column voltage in reset and readout stage respectively, $V_{col\ RTS}$ is the error voltage caused by column RTS, then V'_o means the output voltage difference including column RTS, DN is the digital number output, and $Gain$ is the analog and digital gain applied on the V_o in the readout module. V_{step} is the step voltage corresponding to one unit of digital number.

Considering that light intensity has no attribution to the column RTS noise, the experiment can be conducted at completely dark scene without any photons injection. What need to be paid more attention to is that the column RTS noise is not the only noise could affect V_o. The real V_o also include some other noise, such as fixed pattern noise and random thermal noise, which cause the difficulty to distinguish the column RTS noise.

2.2 Column RTS detection methodology

Observing the characteristic of column RTS noise which is random and influence the whole column, we design a method including such steps.

Step1: calculate the standard deviation of each pixel output, just as the equation (4).

By summarizing the output of each pixel in at least 28 frames and average the summary, the fixed pattern noise is concluded only in the average brightness $\bar{p}$, but not the standard deviation Δ_p. In other words, the process getting the standard deviation excludes the fixed pattern noise and preserves the random noise including column RTS noise.

Step2: calculate the average random noise of the whole column as the random noise level of a unique column, as equation (5) works

Considering one column contain more than five hundreds pixels, the sum of random noise among all pixels in every column stay in the very similar value, and the noise difference among the columns is derived from the discrepancy of the column RTS noise.

Step3: calculate the difference between each Δ_C of the column and average Δ_C value of all columns, as equation (6) shows.

We can acquire the information from the difference Δ, which reveals the level of column RTS noise.

$$\Delta_p = \frac{1}{27}\sqrt{\sum_{k=1}^{n}(p_k - \bar{p})^2} \tag{4}$$

$$\Delta_C = \frac{1}{R}\sum \Delta_p \tag{5}$$

$$\Delta = \left|\Delta_C - \frac{1}{C}\sum \Delta_C\right| \tag{6}$$

2.3 Noise source distinction

Here we developed a method to confirm the column RTS noise source based on the different connection between the bitline and comparator. The image sensor we used to test adopts the common RGGB pattern to sense and reproduce the color information, and in order to keep the uniformity of G-channel, the comparator transistor connect in a X-cross way, which means one comparator is either connecting the 2 G-channel column or connecting R and B channel in two columns, while the bitline transistor just connects the pixels in the same physical structure column. Based on this difference we can distinguish the noise source by calculating the column RTS in different channel, meaning one column has two Δ, ΔB and ΔG, or ΔG and ΔR. As the Fig. 2 shows, if two columns nearby sharing the same pattern have large ΔB and ΔR, or large ΔG and ΔG separately, then the large column RTS noise is caused by comparators, and if for two columns nearby only one column has two large Δ, then it is the bitline transistors that cause bad effect.

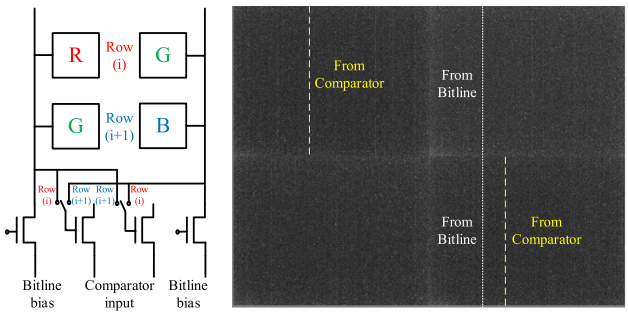


Fig. 2. The difference circuit connection and column RTS behaviour between bitline and comparator source

3. Experimental results

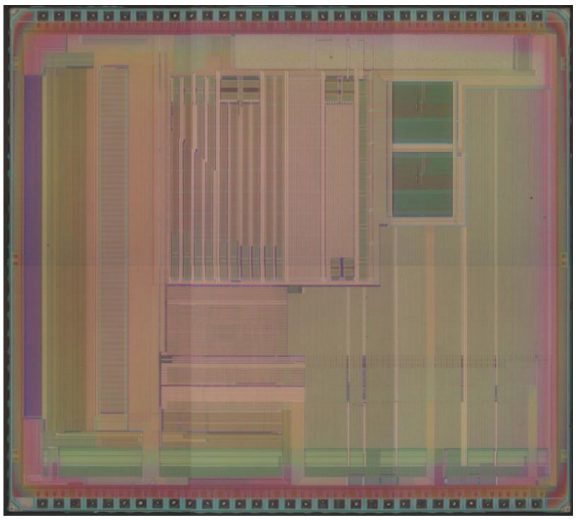
To make the test result consistent with the observation result, we need to establish a criterion for our methodology in order to judge a RTS column. According to the equation (3), we could set different error voltage applied on V_o to acquire different number of judged RTS column in particular behavior. Compared with the real observation situation, the number and column position with 14.4 uV error voltage has the best consistence. The column position marked by the data process algorithm based on the equations above has obvious large column RTS noise, which can be seen from digital display platform. This condition have confirmed the accuracy of the method to detect RTS column. So we choose the 14.4 uV as main error voltage to analyze test data, and 9.6 uV as a supplement.

Many experiments has been done to validate the method and find the influence parameters. The sensor chips used in experiments are fabricated in Dongbu 0.13 um 1Poly-5Metal process with different correlated parameters design. Fig. 3 shows CIS chips and devices used for column RTS tested, including the tested sensor chip structure, chip appearance (front and back), test hardware device and visual interface respectively. The experiment results are shown below.

3.1 Gate channel size influence

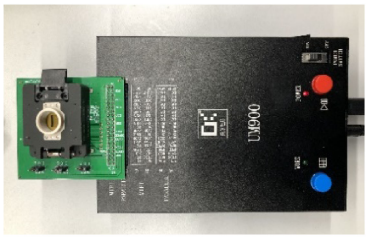
The relationship between column RTS noise level, expressed as the number of RTS column in specific error voltage, and transistor gate size, including width and length, in bitline bias transistor and comparator input transistors is shown in Fig. 4 and Fig. 5 separately.

From the Fig. 4 we can see, the gate width has no clear relationship with the column RTS noise, while Fig. 5 shows that the gate length influence the column RTS noise in an obvious way. The RTS column number decreases with the increase of gate length, indicating that by increasing the transistor gate length the column RTS noise can be effectively restrained. This result is in agreement with the measurement reported in [1, 13]. The reason that large gate length could decrease column RTS is illustrated in the following content.

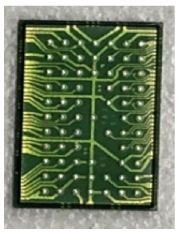


(a) sensor chip design structure

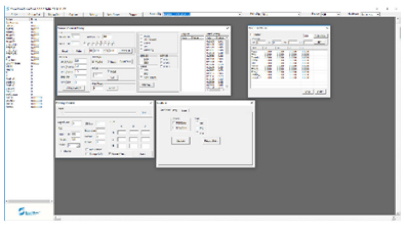
(b) chip appearance (front)



(c) test hardware device

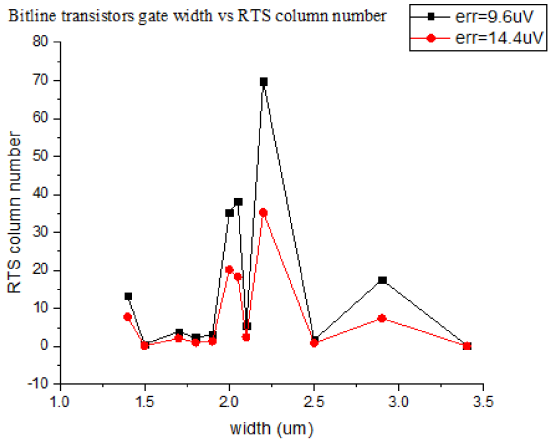


(d) chip appearance (back)

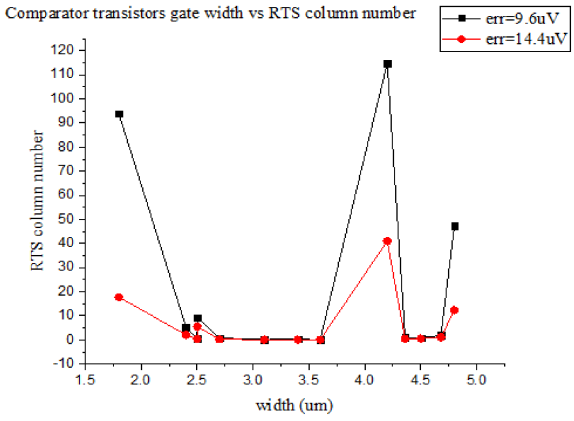


(e) visual interface

Fig. 3. CIS chips and devices used for column RTS tested

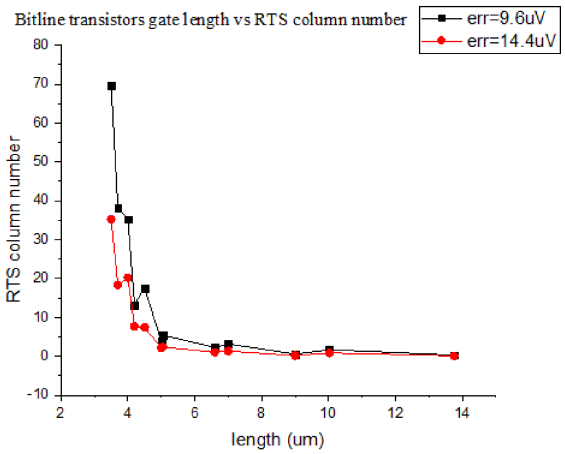


(a) Bitline transistor gate width

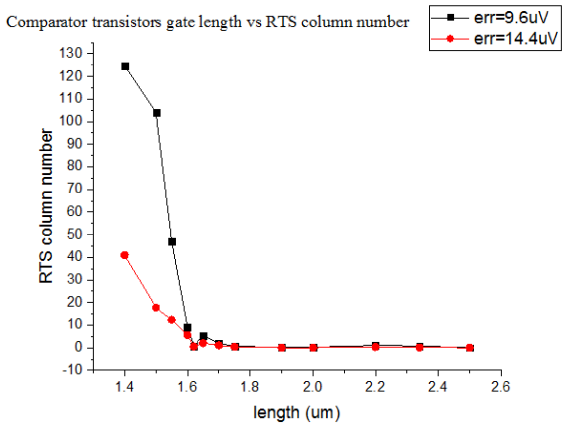


(b) Comparator transistor gate width

Fig. 4. Column RTS versus gate channel width.

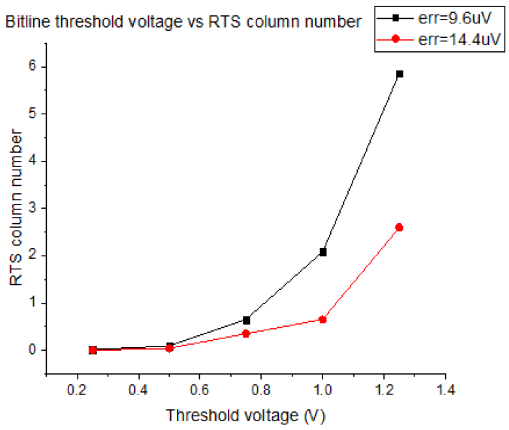


(a) Bitline transistor gate length

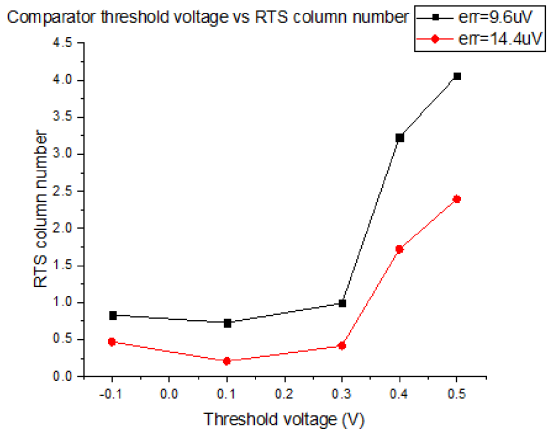


(b) Comparator transistor gate length

Fig. 5. Column RTS versus gate channel length



(a) Bitline transistor threshold voltage influence



(b) Comparator transistor threshold voltage influence

Fig. 6. Column RTS versus threshold voltage.

3.2 Threshold voltage influence

Similar as the expression in a), the relationship between the column RTS noise level and threshold voltage of bitline transistor and comparator input transistor is shown in Fig. 6.

According to the data in Fig. 6, an apparent inflection point can be seen from the curve, meaning that there exists a critical voltage value of threshold voltage in both source type. When the threshold voltage is higher than the critical voltage value, the RTS column number increase as the threshold voltage raise. In contrast, when the threshold voltage is lower than the critical voltage value, the RTS column number remain stable with the drop of threshold voltage. Due to the abnormal display condition existing in super low voltage threshold area, the best choice about threshold voltage to decrease the column RTS noise is setting the threshold voltage value a little lower than the critical voltage value mentioned above. It is noteworthy that the critical voltage value is not a fixed value and would change with the process condition, so it is necessary to conduct experiments to get the accurate critical voltage. For most cases in the experiments, the critical voltage value exists between 0.15 V and 0.3 V.

3.3 Combined relationship

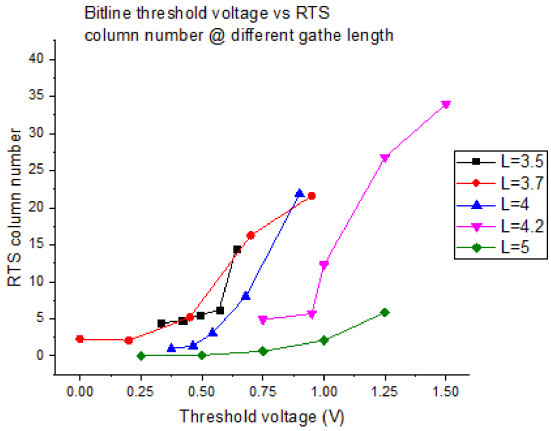
The Fig. 7 shows the combined relationship among column RTS, gate length and threshold voltage, from the two figures we can get the conclusion intuitively that for each type of transistor in different gate length, the RTS column number stay in a low level and begin to increase at specific voltage as threshold voltage increasing. Besides, the RTS column number decreased with larger gate length in similar threshold voltage. The conclusion conforms to the content shown in the part a) and b), and tells us that the best design to decrease the column RTS noise is setting the related transistor gate length as long as possible and setting the threshold voltage of relate transistor in a suitable value, 0.15 V to 0.3 V for most cases.

4. Discussion

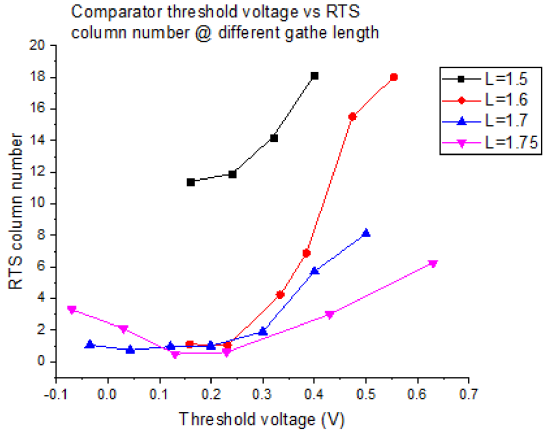
As Section 3 shows, the column RTS is related with gate channel length and transistor threshold voltage. The reasons for this situation are explained as follow.

4.1 Reason for gate channel size influence

As electron flows from source to drain, the defects existing in the silicon and oxide interface may trap and detrap the electron randomly, leading to the nonuniformity of electron flow temporally, which is the main cause of the RTS noise. So the temporal distribution of the process that a single mobile electron controlled by Si/SiO2 interface defects, and the number of electron flow along the channel per unit time are two vital influence factors of the RTS noise



(a) Bitline transistor parameters influence



(b) Comparator transistor parameters influence

Fig. 7. Column RTS versus channel length and threshold voltage

amplitude. When the gate channel length increase, the number of defects increase, meaning the increasing temporal uniformity of the process that trap and detrap the electrons. Besides, with the increased moving distance, the temporal distribution of the process that electron controlled by defects perform in a more steady status. So the column RTS amplitude decrease. As for the situation that gate channel width increase, the temporal distribution electron controlled by defects perform in a less steady status owing to the larger electron flow under the Si/SiO2 interface. So the change of column RTS level has no specific direction with the negative influence of the temporal distribution of electron controlled by defects and positive influence of increased total numbers of defects existing in the Si/SiO2 interface. This reason tallies with the content in [13].

4.2 Reason for threshold voltage influence

The method we used to decrease the threshold voltage is adopting the buried channel process, which can form the channel below the oxide and Si/SiO2 interface. When the electron flow in such channel, the electron is difficult to be trapped by the defects in the Si/SiO2 interface due to the long distance between the interface and the channel. The lower threshold voltage means the higher density of doping dose to form buried channel, leading to a higher proportion of electron flowing in the buried channel and staying far from the Si/SiO2 interface, which cause the decrease of column RTS level. As for the critical point, we guess it is the sign that most electron start to travel in the buried channel, so the lower threshold voltage than critical point has little influence on the column RTS level.

5. Conclusion

We designed a method to quantify and analyze the column RTS noise derived from bitline bias transistor and comparator input transistor, in CMOS image sensor. Based on the statistics and calculation about data acquired from a digital platform, the method is easy to be applied and could acquire a test result which has a good consistence with the real image quality. With this method we then conducted many experiments. The result has shown that the larger length of transistor gate could decrease the RTS column number while gate width had no obvious tendency about the effect on column RTS noise. And a proper threshold voltage of transistors, which means a little lower than the critical voltage, 0.15 V to 0.3 V for most cases, can make good contribution to restrain the column RTS noise.

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