ELectronics EXpress

IEICE Electronics Express, Vol.16, No.8, 1–4

LETTER

Characterization of P-hit and N-hit single-event transient using heavy ion microbeam

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Abstract P-hit and N-hit single-event transients are investigated using heavy ion microbeam. A novel layout placement was implemented in the test chip to distinguish SETs originating from P-hit and N-hit. Experimental results indicate both the P-hit and N-hit SETs show an exponential-like distribution in all target circuits. The SET cross sections and the average pulse width for P-hit and N-hit are also investigated. The well process, the transistor size and the layout topology significantly impact on the cross sections. Only the transistor size impacts on the average pulse width at low LET.

Keywords: single event transient, pulse width, cross section, soft error
Classification: Integrated circuits

1. Introduction

Single event transients (SETs) has become a major reliability concern for nanoscale technologies [1, 2, 3]. Reduced nodal capacitances and supply voltages decrease the minimal charge to cause a transient pulse [4, 5, 6, 7]. Higher operating frequencies make SETs more likely to be captured by the storage element [8, 9, 10, 11]. Some works have predicted that soft errors caused by SETs are higher than that caused by single event upset (SEU) [12]. The SET distribution and pulse width have become critical parameters to determine the soft error rate (SER) of integral circuits.

Although experimental measurement of SETs has been accomplished with a variety of techniques [13, 14, 15, 16], few works could distinguish SETs originating from PMOS transistors (P-hit) and NMOS transistors (N-hit) directly. For instance, a circuit design for separating SET is described in [17]. The combined inverters and NOR/NAND cells are used to measure P-hit and N-hit SETs independently. However, SET measurement results are limited by the circuit structure. It is hard to directly measure P-hit and N-hit SETs for any other circuit cells.

In this paper, P-hit and N-hit SETs are directly measured using heavy ion microbeam. To distinguish SETs originating from P-hit and N-hit, a novel odd-even-separation layout placement was implemented in the test chip. The SET distributions, SET cross sections and the average pulse widths for P-hit and N-hit are reported.

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DOI: 10.1587/elex.16.20190141
Received March 11, 2019
Accepted March 18, 2019
Publicized April 8, 2019
Copyedited April 25, 2019

2. Test chip design and experimental setup

2.1 Test chip design

A test chip was designed and fabricated in the commercial 65 nm bulk CMOS process. It contained five inverter chains and an autonomous SETs capture circuit. The main characteristics of the inverters are synthesized in Table I. Note that the inverter chains C–E were designed with different layout topologies, as shown in Fig. 1. To mitigate the effect of Propagation Induced Pulse Broadening (PIPB) [18] and charge sharing [19], each inverter chain only has 120 stages with purposive large transistor spacing.

Table I. Target circuits used in the test chip

Circuit number	PMOS WL W/L (nm)	NMOS WL W/L (nm)	Description
A	450/60	300/60	Noraml layout
B	450/60	300/60	Normal layout (Triple-well)
C	900/60	600/60	Noraml layout
D	450/60	300/60	Layout with SDS
E	450/60	300/60	Layout with DSD

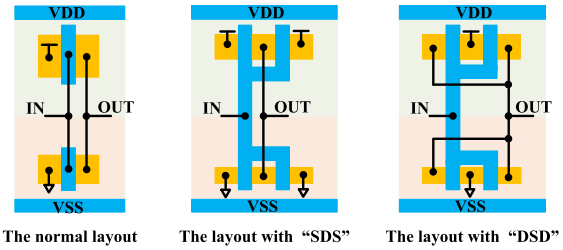

Fig. 1. The inverters with different layout topologies. Note that the equivalent transistor widths of target circuit D and E are consistent with that of target circuit C.

To distinguish SETs originating from P-hit and N-hit, a novel odd-even separation layout placement was used, as shown in Fig. 2. This layout placement separates the odd- and even-stage inverters to ensure the adjacent inverters have same sensitive transistors. For instance, when the input data is set to LOW, the sensitive NMOS transistors are located in the odd-stage inverters and the sensitive PMOS transistors are located in the even-stage inverters. The P-hit and N-hit SETs can be obtained when the microbeam explore different inverter regions. The autonomous SET capture circuit was based on the self-triggered SET pulse width measurement technique first described in

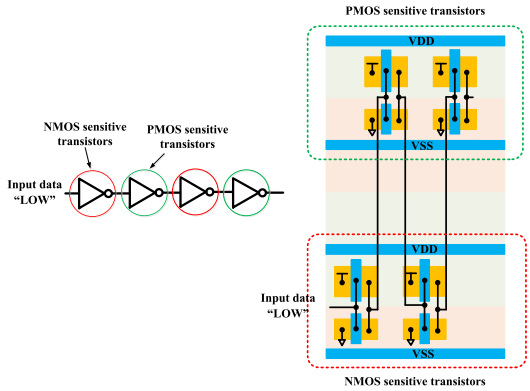

Fig. 2. The proposed odd-even separation layout placement.

[13]. It has a measurement range of 680 ps and a resolution of 40 ps.

2.2 Experimental setup

Heavy ion microbeam experiment was conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy. The microbeam equipment is shown in Fig. 3. The sulphur ion was used in the experiment. The linear energy transfer (LET) value was 12.2 MeV·cm^2/mg with the penetration range of 42.2 μm in silicon. The microbeam size was 3.2 μm × 2.5 μm at the target plane. Five inverter chains were irradiated respectively to obtain P-hit and N-hit SETs. The statistical SETs were read out by FPGA.

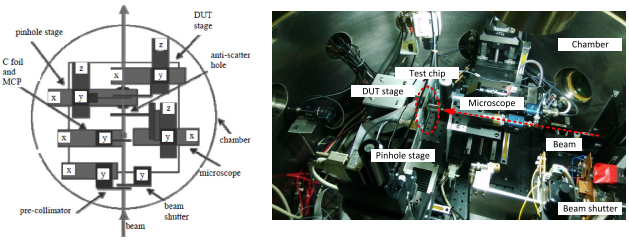

Fig. 3. Heavy ion microbeam equipment used in the experiment.

3. Experimental results

3.1 P-hit and N-hit SET distributions

The SET distribution for the target circuit A is shown in Fig. 4. An exponential-like pulse distribution is observed in both P-hit and N-hit SETs. The number of SETs shows an exponential increase with the pulse width increases. When the pulse width is longer than the peak value, the number of SETs shows a sharp decrease trend. The SET distributions for other inverters are shown in Fig. 5. Although these inverters have different transistor sizes and layout topologies, similar SET distributions are observed.

The peak pulse width is induced when an ion strikes the drain region of sensitive transistors. However, it is worth to note that some measured pulse widths exceed the peak value. Charge sharing between adjacent transistors is the mechanism to produce these longer pulses [19, 20]. Although the purposive large transistor spacing is implemented to mitigate charge sharing, some incident ions can still cause this effect.

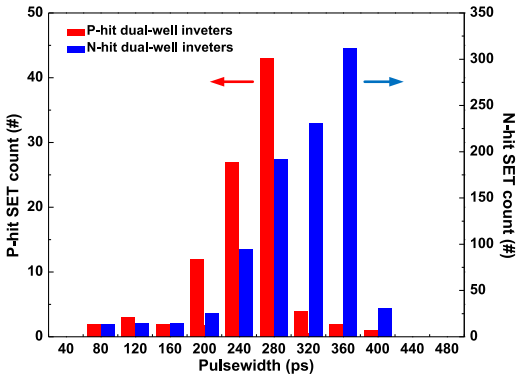

Fig. 4. The SET distributions for the target circuit A.

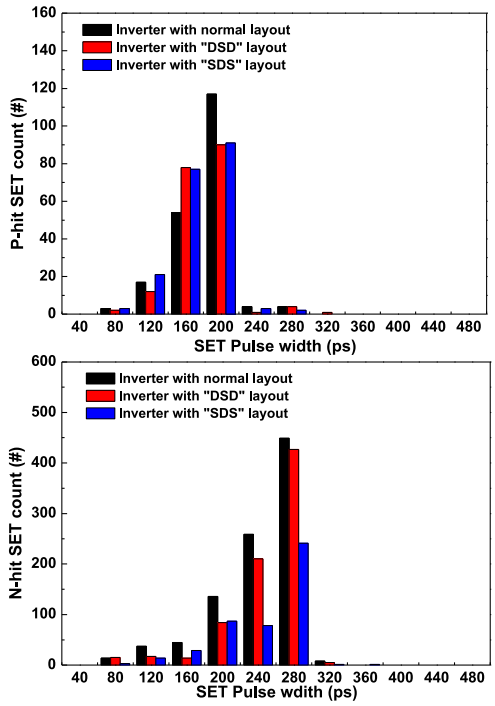

Fig. 5. The SET distributions for the target circuit C–E.

3.2 P-hit and N-hit SET cross sections

The SET cross sections for P-hit and N-hit are shown in Fig. 6. The N-hit cross sections are higher than P-hit cross sections in all target inverters. It indicates the NMOS sensitivity is larger than the PMOS sensitivity at low LET. This experimental result is different from the experimental data at high LET [17]. To match the current drive, the width of the PMOS transistor is about several times larger than the width of the NMOS transistor. It results in a large sensitive drain region for PMOS transistors [21, 22, 23]. Moreover, the bipolar amplification effect also significantly influences the PMOS transistors at high LET [24]. It enhances the PMOS sensitivity and results in higher SET cross sections.

However, the bipolar amplification effect is neglectable at low LET. The carrier drift-diffusion becomes the main mechanism to induce charge collection. The hole diffusion ability is smaller than the electron diffusion ability due to the lower mobility. It results in a larger sensitive area for NMOS transistors although the drain regions of NMOS

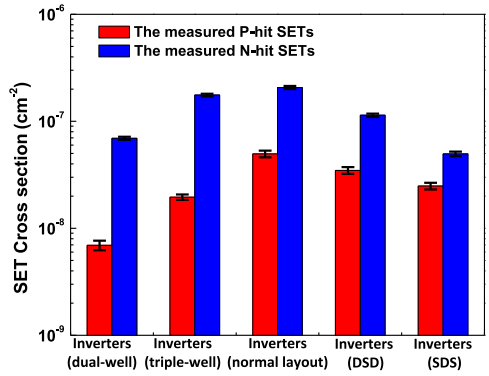

Fig. 6. The measured P-hit and N-hit SET cross sections for all target circuits.

transistors are smaller than those of PMOS transistors. Therefore, the SET cross sections for N-hit is higher at low LET.

It is worth to note that the well process and the layout topology impact on the P-hit and N-hit SET cross sections. The inverters in the triple-well process are more sensitive in both P-hit and N-hit compared with the dual-well inverters. The detail single event mechanisms to impact on SET sensitivity in the triple-well have been investigated in the previous works [25, 26, 27]. Different layout topologies also impact on the SET sensitivity of the inverters. For the SDS layout topology, two mechanisms impact the SET cross sections. Firstly, this layout topology reduces the drain area of PMOS and NMOS transistors. Secondly, the additional source region can help to collect more carriers. The SET cross sections for circuit E are smallest compared with measured results for circuit C and D. For the DSD layout topology, one mechanism impacts the SET cross sections. The source region of transistors separates the drain region of transistors. Although this layout topology does not reduce the drain region, an incident ion can only impact one part of the drain region. The SET cross sections for circuit D are smaller than measured results for circuit C. The detail discusses have been reported in our previous works [28, 29, 30, 31].

3.3 P-hit and N-hit average pulse widths

The average SET pulse widths for all target circuits are shown in Table II. The dual-well inverters and the triple-well inverters show similar average pulse widths although they are designed with different well processes. Because of the neglectable bipolar amplification effect, the deep N-well shows a slight influence on the P-hit and N-hit pulse width. The inverters with higher W/L rate show shorter average pulse widths. A higher drive current is the main mechanism to decrease the average pulse widths. Although the target circuit D and the target circuit E have the different layout topologies, they still show similar P-hit and N-hit SET pulse widths compared with the target circuit C. Experimental results indicate the layout topology slightly impacts on the average SET pulse width at low LET.

It is worth to note that the N-hit pulse widths show about 20% longer than the P-hit pulse width in all target circuits. The carrier recombination is the main reason to reduce the P-hit pulse width. Due to the high doping concentration of N-well, the hole recombination rate in PMOS transistors is higher than the electron recombination rate in NMOS transistors. The higher recombination rate reduces the density of ionized holes quickly. It results in reducing the charge collection of PMOS transistors and leads to short pulse widths.

Table II. The measured average SET pulse width

Circuit number	P-hit average pulse width (ps)	N-hit average pulse width (ps)
A	252	311
B	267	315
C	178	251
D	169	247
E	182	256

4. Conclusion

P-hit and N-hit SET experimental results are reported using heavy ion microbeam. A novel layout placement was implemented in the test chip to distinguish SETs originating from P-hit and N-hit. The number of P-hit and N-hit SETs show an exponential-like distribution in all target circuits. The number of SETs show an exponential increase with the pulse width increases while it shows a sharp decrease trend when the pulse width is over than the peak value. The SET cross sections and the average pulse width for P-hit and N-hit are also measured. Both the P-hit cross section and the average pulse width are smaller that N-hit results. The well process, transistor size and the layout topology significantly impact on the cross sections while only the transistor size impacts on the average pulse width.

Acknowledgments

This work is supported by National Natural Science Foundation of China (Grant No. 61804180). The authors would like to thank the HI-13 teams for heavy ion experiment supports.

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