

LETTER

Design and verification of universal evaluation system for single event effect sensitivity measurement in very-large-scale integrated circuits

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Abstract A flexible and multipurpose Single Event Effects (SEEs) testing system was developed for evaluating the reliability of nanoscale Very Large Scale Integrated Circuit (VLSI). The accurate detection, comparison and classification of latch-up, upset, and functional interrupt were achieved. In host PC part, two customized software systems were developed, including the Procise for maximal resources occupation and a C# based visual control interface for real-time communication. For hardware, a motherboard-daughterboard system guaranteed testing performance and kept its compatibility throughout testing. The fault injection and $^{181}\text{Ta}^{31+}$ irradiation results indicated the validity of proposed measurements and the stability of hardware operation. Importantly, the high anti-irradiation performance of device was also verified.

Keywords: FPGA, single event effects, heavy ions, irradiation

Classification: Integrated circuits

1. Introduction

With the feature size of Very Large Scale Integrated circuit (VLSI) continuously shrinking, the complexity and variety of Single Event Effects (SEE) phenomenon have been extended to some degree. For examples, Field Programmable Gates Arrays (FPGAs), Complex Programmable Logic Devices (CPLDs) and System on Chips (SoCs) with high processing ability and configuration flexibility are extremely sensitive to Single Event Latch-up (SEL), Single Event Upset (SEU), and Single Event Functional Interrupt (SEFI), which make their space application limited [1, 2, 3, 4, 5, 6]. Additionally, the SEE evaluation on these VLSIs also becomes very complex due to their abundant circuit resources and high transistor density. Ground SEE tests especially for heavy-ion test are the primary assessment for anti-irradiation evaluation in VLSIs. And almost all aerospace electronics must pass the test of heavy ion irradiation, which cause a great and urgent need in SEE test [7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17]. For memory

chips, the SEE test and characterization are simple at most of time because their control circuits and storage cell are clear and comprehensible. However, for multifunctional chips with high density, high speed and large resources, the SEEs occurred in these chips could not be identified directly through a simple test frame [2, 5, 6]. Besides, the high-frequency VLSIs also bring challenges on the effective identification of SEE. Therefore, developing an effective and universal SEE testing system for complex VLSI is necessary.

There existed problems such as rudimentary function and identification ways, low efficiency, low testing frequency and high costs in the specially designed SEE testing systems in the previous reports [4, 7, 14, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27]. Other methods, such as a convenient test implemented by the commercial evaluation board have also been published [28]. However, based on the existing evaluation boards, the majority of I/O blocks were restricted and only Joint Test Action Group (JTAG) interfaces could be used to provide configuration and read-back operation. Therefore, the dynamic and simultaneous monitoring of SEL, SEU and SEFI in different modules were unable to be achieved.

In this paper, we propose an effective detection and management method for SEL, SEU and SEFI phenomena in FPGA testing. A testing hardware system with power and communication interface ports inside was put forward. In addition, the corresponding logic functions, including a current monitor, a SEU checker and counter, and a SEFI classification were accomplished by a main control FPGA with Hardware Description Language (HDL) and implemented by a special designed Electronics Design Automation (EDA) software named Procise. The special space-application oriented synthesis, implementation and configuration of Devices Under Test (DUTs) were also executed in Procise. Finally, the fault injections and $^{181}\text{Ta}^{31+}$ irradiation tests confirmed the effectiveness of our testing system.

2. SEE testing requirements

To realize the actual on-orbit radiation environment requirements, the ground heavy ion parameter and testing standards (ESCC-25100, JESD57/JESD89, MIL-STD750E, ASTM-F1192 [9, 10, 11, 12, 13]), a flexible SEE testing system for VLSI was designed and constructed based on

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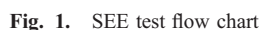
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SEL is prone to be induced by high Linear Energy Transfer (LET) particles irradiation, which is characterized by current surging phenomenon. SEL should be entirely prohibited because of its destructive nature. Additionally, SEU may occur in memories, routes or switch resources, while SEFI may exist in Power on Reset (POR) ports, Frame Registers (FR), the Global Signal (GS), or communication interfaces especially in SelectMAP (SMAP) [14, 15, 16, 17]. Though not so severe as the destructive SEL, the majority of SEU in routes or switch resources and SEFI in interfaces can also affect the on-orbit function of FPGA significantly. Thus, both SEU and SEFI should also be detected in real-time and addressed by the evaluation system.



A current monitor system was required to detect and record the current values and changes in DUT core currents, auxiliary currents and I/O ports. The core currents are the main current parameter for electronic devices, while the auxiliary currents are mainly for analog module if DUT possessed. All three currents should be detected in real-time. If more than 1 A current surging in each part of DUT happened, the SEL phenomenon would be confirmed and the system would cut-off the power supply automatically within 100 ms. As shown in Fig. 1, the current changes and SEL data are collected by host computer for further examination after the irradiation test.

POR, FR, GS and the communication interfaces were tested to evaluate the SEFI sensitive area, the interruption threshold and the deep influence in circuit level. Errors in the FR were detected based on the continuous checking of read and write functions during the test. Because the interrupt phenomenon in the FR could cause changes in control logic, the write or read command sent by control FPGA could then lose efficacy. POR failure could be examined by checking the high or low electrical level in

Upset errors could exist in embedded memories, flip-flops, registers, interconnect routes or switch resources covering nearly the whole DUT. In the SEU test, memory data was read back in dynamic ways and all of the checks and compare operation were finished by peripheral main control FPGA in motherboard based on its parallelism processing ability. The control register in interface ports could switch in read/write status. The readback file could be used to compare with the golden one in control FPGA and the SEU data in embedded memories, flip-flops, registers or interconnects would be distinguished and collected. To avoid the disturbance of SEL and SEFI phenomenon in heavy ion irradiation, dynamic check for SEFI and current changing were required. If any interruption or abnormal current appeared, the upset detection was stopped and the error data collected so far is regarded as invalid.

A block diagram of the SEE testing system shown in Fig. 2 was designed based on the corresponding guidelines and standards in Refs. [1, 9, 10, 11, 12, 13, 29, 30]. The system was separated into two parts with flexible pin connected motherboard-daughterboard structure with a reused motherboard to satisfy the cost reduction strategy.

A host computer with C[#] compiled visual control and operation interface (Fig. 3) was placed in the laboratory to control the SEE testing system. An additional action channel for bitstream download and debug use is also necessary. Furthermore, to supply the suitable voltages to the testing

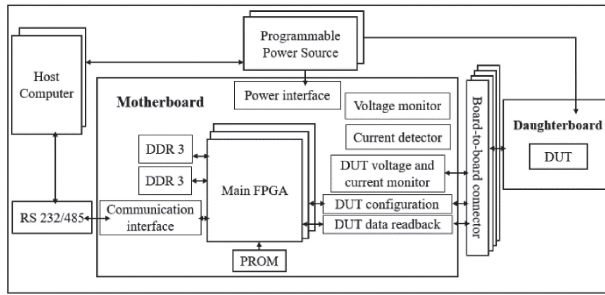


Fig. 2. Block diagram of the SEE testing system

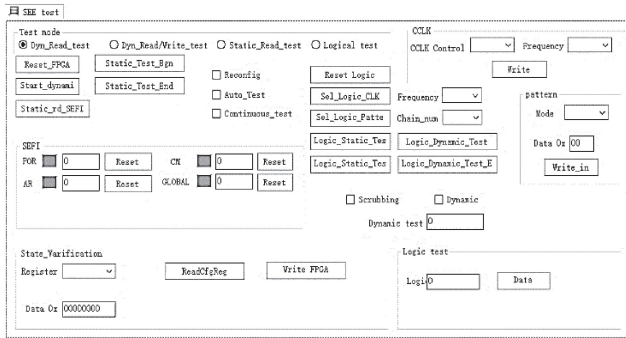


Fig. 3. Host computer control and operation interface

system, an Agilent N6705 power source with its debugging and monitoring software were utilized especially for the automatic protection of SEL. The current monitor screen was from the visual interfaces given by Agilent N6705.

4. Software configuration method and DUT setup

FPGA possessed diverse resources including the configuration logics, the internal block memories and D flip-flops is a good choice for DUT to examine the testing system. Different circuits in FPGA system would be presented and compared separately during the irradiation test. Detection in each separated module in FPGA is identical to the operation in other independent devices. The tests in D flip-flops and configuration logics are universal with other programmable logic devices due to their same structures. The internal block memory resources like commercial Random Access Memory (RAM), storing some basic information. Both the testing methods and even the error mitigation techniques between the block memory and the commercial RAMs are the same. For the Read-Only Memory (ROM) tests, the different points from the RAM tests are that the write enable and data input in RAM tests are forbidden in experiments.

The DUT adopted a 65 nm bulk silicon epitaxial process with a flip-chip geometry. For ion range consideration, the DUT substrate was thinned down to $\sim 34 \mu\text{m}$ before irradiation test. The general anti-SEL guard strips, the 12-T Dual Interlocked Storage Cell (DICE) in configuration memories and the redundant cells in D flip-flop were used as main radiation hardness techniques. All of the irradiation sensitive resources including 15 Mbit configuration memories, 6 Mbit block memories and 50 Kbit D flip-flops were configured by HDL to realize a maximum utilization ratio

and to make each module effective during the irradiation test. Moreover, the programmed DUT was fully connected to the main FPGA successfully.

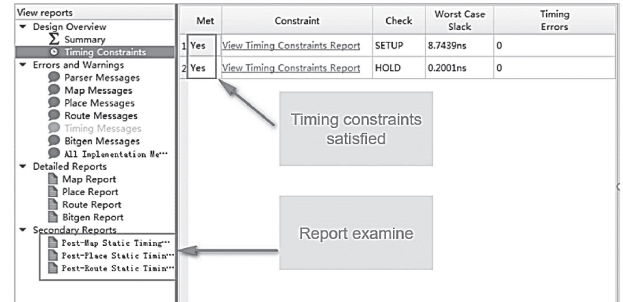


Fig. 4. Compatible FPGA configuration software

Table I. The primary TCL command in Procise

Manipulate	Basic TCL command
Device resources	set_device {name}
HDL resources input	read_verilog {file1}, {file2} ...
Top file chosen	Elaborate_top {top_module_name}
Constrain file input	read_constraint_{file}
Area chosen	area_opt
Speed option	speed_opt {number}
Map& Route	map& route
Bitstream generate	bitgen {design}. bit [-bmm {design}.bmm]

The bit stream, including the instantiation of block memory, configuration and D flip-flop resources was generated by Procise (Fig. 4) with reports detailed enough about routing and timing conditions. Tool Command Language (TCL) was also supported in Procise. The source code including resources input and bitstream generation were shown in Table I. Configuration memory distributed throughout the whole DUT was maximumly assigned by register command and checked during irradiation test in main FPGA by comparing with readback bitstream. Fig. 5 illustrates the configuration and data communication of all the embedded block memories in DUT. The additional soft error mitigation techniques and triple module redundancy were utilized alternatively from Procise based on the anti-irradiation capacity required by user. In the logic blocks, the full D flip-flops were used as shown in Fig. 6. The generated D flip-flop chain was initialized with different input patterns including all "0", all "1" or square wave. After initialization, the clock signal was stopped to put the D flip-flop chain under a static state. Errors could be detected and captured dynamically by error check module in main FPGA and were sent to the host computer in terms of protocol conversion from RS485 to USB.

5. Verification of testing system

5.1 Fault injection in written data

Fault injection platform usually aims to emulate a harsh space radiation environment where the high radiation ex-

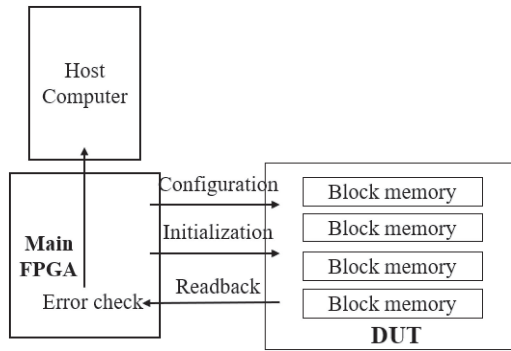


Fig. 5. Configuration and communication in DUT's Block memory

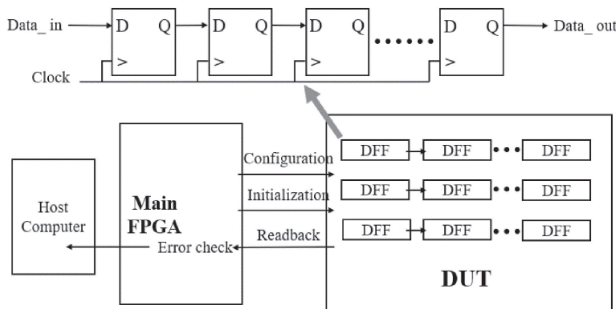


Fig. 6. Configuration and communication in DUT's D flip-flop

posure can lead to bits' flip in FPGA. It was useful to reexamine the error data distinction ability of the SEE testing system by performing randomly bitflips inside the bitstream. Any upsets could affect frame styles, modify the initial value of memory resources, and change the configured function in logical blocks and switching matrix.

Our motherboard-daughterboard design could achieve high-speed fault injection and could be easily controlled in the procedure of bitstream configuration from a board interface. Here, a main control FPGA in motherboard was used to generate test patterns via FPGA logic writing code. The same data writing operation and the same golden file were used in fault injection process, while the actual input data type in DUT were not "0x00", "0xFF" and "0x55" as the golden one. Considering the intuitive visual interface in host PC and time saving purpose in irradiation test, the fault injection was performed only in the DUT module and the operation in DUT was conducted by changing the bitstream of the write/read control modules in main FPGAs' HDL source. The fault injection in block memory module was shown in Table II.

Table II. Fault injection in writing control logic in block memory module

Right data type 55	Error data type 55
BM_write <= 1; write <= write + 1; BM_data <= 32'h5555_5555;	BM_write <= 1; write <= write + 1; BM_data <= BM_data + 1'b1;

To validate the error probing efficiency in our testing system, the injected cumulative counts downloaded to DUT were regarded as a string of SEUs. The SEU forced

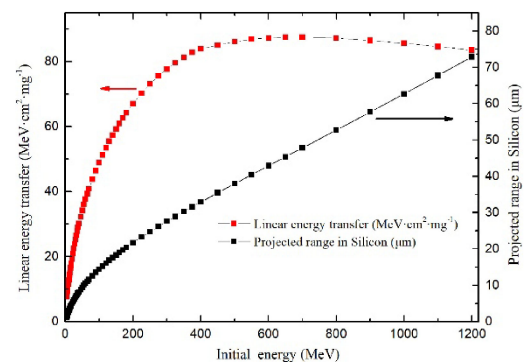
by the intentional fault injection could affect the memory resources and produce mismatch between the written data in the DUT and the golden file in the control FPGA. As shown in Table III, 0x55 data input was the command of host computer corresponding to the golden data (0x55). However, with the HDL code changing to the cumulative number in Table II, a series of errors with continuous addresses information appeared in host PC (Table III), which indicates the intact data discrimination and presentation capability of system.

Table III. Injected error extraction after comparison with golden data

Error counts	Error address	Error data	Golden data
001	1	01	55
002	2	02	55
003	3	03	55
004	4	04	55
005	5	05	55
...

5.2 Heavy ion experiment

To verify the effectiveness of our flexible SEE testing system, heavy ion irradiation experiment was also necessary. The vertical heavy-ion incidence irradiation experiments were conducted to explore the SEL, SEU and SEFI performance of radiation-hardened DUTs. Heavy ion test was performed in air at HIRFL in the Institute of Modern Physics, Chinese Academy of Sciences. Ion beams pass through a vacuum/air transition foil where both Al-foils and air act as energy degraders to adjust beam energy. The swift heavy ions were $^{181}\text{Ta}^{31+}$ with initial energy of 2262.5 MeV. After the 12.5 μm scintillator detector, 14.7 μm titanium window and 40 mm air distance, the ion energy was at ~ 1299.5 MeV. The relations between LET values and energy and between ion ranges in silicon and energy are shown in Fig. 7. During irradiation test, the ion fluence of each test was controlled in 10^7 ions/ cm^2 . Based on SEE testing requirements and DUT configuration state illustrated above, the configuration cell and functional status could be operated, monitored, recorded, and presented in host computer.

Fig. 7. Linear energy transfer and projected range of $^{181}\text{Ta}^{31+}$ vs. initial energy

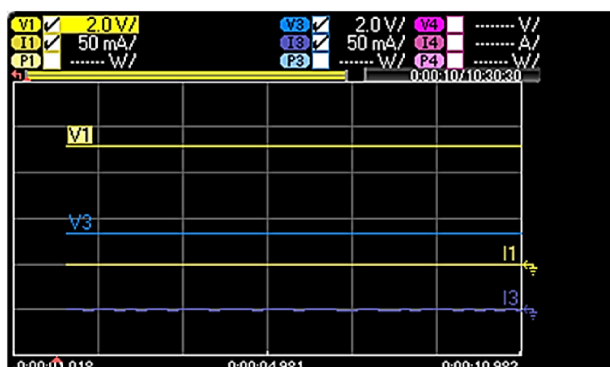


Fig. 8. Multichannel current detection interface

Due to the guard strips, no single event latch-up (SEL) phenomenon occurred in DUT during the whole testing under 60°C even with $^{181}\text{Ta}^{31+}$ ions (LET: $81\text{--}84\text{ MeV}\cdot\text{cm}^2/\text{mg}$) at $10^4\text{ ions}\cdot\text{cm}^{-2}\cdot\text{s}^{-1}$. The visual interface of current monitor was shown in Fig. 8. Considering the accuracy of experimental results and the difficulties of operation on the large-size flip-flop chips, higher temperatures are not tested. The strong anti-SEL capacity with SEL threshold over $80\text{ MeV}\cdot\text{cm}^2/\text{mg}$ could also be concluded at temperature $\leq 60^{\circ}\text{C}$. Because the end current in V_{CCAUX} and V_{CCINT} were only increased for $\sim 5\%$ (from 25.34 mA to 26.61 mA) and for $\sim 2\%$ (from 2.83 A to 2.89 A), respectively. In SEFI detection, the frame registers and configuration interfaces were not influenced by $^{181}\text{Ta}^{31+}$ ions. However, the POR port and global signals have detected the error information within the fluence of $10^7\text{ ions}/\text{cm}^2$.

The SEU is generally characterized by cross section (σ) and σ is equal to $(N/(F\times M))$, where F is the total fluence of $^{181}\text{Ta}^{31+}$ in per square centimeter, N is the number of upsets measured, and M is the number of DUT bits. Three different cross section values including $\sim 6.3 \times 10^{-8}\text{ cm}^2/\text{bit}$ in internal block memory, $\sim 6.2 \times 10^{-13}\text{ cm}^2/\text{bit}$ in configure memory, and $\sim 8.0 \times 10^{-8}\text{ cm}^2/\text{bit}$ in D flip-flop were calculated. These results verified the effectiveness of the testing system.

6. Conclusion

In this paper, a SEE testing system including visual control interface in PC and motherboard-daughterboard testing boards were developed and successfully utilized in VLSI evaluation. The manufactured flexible hardware system adopted board separation techniques, which make majority of control resources in the motherboard reusable and the logic design method as well as HDL codes portable. Furthermore, the ProCise software can easily make under evaluated devices configured into maximal resources occupation status within application-oriented purpose. The results of fault injection and heavy ion experiment on a high-density FPGA, particularly for the diverse SEU cross sections, have directly verified the accuracy of real-time initial data transfer, error data distinction and error information presentation of our evaluation system. The final DUT is a prime representative of complex devices. As

illustrated in section 4, for the universal RAM, ROM and other programmable devices, the implementation for SEE evaluation in our designed system are simpler and quicker.

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