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LETTER

A 14 bit 500 MS/s SHA-less pipelined ADC with a highly linear input buffer and power-efficient supply voltage domain arrangement in 40 nm CMOS

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Abstract In this paper, a 14 bit 500 MS/s SHA-less pipelined Analog-to-Digital Converter (ADC) realized in 40 nm CMOS technology is presented. A 2.5 V powered buffer that exhibits a comprehensive bootstrap architecture is proposed to achieve the trade-off between linearity and power consumption. Besides, the high-voltage-thin-oxide-device design is incorporated to further improve the linearity. In the meantime, an improved supply voltage domain arrangement is proposed to achieve a single power design and improve structural power efficiency. The measured Signal-to-Noise-and-Distortion-Ratio (SNDR) and Spurious-Free-Dynamic-Range (SFDR) are 71 dB and 79 dBc at 120.2 MHz input signal under 500 MS/s. The ADC occupies an active area of 0.4 mm^2 and consumes a total power of 300 mW.

Keywords: pipelined ADC, SHA-less, buffer, CMOS technology, voltage domain arrangement

Classification: Integrated circuits

1. Introduction

As wireless communication technology is advancing, the requirements of accuracy and speed for Analog-to-Digital Converters (ADCs) are increasing. Compared with other architectures, a pipelined ADC is more suitable for high-speed and high-resolution applications like the wideband receiver system [1, 2, 3]. A SHA-less architecture with an input buffer has been widely employed to design high-speed pipelined ADCs [4, 5]. However, the input buffer's dynamic performance usually limits the system's linearity [6, 7]. High-speed ADC design also benefits from the decreasing process dimension in power and chip area consumption [8, 9, 10], but the deep-submicron technology requires supply voltage domain arrangement to fully exploit its benefit considering the decreasing voltage supply [11, 12, 13].

A comprehensive bootstrape input buffer with a current compensation method is proposed here to achieve the trade-off between linearity and power consumption. The proposed architecture also make use of both thin-oxide devices and thick-oxide devices with a single 2.5 V supply, thereby further improves the linearity and enlarge the input swing. In the meantime, back-gate voltage chasing design is proposed to ensure all the thin-oxide devices work safely.

To deal with the decreasing voltage supply in the deep-submicron technology, an improved supply voltage domain arrangement is proposed in this study. With the help of elevated power/ground supplies provided by the on chip low dropout regulator (LDO), single-power design and structural power efficiency improvement are realized.

This study is organized as follows: Section 2 introduces the topologies and implementation, which involves the ADC core design, the highly linear input buffer design and the improved supply voltage domain arrangement. Section 3 presents the measurement results of the ADC. Finally, Section 4 draws the conclusions.

2. Topologies and implementation

As shown in Fig. 1, the design is a SHA-less 14-bit pipelined ADC. It consists of a RF input buffer, an ADC core and a digital module. The RF input buffer incorporates a comprehensive bootstrap architecture. The ADC core consists of six 2.5-bit MDAC stages and at last a 2-bit Flash sub-ADC. The first stage is a SHA-less 2.5-bit multiplying digital-to-analog converter (MDAC) frontend. It is followed by five 2.5-bit MDAC stages and at last a 2-bit flash sub-ADC. Based on the supply arrangement, the buffer and amplifiers in each stage are supplied by 2.5 V while the comparators, switches and the digital module work in the 0.8/1.7 V supply domain.

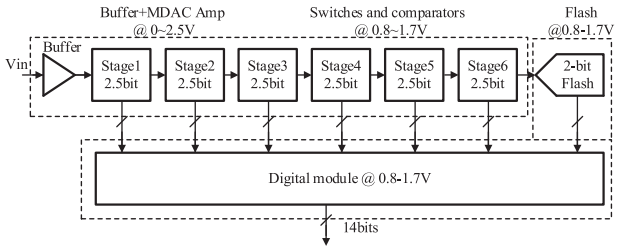

Fig. 1. Architecture of the proposed SHA-less pipelined ADC

2.1 ADC core design

The ADC core consists of six 2.5-bit MDAC stages and at last a 2-bit Flash sub-ADC. The structure of each MDAC stages is similar, its implementation and timing diagram of the sampling clocks is illustrated in Fig. 2.

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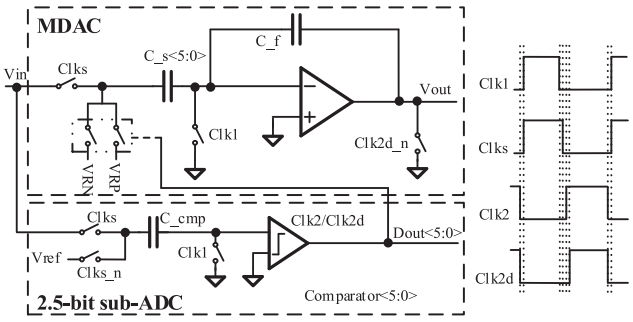

Fig. 2. Implementation of each stages

The input signal Vin is sampled at the falling edge of Clk1 by MDAC and sub-ADC. Sampling capacitors of sub-ADC are then connected to Vref at the falling edge of Clks and the comparators start comparison at the raising edge of Clk2. Latched at the raising edge of Clk2d, the results of comparators are sent to control the switches in MDAC connecting to reference levels of VRN or VRP. This process takes the difference between the sampled voltage and its quantized version to obtain the residual voltage.

The amps in each MDAC stages then amplify the residual voltage and the stage gain is determined by the ratio of C_s and C_f. A foreground calibration algorithm proposed by [14] is employed to correct the mismatch of capacitors for more precise gain. Telescopic cascode op amps with gain boosting on both the NMOS side and the PMOS side are also employed to realize large open-loop DC gain and high gain bandwidth which can further address the nonlinearity and noise [15].

In order to reduce the impact of aperture errors, the size of the sampling switches in MDACs and sub-ADCs are adjusted to keep the same time constant with different size of sampling capacitors. All these switches are also designed with bootstrapped architecture to improve the linearity [16].

The 2.5-bit sub-ADCs in each MDAC stages and the 2-bit sub-ADC in the last stage consist of the same comparators. The input offset storage (IOS) technique and the structure with pre-amplifiers are employed to realize a high speed and low offset comparator design which can improve the overall performance of the pipelined ADC [17].

2.2 Highly linear buffer design

The input buffer is the first module on the signal path, so its linearity determines the theoretical maximum linearity that the ADC can achieve [18]. In the conventional design, a pseudo-differential NMOS source follower has commonly served as the input buffer [19, 20, 21], of which the transfer function can be concluded in the equation as:

$$\frac{V_{out}}{V_{in}} = \left[1 + \left(g_m Z_L + \frac{Z_L}{Z_\pi}\right)^{-1}\right]^{-1} \approx 1 - \frac{1}{g_m Z_L} \qquad (1)$$

where V_{in} and V_{out} is the input and output of the buffer, Z_L is the load, g_m is the transconductance of the source follower device and Z_π is the input impedance. So, the non-linearity of the buffer is given as:

$$\frac{\Delta V_{out}}{V_{in}} = \frac{\Delta g_m}{g_m} \times \frac{1}{1 + g_m Z_L} \qquad (2)$$

A lot of efforts have been made to improve the linearity with low power consumption based on the equation (2) [22, 23, 24].

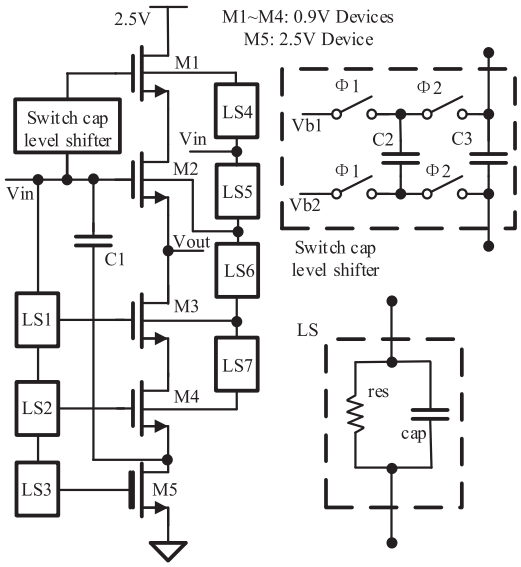

Fig. 3. Simplified schematic of the buffer proposed in this paper

In this study, the simplified schematic of proposed buffer is shown in Fig. 3. To maximize the linearity, a 2.5 V power supply is taken for the buffer since large voltage headroom can achieve lower distortion, especially for large input signal. C1 is the feed-forward linearization replica capacitor, capable of reducing the power consumption to 70% [25]. In the proposed comprehensive bootstrap architecture, M2 is the NMOS source follower transistor, and M3~M5 compose the current mirror. M1 and the switch cap level shifter (LS) can boost the drain voltage of M2 and help the output voltage Vout follow the input voltage Vin better. The linearity can be further improved as the gate voltages of the M3~M5 are also boosted by the level shifters. Unlike the switch cap structure, a simpler level shifter that consists of a resistance and a capacitor is employed to avoid the effects of the multi-phase clock. Besides, the back-gate voltage chasing design helps each device whose back-gate is boosted by the level shifter avoid the variation of the back-gate-source voltage and effectively reduce the non-linearity caused by the body effect.

This proposed architecture also makes the high-voltage-thin-oxide-device design possible. In 40 nm technology, a thin gate transistor can provide a larger g_m compared with a thick gate one with the same area and power consumption [26, 27, 28]. This suggests that the use of the thin gate transistor can effectively reduce the non-linearity owing to g_m variation. In the proposed comprehensive bootstrap architecture buffer, M1~M4 are 0.9 V thin gate devices which can achieve a four-terminal voltage variation less than 0.9 V. M5 is a 2.5 V thick gate device considering the unavoidable large voltage variation.

2.3 Improved supply voltage domain arrangement

To achieve a better balance between performance and power consumption, multiple power supplies design has been used in high-speed ADCs [29, 30, 31]. However, these methods will result in complex power plans and consuming more power structurally. Inspired by the design in [32], an improved supply voltage domain arrangement is proposed as shown in Fig. 4.

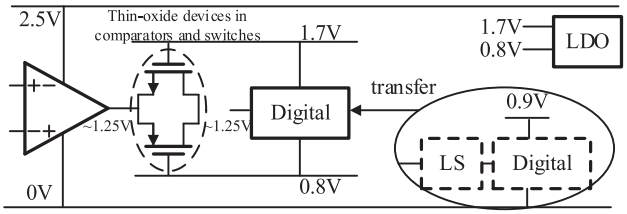

Fig. 4. Improved supply arrangement

In the proposed supply domain arrangement, the buffer and the amplifiers in each stage are supplied by 2.5 V voltage while the comparators and the switches are working in the elevated 1.7/0.8 V supply domain. Given the fast rise and fall time characteristics, smaller RC time constant and smaller parasitic capacitance, the thin-oxide devices should be used in the comparators and switches design [32].

Fig. 5 shows that the proposed supply domain arrangement also transfers the digital module to the elevated 1.7/0.8 V supply domain. The 14 bit digital data is level shifted to the 0.9 V power domain while interfacing to the outside by level shifters. All the supplies (e.g. 0.8 V, 1.7 V and 0.9 V) are generated by on chip LDOs so that the proposed ADC can work with a single 2.5 V supply. Besides, all the level shifters between the pipelined-stages and the digital module can be removed since data from the pipelined-stages are generated by the comparators that works in 1.7/0.8 V supply domain as well. According to the simulation, the total power consumption can be reduced by 10%.

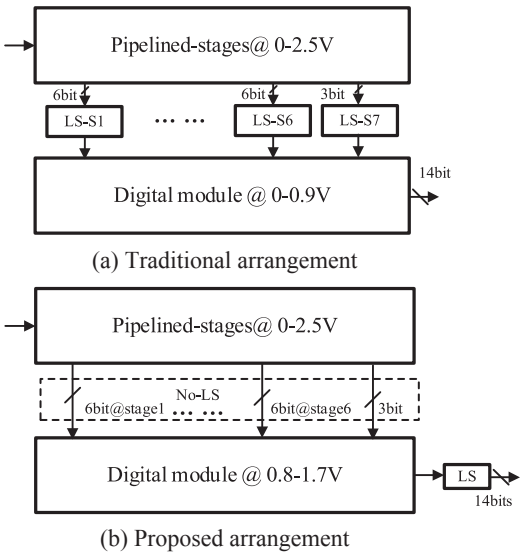

Fig. 5. Two digital module supply arrangements

3. Measurement results

The proposed ADC is fabricated in a 40 nm CMOS technology, which is included in a transceiver. The micrograph of the chip is shown in Fig. 6, and the active area of one ADC is 0.4 mm^2. The floor plan of the ADC is shown in Fig. 7.

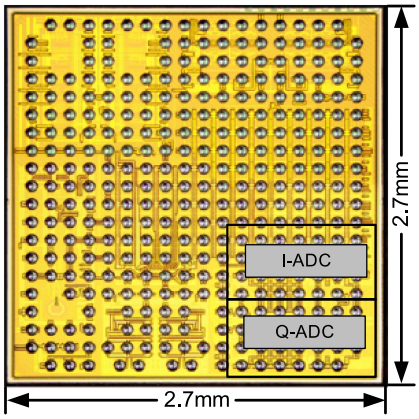

Fig. 6. The micrograph of the chip.

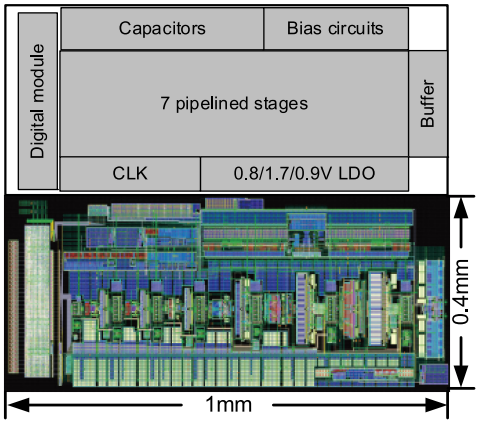

Fig. 7. The floor plan of the ADC

The measurement results of the ADC are given in Fig. 8. According to the measurements, the proposed ADC achieves a SNDR of 71 dB and a SFDR of 79 dBc at 120.2 MHz input signal with 500 MS/s sampling rate while consuming a power of 300 mW with 2.5 V supply. With an input signal at the Nyquist frequency, the proposed ADC achieves a SNDR of 69 dB and a SFDR of 77.8 dBc. More measurement results of different input frequencies are given in Fig. 9.

The performance of the proposed ADC compared with other stage-of-art designs is listed in Table I. The figure of merit (FOM) is calculated, which is expressed as

$$FOM = \frac{Power}{2^{ENOB} \cdot Sample\_rate} \tag{3}$$

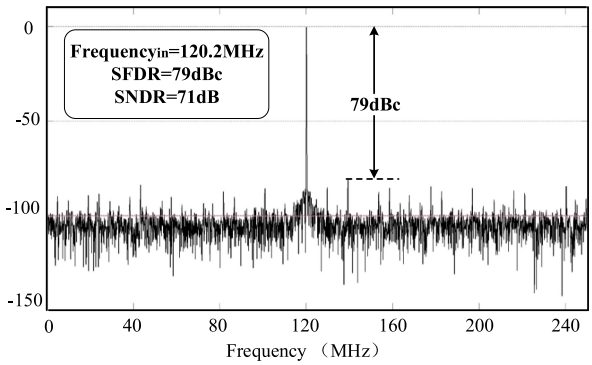

Fig. 8. Measurement results for the ADC in 500 MS/s

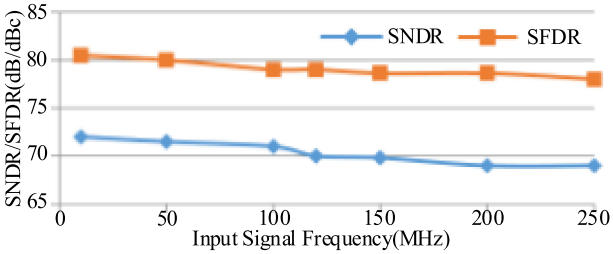

Fig. 9. Measurement results of different input frequencies

Table I. Performance comparison.

	[5]2018	[31]2016	[33]2016	This work
Technology	130 nm CMOS	0.18 um CMOS	65 nm CMOS	40 nm CMOS
Supply (V)	3.3	3.3/1.8	2.5	2.5
Sample rate (MS/s)	120	500	800	500
Resolution (bit)	12	12	12	14
SFDR (dBc)	83.6	82	67.5	77.8
SNDR (dB)	66.9	65.6	61.3	69
Area (mm^2)	6	-	3.8	0.4
Power (mW)	180	800	720	300
FOM (pJ/step)	0.83	-	0.58	0.26

4. Conclusion

In this study, a 14-bit 500 MS/s SHA-less pipelined ADC is proposed and fabricated in 40 nm CMOS technology. According to the measurement results, the proposed ADC achieved high linearity for wide band transceiver application with a quite low power consumption of 300 mW when the sampling rate reaches 500 MS/s. The design of ADC can also be conveniently migrated in other transceivers since it incorporates a single power supply.

References

[1] S. Devarajan, *et al.*: "A 12-b 10-GS/s interleaved pipeline ADC in 28-nm CMOS technology," IEEE J. Solid-State Circuits **52** (2017) 3204 (DOI: 10.1109/JSSC.2017.2747758).
[2] D. Vecchi, *et al.*: "An 800 MS/s dual-residue pipeline ADC in 40 nm CMOS," IEEE J. Solid-State Circuits **46** (2011) 2834 (DOI: 10.1109/JSSC.2011.2164301).
[3] M. Chu, *et al.*: "A 10-bit 200-MS/s zero-crossing-based pipeline ADC in 0.13-µm CMOS technology," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **23** (2015) 2671 (DOI: 10.1109/TVLSI.2014.2371453).
[4] W. Ke, *et al.*: "A 14-bit 100 MS/s SHA-less pipelined ADC with 89 dB SFDR and 74.5 dB SNR," IEICE Electron. Express **12** (2015) 20150070 (DOI: 10.1587/elex.12.20150070).
[5] Z. K. Zhou, *et al.*: "A 12 bit 120 MS/s SHA-less pipeline ADC with capacitor mismatch error calibration," IEICE Electron. Express **15** (2018) 20180481 (DOI: 10.1587/elex.15.20180481).
[6] R. Wang, *et al.*: "A 3.3 mW 12 MS/s 10 b pipelined ADC in 90 nm digital CMOS," IEEE International Solid-state Circuits Conference Digest of Technical Papers (2005) (DOI: 10.1109/ISSCC.2005.1493977).
[7] D. Kim, *et al.*: "A wideband fully differential source follower," Analog Integr. Circuits Signal Process. **72** (2012) 155 (DOI: 10.1007/s10470-011-9750-2).
[8] L. Kull, *et al.*: "28.5 A 10 b 1.5 GS/s pipelined-SAR ADC with background second-stage common-mode regulation and offset calibration in 14 nm CMOS FinFET," IEEE International Solid-State Circuits Conference Digest of Technical Papers (2017) (DOI: 10.1109/ISSCC.2017.7870467).
[9] M. Inerfield, *et al.*: "An 11.5-ENOB 100-MS/s 8 mW dual-reference SAR ADC in 28 nm CMOS," IEEE Symposium on VLSI Circuits Digest of Technical Papers (2014) (DOI: 10.1109/VLSIC.2014.6858453).
[10] B. W. Xu, *et al.*: "A 23 mW 24 GS/s 6 b time-interleaved hybrid two-step ADC in 28 nm CMOS," IEEE Symposium on VLSI Circuits Digest of Technical Papers (2016) (DOI: 10.1109/VLSIC.2016.7573535).
[11] J. Fang, *et al.*: "A 5-GS/s 10-b 76-mW time-interleaved SAR ADC in 28 nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers **64** (2017) 1673 (DOI: 10.1109/TCSI.2017.2661481).
[12] K. Tanaka, *et al.*: "A 1.6 GS/s 3.17 mW 6-b passive pipelined binary-search ADC with memory effect canceller and reference voltage calibration," ESSCIRC Conference 2015-41st European Solid-State Circuits Conference Digest of Technical Papers (2015) (DOI: 10.1109/ESSCIRC.2015.7313893).
[13] T.-V. Cao, *et al.*: "A 9-bit 50 MS/s asynchronous SAR ADC in 28 nm CMOS," Nordic Microelectronics Conference Digest of Technical Papers (2012) (DOI: 10.1109/NORCHP.2012.6403105).
[14] S. Roy, *et al.*: "Foreground calibration technique of a pipeline ADC using capacitor ratio of multiplying digital-to-analog converter (MDAC)," Microelectronics J. **44** (2013) 1336 (DOI: 10.1016/j.mejo.2013.09.004).
[15] J. F. Wu, *et al.*: "A 240-mW 2.1-GS/s 52-dB SNDR pipeline ADC using MDAC equalization," IEEE J. Solid-State Circuits **48** (2013) 1818 (DOI: 10.1109/JSSC.2013.2259013).
[16] H. Pan, *et al.*: "A 3.3-V 12-b 50-MS/s A/D converter in 0.6-µm CMOS with over 80-dB SFDR," IEEE J. Solid-State Circuits **35** (2000) 1769 (DOI: 10.1109/4.890290).
[17] L. Zhao, *et al.*: "A high speed low power latched comparator for SHA-less pipelined ADC," J. Circuits Syst. Comput. **22** (2013) 1350004 (DOI: 10.1142/S0218126613500047).
[18] L. Li, *et al.*: "A novel input buffer used for SHA-less pipeline ADC," Appl. Mech. Mater. **678** (2014) 501 (DOI: 10.4028/www.scientific.net/AMM.678.501).
[19] K. Hadidi, *et al.*: "A highly linear cascode-driver CMOS source-follower buffer," IEEE International Conference on Electronics, Circuits, and Systems Digest of Technical Papers (1996) (DOI: 10.1109/ICECS.1996.584657).
[20] I. Ahmed, *et al.*: "A low-power capacitive charge pump based pipelined ADC," IEEE J. Solid-State Circuits **45** (2010) 1016 (DOI: 10.1109/JSSC.2010.2042524).
[21] W.-C. Song, *et al.*: "A 10-b 20-Msample/s low-power CMOS ADC," IEEE J. Solid-State Circuits **30** (1995) 514 (DOI: 10.1109/4.384164).
[22] A. M. A. Ali, *et al.*: "A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs Jitter," IEEE J. Solid-State Circuits **41** (2006) 1846 (DOI: 10.1109/JSSC.2006.875291).
[23] M. V. Campos and C. A. R. Filho: "A high-speed low-distortion CMOS source follower buffer," IEEE Latin Am. Trans. **11** (2013)

677 (DOI: 10.1109/TLA.2013.6533954).
[24] A. M. A. Ali, *et al.*: "A 14 bit 1 GS/s RF sampling pipelined ADC with background calibration," IEEE J. Solid-State Circuits **49** (2014) 2857 (DOI: 10.1109/JSSC.2014.2361339).
[25] A. M. A. Ali, *et al.*: "A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration," IEEE J. Solid-State Circuits **45** (2010) 2602 (DOI: 10.1109/JSSC.2010.2073194).
[26] C. Constantinescu: "Impact of deep submicron technology on dependability of VLSI circuits," International Conference on Dependable Systems and Networks Digest of Technical Papers (2002) (DOI: 10.1109/DSN.2002.1028901).
[27] R. Pelliconi, *et al.*: "Power efficient charge pump in deep sub-micron standard CMOS technology," IEEE J. Solid-State Circuits **38** (2003) 1068 (DOI: 10.1109/JSSC.2003.811991).
[28] B. Yu, *et al.*: "Reverse short-channel effects and channel-engineering in deep-submicron MOSFETs: Modeling and optimization," IEEE Symposium on VLSI Circuits Digest of Technical Papers (1996) (DOI: 10.1109/VLSIT.1996.507833).
[29] Y. Z. Dong, *et al.*: "15.5 A 930 mW 69 dB-DR 465 MHz-BW CT 1–2 MASH ADC in 28 nm CMOS," IEEE International Solid-state Circuits Conference Digest of Technical Papers (2016) (DOI: 10.1109/ISSCC.2016.7418015).
[30] M. Brandolini, *et al.*: "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," IEEE J. Solid-State Circuits **50** (2015) 2922 (DOI: 10.1109/JSSC.2015.2464684).
[31] L. Li, *et al.*: "A 12 bit 500 MS/S SHA-less ADC in 0.18 um CMOS," IEEE International Nanoelectronics Conference Digest of Technical Papers (2016) (DOI: 10.1109/INEC.2016.7589282).
[32] C. Y. Chen, *et al.*: "A 12-bit 3 GS/s pipeline ADC with 0.4 mm 2 and 500 mW in 40 nm digital CMOS," IEEE J. Solid-State Circuits **47** (2012) 1013 (DOI: 10.1109/JSSC.2012.2185192).
[33] M. Ni, *et al.*: "A 12 bit 800 MS/s time-interleaving pipeline ADC in 65 nm CMOS," IEEE International Conference on Electron Devices and Solid-State Circuits Digest of Technical Papers (2016) (DOI: 10.1109/EDSSC.2016.7785290).