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LETTER

# Linearization of power amplifiers with mismatched output impedance using on-line digital pre-distortion structure

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**Abstract** This letter introduces a novel on-line digital pre-distortion structure for linearizing RF power amplifier under the output impedance mismatch conditions. Unlike traditional off-line structures, the proposed structure updates its weight parameters adaptively synchronizing with the power amplifier load impedance. Furthermore, this letter analyses with a MOSFET model and proves that the output conductance of MOSFET are relevant to nonlinearity of power amplifier with variable load impedance. To verify this structure and the analysis, a simulation on MATLAB Simulink was built using a N-channel MOSFET based on Shichman-Hodges model. Proposed on-line Digital Pre-Distortion structure significantly acquired better linearity performance with variable load impedance than conventional off-line structures.

**Keywords:** linearization technique, output impedance mismatch
**Classification:** Microwave and millimeter-wave devices, circuits, and modules

## 1. Introduction

Cellular mobile communication is stepping into its fifth generation. With continued escalation requirements for higher efficiency, compensating the nonlinearity of radio frequency system has courted much attention [1, 2]. However, the nonlinearity of whole system largely derives from Power Amplifier (PA) [3, 4, 5, 6].

Researchers have put forward massive linearization technologies [7, 8, 9, 10, 11, 12, 13] for PA. Digital Pre-Distortion (DPD) system was proved an efficient [14, 15] and adaptive [16, 17] one among all the techniques. However, linearity performance degrades severely when antenna mismatched with PA output impedance even with traditional off-line DPD applied [18]. Off-line DPD structure needs frequent retraining process when dealing with dynamic environments [19].

To overcome the drawback of off-line structure, this letter introduces an adaptive on-line DPD structure. Our structure is able to rapidly and stably follow the variable load impedance and achieves excellent linearity performance.

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## 2. Output impedance mismatch conditions

When load impedance match with output impedance, no additional voltage was reflected to transistor. To study the additional voltage in the mismatch conditions, we use a MOSFET transistor formula modelled by previous researchers [20]. Transistor current $I_{trans}(t)$ is expressed in Eq. (1):

$$I_{trans}(t) = \sum_{p=1}^{P} C_{i,p}[1 + \gamma_p V_{DS}(t)]u^p(t). \quad (1)$$

Here $u(t)$ denotes transistor input signal. $C_{i,p}$ represents static and dynamic nonlinearity characteristic of transistor. $V_{DS}(t)$ is the output voltage of transistor. Variable load impedance will cause $V_{DS}(t)$ to change, which is scaled by output conductance of transistor $\gamma_p$. Note that $\gamma_p$ is mainly determined by channel-length modulation parameter $\lambda$ in longer MOSFETs [21]. As a consequence, the nonlinearity of transistor may change with different load impedance.

## 3. Proposed on-line DPD structure

Conventional off-line DPD structure is a typical indirect learning structure [22, 23]. Its inverse model of PA requires identification after each transmission. As analyzed above, the nonlinearity of transistor changes simultaneously with load impedance. Thus an on-line DPD structure is more reliable under the variable load impedance conditions.

On-line structure exposes two challenges in comparison to off-line one [24, 25]. First one is to keep adaptive algorithm converging under variable conditions. The second is to compensate the loop delay of the system in real-time. So we designed amplitude divider and Loop Delay Estimation (LDE) respectively as showed in Fig. 1. Amplitude divider is a simple divider operation that gives the estimated amplitude gain $G_n$, which is used to pre-scale baseband signal instead of normalizing output signal of PA.

Loop delay consists of integer part as well as fractional part. As showed in Fig. 2, the latency throughout the RF components is $(\tau_n + \theta_n)$ times of sampling period. Here $\tau_n$ and $\theta_n$ represent the estimated integer and fractional LDE separately. $G_n$ denotes the estimated voltage amplitude gain of PA, which is estimated between integer and fractional LDE procedure.

The structure of integer LDE consists of delay units, multipliers and comparators, the latency index of the maximum cross-correlation [26] results is the estimation

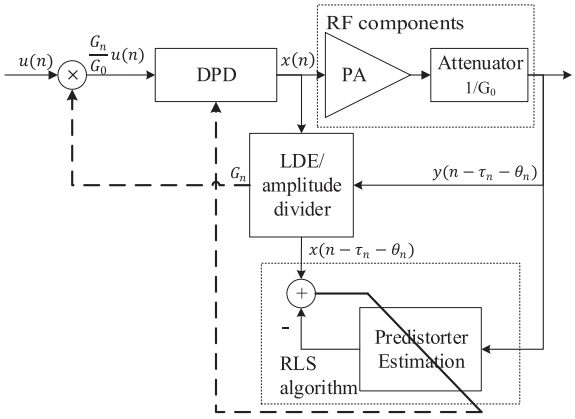


**Fig. 1.** Proposed on-line DPD structure.

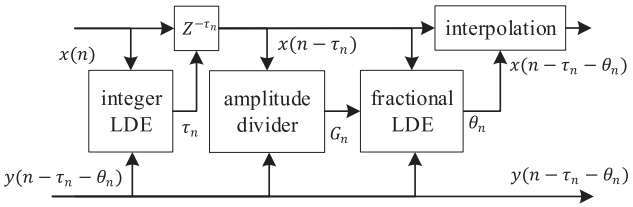


**Fig. 2.** LDE and amplitude divider structure with real-time processing.

of integer LDE. The LMS procedure of calculating fractional LDE is presented as Eq. (2), Eq. (3) and Eq. (4). $x_\theta(n)$ is the output of a three-points Lagrange interpolation filter [27] with the fractional delay of $\theta$. The symbol $\mu$ is an empirical constant represents for the speed of convergence, which is set to 0.25.

$$|x_\theta(n)| = \frac{1}{2}\theta(\theta-1)\cdot|x(n+1)| + (1+\theta)(1-\theta)\cdot|x(n)| + \frac{1}{2}\theta(\theta+1)\cdot|x(n-1)|. \quad (2)$$

$$e_n(\theta) = \frac{G_n}{G_0}|x_\theta(n)| - |y(n)|. \quad (3)$$

$$\theta_{n+1} = \theta_n - 2\mu\frac{\partial e_n(\theta)}{\partial\theta}e_n(\theta) \quad (4)$$

RLS algorithm is capable of rapid convergence yet sensitive to the amplitude of signals [28]. For the sake of stabilizing algorithm, our approach is to avoid using the ever-changing $G_n$ to achieve normalization and let RLS algorithm following the impedance mismatch status.

## 4. Experimental setup

In the experiment, we used a traditional off-line DPD structure as linearity comparison. Both structures employed the same Shichman-Hodges model [29] with intrinsic transconductance $K = 1.5\,A/V^2$, threshold voltage $V_{th} = 1\,V$, channel length modulation $\lambda = 0.05/0.5\,V^{-1}$, input capacitance $C_{iss} = 33\,pF$, output capacitance $C_{oss} = 14.3\,pF$ and reverse transfer capacitance $C_{rss} = 2.2\,pF$. The DPD was constructed using Memory Polynomial model [30] with memory depth $M = 3$ and nonlinear order $P = 9$.

Baseband signal is a 10 MHz bandwidth 64-QAM modulated complex signal with 8000 samples. The output-matching network of PA employs a simple lumped LC circuit working at 180 MHz. Load impedance of PA varies within the VSWR = 1.8 circle of smith chart by a fixed interval every 16000 samples during the simulation.

## 5. Results

Both structures compensate the nonlinearity of PA in ACPR for about 22 dB as presented in Fig. 3. But as output impedance mismatch status getting worse, the linearity of the traditional off-line DPD deteriorates. Yet the POLDPD structure retains great linearity.

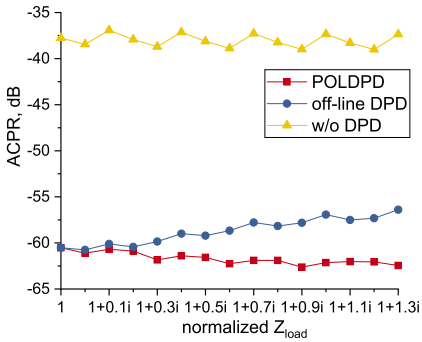


**Fig. 3.** ACPR performance comparison along with the imaginary part of load impedance increasing.

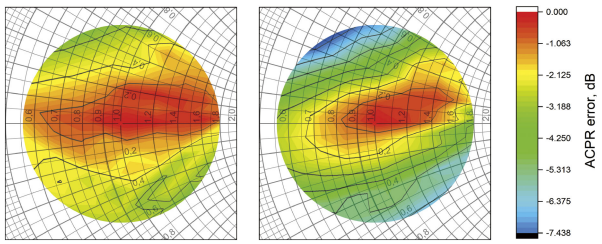


**Fig. 4.** Comparison of ACPR error between POLDPD and traditional off-line DPD with $\lambda = 0.05\,V^{-1}$ (left) and $\lambda = 0.5\,V^{-1}$ (right).

Comparison of ACPR error between POLDPD and traditional off-line DPD with two values of $\lambda$ is showed in Fig. 4. The structure of POLDPD achieved better linearity performance than off-line structure under the mismatch status. Besides, POLDPD compansates more nonlinearity under resistive impedance mismatch status than under capacitive and inductive ones with the same VSWR. Further more, the channel-length modulation parameter $\lambda$ is obviously relevant to the nonlinearity caused by load impedance mismatch.

## 6. Conclusion

An adaptive on-line digital pre-distortion structure is proposed in this letter. Simulation result reveals that this structure is far superior to the off-line structures in compensating the nonlinearity under the variable load impedance situations, where the nonlinearity is proved relevant to the output conductance of transistor. The simulation

carried out in this letter only studied one of the factors that may affect the nonlinearity under the mismatch conditions. Therefore, further studies should work on a realistic PA and the proposed structure should be pruned either.

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### References

[1] J. Reina-Tosina, *et al.*: "Behavioral modeling and predistortion of power amplifiers under sparsity hypothesis," IEEE Trans. Microw. Theory Techn. **63** (2015) 745 (DOI: 10.1109/TMTT.2014.2387852).

[2] A. E. Abdelrahman, *et al.*: "A novel weighted memory polynomial for behavioral modeling and digital predistortion of nonlinear wireless transmitters," IEEE Trans. Ind. Electron. **63** (2016) 1745 (DOI: 10.1109/TIE.2015.2494040).

[3] R. N. Braithwaite: "Digital predistortion of an RF power amplifier using a reduced Volterra series model with a memory polynomial estimator," IEEE Trans. Microw. Theory Techn. **65** (2017) 3613 (DOI: 10.1109/TMTT.2017.2729513).

[4] J. Peng, *et al.*: "Digital predistortion for power amplifier based on sparse Bayesian learning," IEEE Trans. Circuits Syst. II, Exp. Briefs **63** (2016) 828 (DOI: 10.1109/TCSII.2016.2534718).

[5] F. Mkadem, *et al.*: "Multi-band complexity-reduced generalized-memory-polynomial power-amplifier digital predistortion," IEEE Trans. Microw. Theory Techn. **64** (2016) 1763 (DOI: 10.1109/TMTT.2016.2561279).

[6] M. Li, *et al.*: "Sparsity adaptive estimation of memory polynomial based models for power amplifier behavioral modeling," IEEE Microw. Wireless Compon. Lett. **26** (2016) 370 (DOI: 10.1109/LMWC.2016.2549024).

[7] Y. Yang, *et al.*: "Optimization for error-canceling loop of the feedforward amplifier using a new system-level mathematical model," IEEE Trans. Microw. Theory Techn. **51** (2003) 475 (DOI: 10.1109/TMTT.2002.807824).

[8] M. Johansson and T. Mattsson: "Linearised high-efficiency power amplifier for PCN," Electron. Lett. **27** (1991) 762 (DOI: 10.1049/el:19910474).

[9] Y. Zhou and M. Y.-W. Chia: "A novel alternating and outphasing modulator for wireless transmitter," IEEE Trans. Microw. Theory Techn. **58** (2010) 324 (DOI: 10.1109/TMTT.2009.2037879).

[10] A. Katz, *et al.*: "The evolution of PA linearization: From classic feedforward and feedback through analog and digital predistortion," IEEE Microw. Mag. **17** (2016) 32 (DOI: 10.1109/MMM.2015.2498079).

[11] A. Birafane, *et al.*: "Analyzing LINC systems," IEEE Microw. Mag. **11** (2010) 59 (DOI: 10.1109/MMM.2010.935774).

[12] G. Hanington, *et al.*: "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," IEEE Trans. Microw. Theory Techn. **47** (1999) 1471 (DOI: 10.1109/22.780397).

[13] J. H. Chen, *et al.*: "A technique for implementing wide dynamic-range polar transmitters," IEEE Trans. Microw. Theory Techn. **58** (2010) 2368 (DOI: 10.1109/TMTT.2010.2057810).

[14] L. Zhang and F. Yan: "An improved digital predistortion in wideband wireless transmitters using an under-sampled feedback loop," IEEE Commun. Lett. **20** (2016) 910 (DOI: 10.1109/LCOMM.2016.2546257).

[15] W. Cao and Z. Anding: "A modified decomposed vector rotation-based behavioral model with efficient hardware implementation for digital predistortion of RF power amplifiers," IEEE Trans. Microw. Theory Techn. **65** (2017) 2443 (DOI: 10.1109/TMTT.2016.2640318).

[16] D. Zhou and E. D. Victor: "Novel adaptive nonlinear predistorters based on the direct learning algorithm," IEEE Trans. Signal Process. **55** (2007) 120 (DOI: 10.1109/TSP.2006.882058).

[17] B. Song, *et al.*: "Dynamic deviation memory polynomial model for digital predistortion," Electron. Lett. **53** (2017) 606 (DOI: 10.1049/el.2017.0226).

[18] E. Zenteno, *et al.*: "Output impedance mismatch effects on the linearity performance of digitally predistorted power amplifiers," IEEE Trans. Microw. Theory Techn. **63** (2015) 754 (DOI: 10.1109/TMTT.2014.2387060).

[19] O. Z. Alngar, *et al.*: "On-line predistortion algorithm for nonlinear power amplifiers with memory effects based on real-valued time-delay neural network," NRSC (2018) 338 (DOI: 10.1109/NRSC.2018.8354388).

[20] T. R. Cunha, *et al.*: "Validation and physical interpretation of the power-amplifier polar Volterra model," IEEE Trans. Microw. Theory Techn. **58** (2010) 4012 (DOI: 10.1109/TMTT.2010.2087347).

[21] W. M. Sansen: *Analog Design Essentials* (Springer Science & Business Media, New York, 2007) 0124.

[22] H. Paaso and A. Mammela: "Comparison of direct learning and indirect learning predistortion architectures," IEEE ISWCS (2008) 309 (DOI: 10.1109/ISWCS.2008.4726067).

[23] C. Eun and E. J. Powers: "A new Volterra predistorter based on the indirect learning architecture," IEEE Trans. Signal Process. **45** (1997) 223 (DOI: 10.1109/78.552219).

[24] S. Ferguson and A. Chopra: "Real-time digital predistortion for radio frequency power amplifier linearization," IEEE MTT-S IWS (2016) 1 (DOI: 10.1109/IEEE-IWS.2016.7585463).

[25] Y. Guo, *et al.*: "Simplified online coefficients updating for digital predistortion of wideband/multi-band RF power amplifiers," APMC (2015) 1 (DOI: 10.1109/APMC.2015.7411574).

[26] S. Zhu, *et al.*: "A high-efficiency loop delay estimator in digital predistortion subsystem," IEEE ChinaSIP (2014) 568 (DOI: 10.1109/ChinaSIP.2014.6889307).

[27] V. Valimaki and H. Azadeh: "Fractional delay filter design based on truncated Lagrange interpolation," IEEE Signal Process. Lett. **14** (2007) 816 (DOI: 10.1109/LSP.2007.898856).

[28] V. J. Mathews: "Adaptive polynomial filters," IEEE Signal Process. Mag. **8** (1991) 10 (DOI: 10.1109/79.127998).

[29] H. Shichman and A. H. David: "Modeling and simulation of insulated-gate field-effect transistor switching circuits," IEEE J. Solid-State Circuits **3** (1968) 285 (DOI: 10.1109/JSSC.1968.1049902).

[30] J. Kim and K. Konstantinou: "Digital predistortion of wideband signals based on power amplifier model with memory," Electron. Lett. **37** (2001) 1417 (DOI: 10.1049/el:20010940).