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LETTER

Reliable packaging of Josephson voltage standard circuit for cryocooler operation

Hirotake Yamamori[1a)], Michitaka Maruyama[2], Yasutaka Amagai[2], and Takeshi Shimazaki[2]

Abstract Reliable and easy fabricated packaging for a Josephson voltage standard circuit was proposed and the thermal stress and temperature distribution in the chip were numerically analyzed. The chip for programmable Josephson voltage standard circuits was bonded with InSn solder to a copper plate to achieve good thermal contact. Although this packaging allowed very good thermal contact, the chip sometimes broke due to thermal stress caused by a difference in the expansion coefficient between silicon and copper. Slits were thus added to the copper plate to reduce the thermal stress. The numerical analysis suggested that the slits reduce the thermal stress in the voltage standard chip, and thus reduce the risk of the chip cracking when it is cooled. The numerical analysis also suggested that the temperature increase in the chip was about 1 mK which caused a negligible reduction in the operating margin of the PJVS operation.

Keywords: cryocooler, Josephson voltage standard, PJVS, NbN, InSn solder
Classification: Superconducting electronics

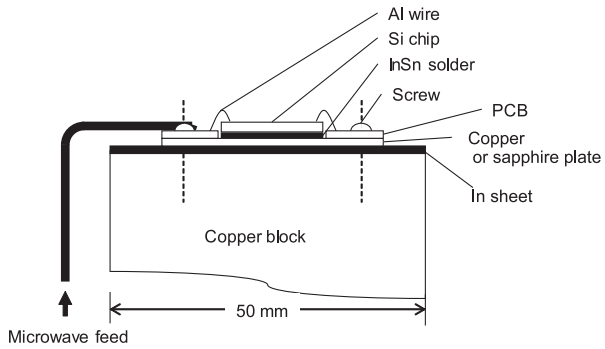

Fig. 1. Layout of sample-holding section composed of PJVS chip, printed circuit board and coaxial cable.

1. Introduction

Superconducting devices such as single flux quantum (SFQ) logic gates are being considered as significant low dissipation power devices [1, 2, 3]. An SFQ-based readout circuit has been successfully demonstrated with a 0.1 W Gifford-McMahon cryocooler [4, 5, 6]. As the magnitude of the integration becomes larger, the bias current and power dissipation are getting larger. An adiabatic quantum flux parametron (AQFP) which dissipation power is much smaller than SFQ circuit has been also proposed and has been demonstrated [7, 8].

On the other hand, a dissipation power for Josephson voltage standard circuit is much larger than SFQ circuits. A Josephson junction (JJ) array using a superconductor-normal-superconductor (SNS) junction can generate arbitrary waveforms including sine waves [9, 10]. One of the advantages of the SNS junction is a large critical current density that enables a large operating current margin for the PJVS. Because the dissipation power of the chip is high, typically 0.3 W, cryo-packaging is important for operating a PJVS chip with a cryocooler [11, 12, 13, 14, 15, 16, 17, 18].

JJ arrays are used in dc-voltage standards [19, 20, 21]. The National Institute of Advanced Industrial Science and Technology (AIST) and the National Institute of Standards and Technology (NIST) have jointly developed NbN-based digital-to-analog converters (DACs) for a programmable Josephson voltage standard (PJVS) [22, 23]. NbN-based DACs can operate at temperatures of around 10 K. The main advantage of such DACs is that they enable operation using more compact cryocoolers and compressors.

The present study proposes simple, reliable, and low-cost cryo-packaging for a PJVS chip for operation with a cryocooler.

2. Packaging for cryocooler

While varnish or silver paste are used to mount a chip with low dissipation power such as superconducting sensors and so on [24, 25], the use of them resulted in a significant temperature increase in the voltage standard chip due to large dissipation power. Thus, a silicon chip is solder-bonded to a copper substrate to achieve good thermal contact between the chip and a cryocooler. InSn solder is used to mount the chip on the copper substrate. Ti/Pd/Au (5 nm/200 nm/100 nm) were deposited on the back of the chip for adhesion.

Fig. 1 shows a schematic diagram of the cryo-packaging. The copper substrate is mounted on the cold-head of the cryocooler with screws and the PJVS chip is cooled at 10 K. The chip is connected to a printed circuit board with aluminum wires, and a microwave current is applied over a co-axial cable. The Aluminum wires and a co-axial cable are thermally anchored to the 4 K stage of the cryocooler.

[1]The National Institute of Advanced Industrial Science and Technology, Nanoelectronics Research Institute, 1–1–1 Umezono, Tsukuba 305–8568, Japan
[2]The National Institute of Advanced Industrial Science and Technology, National Metrology Institute of Japan, 1–1–1 Umezono, Tsukuba 305–8563, Japan
a) h.yamamori@aist.go.jp

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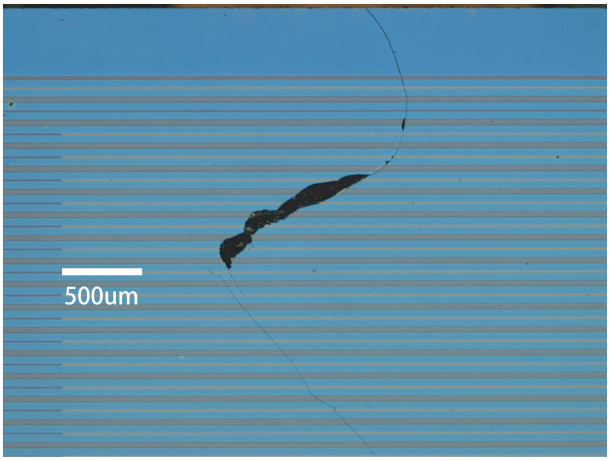

Fig. 2. Photograph of crack on PJVS chip solder bonded to a coper substrate due to thermal stress.

Although the PJVS chip was successfully cooled without temperature increase, there were some reliability problems for the chip in the form of surface cracks as shown in Fig. 2, due to a difference in the coefficient of thermal expansion (CTE) α between the chip and the copper substrate.

3. Numerical simulation of thermal stress

The thermal stress in the PJVS chip soldered to a substrate was numerically analyzed using the finite element method (FEM). A silicon chip was solder-bonded to a copper substrate with InSn (52.0In/48.0Sn), whose melting point is 391 K. Thus, the temperature difference is $\Delta T = 381$ K when the chip is cooled to 10 K. The displacement is given by $\alpha\Delta T$, and the thermal stress $\sigma = -E\alpha\Delta T$, where E is Young's modulus. The size of the silicon chip is 15 mm × 15 mm × 0.6 mm. The thickness of the InSn was measured by cutting the chip and substrate [26]. Although there were variation of the thickness, typical value of 0.01 mm was used for the calculation. The size of the copper substrate is 40 mm × 30 mm × 0.8 mm.

Fig. 3(a) and (b) show calculated results for silicon chip bonded with InSn to (a) the copper substrate and (b) sapphire substrate. Displacement is magnified tenfold. While the thermal stress for the chip bonded to a copper substrate is about 700 MPa, that for the chip bonded to a sapphire substrate is about 70 MPa. As shown in Table I, because the CTE for sapphire is much smaller than copper and close to silicon, the thermal stress for silicon chip solder-bonded to the sapphire substrate is much smaller than that solder-bonded to the copper substrate.

One possible way to avoid cracks in the silicon chip is to use a sapphire substrate instead of a copper substrate because the coefficients of thermal expansion for silicon and sapphire are similar [27]. A sapphire substrate is used for the voltage primary standard at the National Metrology Institute of Japan [28]. However, there are some disadvantages to using sapphire, such as the requirement of an additional process for sputter-depositing gold film on the sapphire substrate for InSn solder bonding, and the high cost of sapphire, both of which increase packaging cost. In addition, the material is very hard to shape, e.g., holes for screws.

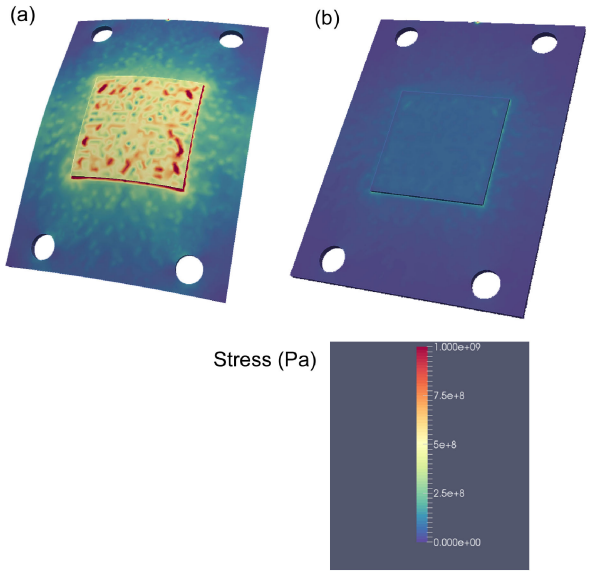

Fig. 3. Calculated thermal stress for silicon chip bonded with InSn to (a) the copper substrate and (b) sapphire substrate. Displacement is magnified tenfold.

Table I. Approximate values used for the stress calculation.

	Si	Cu	Sapphire	InSn
Young's modulus × 10^{11} N/m^2	1.30	1.42	4.70	0.20
CTE $\alpha \times 10^{-6}$ K^{-1}	2.40	16.8	4.00	23.0

Therefore, this study proposes another easy and low-cost packaging using a copper substrate with slits [29]. We numerically demonstrate that the slits in the copper substrate reduce the thermal stress in the silicon chip solder-bonded to the copper substrate, and that they may reduce the risk of cracking due to such thermal stress.

Table I shows the approximate values used for FEM calculation [30, 31, 32, 33, 34]. For simplicity, the temperature dependence of Young's modulus and that of the coefficient of thermal expansion α are not taken into account; the values at room temperature are used for the calculation. The Young's modulus in the silicon [100] is used; the anisotropy of the crystal is not taken into account. Although the calculated values are approximate, they enable qualitative discussion based on a comparison of results obtained with and without slits on the copper substrate.

Fig. 4(a) shows the numerically calculated displacement and thermal stress for a silicon chip bonded to a copper substrate without any slits. The displacement is magnified tenfold. The thermal stress is about 700 MPa. The displacement caused by the tensile thermal stress may break the silicon chip. Fig. 4(b) shows smaller displacement and thermal stress for the silicon chip bonded to the copper substrate with slits. The stress is reduced to about 350 MPa. This suggests that the slits on the copper substrate can reduce the thermal stress by half, namely, the yield may be expected to double. Because it is unclear whether the reduction in thermal stress is sufficient to improve the reliability for cryo-packaging, experiments

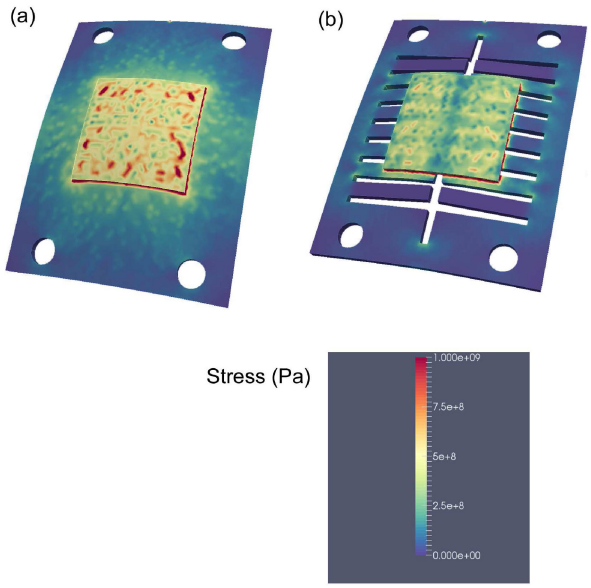

Fig. 4. Calculated thermal stress for silicon chip bonded with InSn to the copper substrate (a) without and (b) with slits. Displacement is magnified tenfold.

Table II. Approximate values used for the temperature calculation.

	Si	Cu	Sapphire	InSn
Thermal conductivity W/mK	2600	4343	3000	8
Thickness mm	0.6	0.8	1.0	0.01

should be conducted. The number and size of the slits should be also optimized.

4. Numerical simulation of temperature

It was confirmed that the slits do not cause a significant temperature increase or a non-uniformity temperature distribution in the silicon chip. Table II shows the parameters used for the temperature calculation. The temperature distribution was calculated when power of 0.3 W was applied to the silicon chip and the bottom surface of the copper substrate was fixed at 10.0 K.

Fig. 5(a) shows the calculated temperature of the silicon chip bonded to the copper substrate without any slits. The temperature of the surface of the silicon chip is 10.0019 K. Fig. 5(b) shows the temperature of the silicon chip bonded to the copper substrate with slits. The temperature is 10.0029 ± 0.0003 K, i.e., the temperature increase is about 1 mK and the non-uniformity at the chip surface is about ± 0.3 mK. Although the temperature and non-uniformity for the package with slits are slightly larger than those for the package without slits, they are nearly negligible compared to the temperature oscillation of about 100 mK caused by a Gifford-McMahon cryocooler [14].

5. Experimental

The operating current margin of the PJVS chip mounted on the copper substrate with slits is under investigation to get statistical data to confirm the advantages of the proposed packaging, while the temperature distribution in the chip

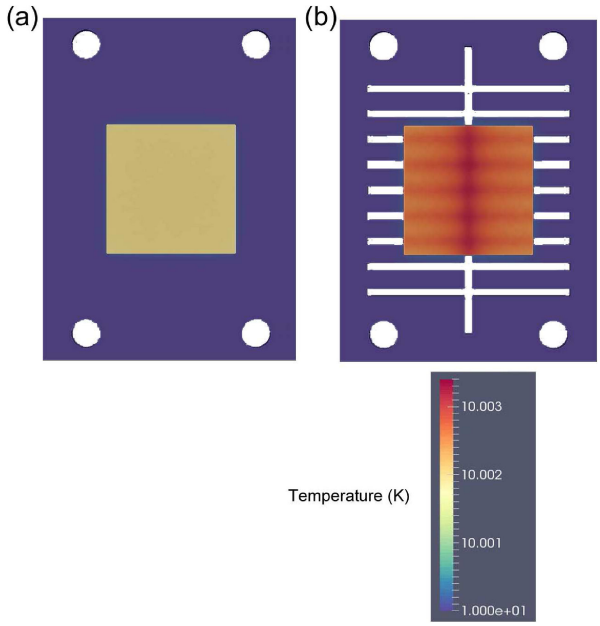

Fig. 5. Calculated temperature distribution of chips with power of 0.3 W on copper substrate (a) without and (b) with slits. The bottom surfaces of the copper substrates was fixed at 10 K.

[35] cannot be directly measured. As reported previously [26], there is a run-to-run variation in the area of the void between the silicon chip and the copper substrate; this void may cause a temperature increase and decrease the operating current margin for the PJVS.

In this calculation, we ignored the void between the chip and copper substrate. Copper substrates without slits did not always brake the chip. We suppose that the risk of breaking the chip depends on the area of void under the chip. The simulation suggested that the chip without any void could result in higher risk of breaking the chip. While we tried to reduce the area of void to get better thermal contact, the area of void could not be controlled in a conventional way.

Fig. 6 shows a photograph of the back side of the PJVS package. The slits may allow excess InSn solder and vaporized flux to easily escape, resulting in thinner solder and a smaller void area, and thus better thermal contact. This also may reduce run-to-run variations of the thermal contact of the packaging.

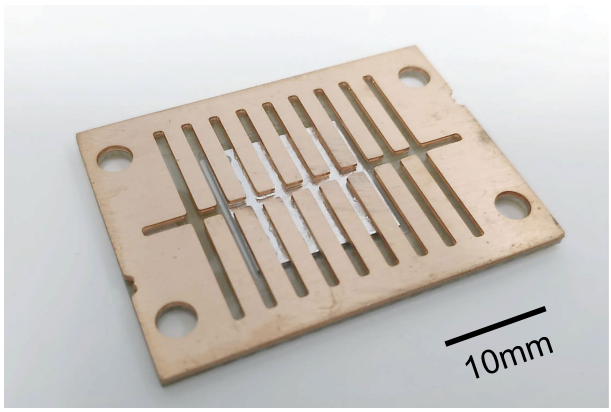

Fig. 6. Photograph of back side of copper-substrate whose size is 40 mm × 30 mm.

6. Conclusion

A silicon chip solder-bonded to a copper substrate sometimes cracked when it was cooled with a cryocooler to 10 K. Reliable and easy packaging for a Josephson voltage standard circuit are proposed. An FEM analysis suggested that slits in the copper substrate reduce the thermal stress to half without significantly increasing the temperature or changing the temperature distribution in the chip. This packaging method is easy, reliable and low-cost for a Josephson voltage standard with a cryocooler.

Acknowledgments

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