

A novel tunable true-time delay line/phase shifter based on distributed Schottky structure

Tian-yu Pen^{1,2}, Bing Huang^{1,2}, Shu-Na Wang¹, Xiao-Wei Sun¹, and Ling-Yun Li^{1a)}

Abstract True time delay lines and phase shifters are widely used in RF timed/phased array systems. Conventional delay lines and phase shifters often associate with reflection type circuits or distributed (periodically loaded) transmission lines. In this paper, we propose a new type of distributed circuit which composed of uniform transmission lines built on integrated Schottky active layer. A bi-functional chip is designed based on the new distributed structure. An Archimedean spiral topology is adopted to reduce the chip area. Theoretical analysis of the design method and circuit parameters is performed and a miniaturized prototype is implemented with p-HEMT technology to validate the design theory. Measurement results shows that this chip could work as either an areaefficient true-time delay line or a low-voltage phase shifter over the bandwidth 11-15 GHz. As an area-efficient true-time delay line, this chip provides 82.1 ps delay time per square millimeter when the biasing voltage fixed at -1.4 V. As a low-voltage phase shifter, this chip provides 26.43° phase shift per volt when the biasing voltage sweeps form 0 V to -1.4 V. Keywords: distributed Schottky, delay line, phase shifter, p-HEMT Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

True-time delay lines (TTDL) and phase shifters are widely used in RF and microwave applications, especially in phased-array antennas and radars [1, 2, 3, 4, 5, 6, 7, 8]. A simple transmission line could work as a fixed time delay line. To achieve a large delay time on a compact chip size, several technics have been proposed. MEMS based [9, 10, 11, 12] and optical [13, 14, 15] TTDLs could offer favorable performance. However, they often need complicate process and are not compatible with standard IC technologies. Composite right/left-handed transmission lines (CRLTLs) [16, 17, 18, 19], using tunable elements periodically loading a transmission line, can be fabricated with a standard IC technology, but suffers from a narrow bandwidth.

Periodically loaded CPW/CPS transmission lines are also adopted to design continuous phase shifters, which is

¹Key Laboratory of Terahertz Solid-state Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 865 Changning Road Shanghai, China

²Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China a) lilingyun@mail.sim.ac.cn

DOI: 10.1587/elex.16.20190231 Received April 8, 2019 Accepted April 10, 2019 Publicized April 26, 2019 Copyedited June 10, 2019

often called distributed structures [20, 21, 22]. Other technics for continuous phase shifter designing include ferrite material based [23, 24, 25], MEMS based [26, 27, 28, 29] and substrate integrated waveguide (SIW) based [30, 31, 32] circuits. These technics suffer from complicate processes, special materials or bulky size [25, 28, 30]. Furthermore, most existing phase shifter acquire tens of volts biasing voltage [20, 22, 27, 30].

In this paper, we propose a new type of distributed circuit structure composed of transmission lines built an integrated Schottky active layer. A bi-functional chip is designed and fabricated based on the new distributed structure, which could work as either a true-time delay line or a phase shifter. Different from existing coplanar waveguide (CPW) or coplanar strip (CPS) based distributed circuit [20, 21, 22], this design is based on micro-stripe line, which could effectively reduce the chip area and complexity. Furthermore, the fabricated chip shows ultralow a bias voltage comparing with other phase shifter works.

2. Analysis and design

2.1 Theoretical analysis

The proposed distributed structure consists of a transmission line built on an integrated Schottky active layer. Fig. 1(a) and Fig. 1(b) shows the detailed structure of the proposed circuit.



Fig. 1. (a) Cross-section of the proposed distributed structure. (b) 3D structure of the new structure. (c) Equivalent circuit of the new structure.

Fig. 1(c) shows the equivalent circuit of a Schottky layer based transmission line where C_j and G_j represent the junction capacitance and conductance per unit length of the Schottky layer respectively [33]. When a biasing voltage is applied, the electro-conductivity of the active layer would change, resulting in a change of signal propagating features. The group delay and phase shift depend on the propagation constant:

$$\beta = \omega \cdot \sqrt{L \cdot C} \tag{1}$$

where C represents the total equivalent capacitance to the ground. The transmission time and phase shift are given by:

$$\tau = \frac{l}{\omega/\beta} = l \cdot \sqrt{L \cdot C} \tag{2}$$

$$\Delta \varphi = \omega \cdot \tau = \omega \cdot l \cdot \sqrt{L \cdot C} \tag{3}$$

When the controlling voltage changes, equivalent capacitance C changes, resulting in a tunable delay time and phase shift:

$$\tau(V) = \frac{l}{\omega/\beta(V)} = l \cdot \sqrt{L \cdot C(V)}$$
(4)

$$\Delta \varphi(V) = \omega \cdot \tau(V) = \omega \cdot l \cdot \sqrt{L \cdot C(V)}$$
(5)

L and C also define the characteristic impedance of the transmission line by the equation:

$$Z_0 = \sqrt{\frac{L}{C(V)}} \tag{6}$$

2.2 Circuit parameter simulation

The circuit parameters are designed for optimal Z_0 and tunable phase range. In our design, the thickness of dielectric is determined by the fabricating technology. Therefore, the top metal width is the key design parameter. The relation between Z_0 and top metal width under various biasing voltage are simulated and plotted in Fig. 2(a), which indicates that Z_0 is mainly influenced by the top metal width rather than the biasing voltage.

Fig. 2(b) shows the phase shift under different top metal width and controlling voltage at 13 GHz, which reveals that top metal width has little influence on the tunable range of phase.

2.3 Circuit design procedure

Most IC technologies acquires anode layer being enclosed by metal layer. Balancing this limit and circuit performance, the width of the anode is designed equal to the width of the top metal.

In a standard IC technology, the Schottky layer is often right beneath the first metal layer, usually called metal-1. For a multilayered metal technology, there are several dielectric layers between neighboring metal layers. To fabricate the new distributed circuit, eliminate all the metal layers except the top one of them. The dielectric layers could constitute the substrate of the tunable delay line and the top metal could work as the metal layer of it.



Fig. 2. Simulation results of Z0 (a) and phase shift @13 GHz (b) under different top metal width and biasing voltage

3. Manufacturing

A miniaturized prototype is implemented with p-HEMT technology, which has two metal layers. The first metal layer is eliminated and the dielectric embedded between these two metal layers works as the substrate layer. The thickness of the dielectric layer is fixed at 1.6 μ m, and the minimum width of the metal layers is 7 μ m. Fig. 3 shows the cross section of the fabricated circuit.



Fig. 3. Cross section of the implemented tunable delay line

As shown in Fig. 2(a), for 50 Ω Z₀, the top metal width is less than 5 µm, which is smaller than minimum metal width. Accordingly, the minimum metal width 7 µm is adopted hence the characteristic impedance is about 37.5 Ω . Although, because the limit of the adopted technology, the thickness of the substrate is much smaller than common MMIC circuits, the transmission features are proved acceptable by EM simulations. Fig. 4 shows the photograph of the fabricated chip. Two central symmetric Archimedean spiral are connected forming a two-arm spiral, which effectively reduced the chip area [34]. The spaces between the adjacent cures are $28 \,\mu\text{m}$ balancing the chip size and the cross talk. A backup DC bias pad is added for reliability.



Fig. 4. Photograph of the fabricated chip. ① and ② are discontinuous points formed by crossing the border of the active layer.

4. Measurement

4.1 Insertion loss and return loss

The fabricated chip is packaged for measurements utilizing an Agilent network analyzer N5245A. The effect of the packaging is de-embedded from the measured results. The DC bias consume zero current, therefore the circuit is a passive component.

The measured insertion loss and return loss are plotted in Fig. 5 and Fig. 6. The ideal matching frequency drifts 1 GHz higher than the simulation result. Both the insertion loss and the return loss deteriorate when the frequency get lower. At the center frequency 13 GHz, the measured insertion loss is -8 ± 2 dB, and the return loss is -8.7 dB.



Fig. 5. Measurement of the insertion loss.

4.2 Area-efficient passive true-time delay line

Fig. 7 shows the group delay under different biasing voltage over 11–15 GHz. There are two main reasons that caused the differences between simulated and measured results. Firstly, the limited top metal width acquires a taper component, which has a certain bandwidth, applied to connect the input/output pads. Secondly, between the in-



Fig. 6. Measurement of the return loss.

put/output pads and the spiral, the border of the active layer brings two discontinuous points (shown in Fig. 4), which formed a series structure of transmission lines with different Z_0 that causes the variation of group delay over the target frequency range.

The average delay time is 300 ps with a tunable range of 8% when the control voltage varies from 0 V to 1.4 V. The maximum delay time is 325 ps when the control voltage is -1.4 V and the maximum delay time per chip area is 82.1 ps/mm².



Fig. 7. Measurement result of group delay.

4.3 Low voltage phase shifter

Fig. 8 shows the measured phase shift and calculated capacitance ratio over 11-15 GHz. The maximum phase shift is 35 degrees when biasing voltage varies from 0 V to 1.4 V. The phase shift per bias voltage is 26.4 deg/V. The capacitance ratio varies from 1.08 to 1.12 over the working frequency band. A comparison with other passive phase shifter works are shown in Table I.



Fig. 8. Measured phase shift and calculated capacitance ratio

| | [30] | [22] | [20] | [27] | [21] | This work |
|---------------------------------------|-------|-------|------|------|------|--------------|
| Max phase shift (deg) | 30 | 285 | 240 | 100 | 15 | 37 |
| Biasing voltage (V) | 30 | 20 | 10 | 16 | 3 | 1.4 |
| Chip area | Large | 9.28 | N.A. | N.A. | 0.35 | 3.96 |
| Technology | SIW | BCTZ | GaAs | MEMS | N.A. | GaAs |
| Phase shift per voltage (deg/V) | 1 | 14.25 | 24 | 6.25 | 5 | 26.43 |

 Table I.
 Comparison with other phase shifter works

5. Conclusion

This paper presents a new distributed Schottky structure. A bi-functional circuit, which could work as either a true time delay line or a phase shifter, is designed and fabricated based on this new structure. As a true time delay line, this circuit shows a large delay time per area of 82.1 ps/mm². As a phase shifter, this circuit has an ultra-low biasing voltage, which leads to a large phase shift per bias voltage of 26.43 deg/V. The design parameters of the circuit are not ideal for the limits of the fabricating technology. To achieve better insertion and return loss performance, a technology with thicker dielectrics or larger relative dielectric constant is preferred.

Acknowledgments

This work is supported by Nature Science Foundation of China under contracts No. 61671439 and No. 61731021.

References

- Y. Guo, *et al.*: "A true-time-delay transmit/receive module for Xband subarray phased arrays," IEICE Electron. Express 14 (2017) 20171039 (DOI: 10.1587/elex.14.20171039).
- [2] A. Ulusoy, *et al.*: "A tunable differential all-pass filter for UWB true time delay and phase shift applications," IEEE Microw. Compon. Lett. **21** (2011) 462 (DOI: 10.1109/LMWC.2011. 2162613).
- [3] M. Kim: "A stepped-impedance true time delay line using GaAs MMIC technology," IEICE Electron. Express 13 (2016) 20160463 (DOI: 10.1587/elex.13.20160463).
- [4] H.-Y. Li, *et al.*: "Broadband analog phase shifter based on multistage all-pass networks," IEICE Electron. Express **10** (2013) 20130491 (DOI: 10.1587/elex.10.20130491).
- [5] A. Asoodeh and M. Atarodi: "A 6-bit active digital phase shifter," IEICE Electron. Express 8 (2011) 121 (DOI: 10.1587/elex.8.121).
- [6] M. Wang, et al.: "A 6-bit 38 GHz SiGe BiCMOS phase shifter for 5G phased array communications," IEICE Electron. Express 14 (2017) 20170451 (DOI: 10.1587/elex.14.20170451).
- [7] M. Duan and J. Ma: "Wide range and high resolution true time delay unit for phased array antenna," 2018 Asia Communications and Photonics Conference (ACP) (2018) (DOI: 10.1109/ACP. 2018.8596111).
- [8] S. Park and S. Jeon: "A 15–40 GHz CMOS true-time delay circuit for UWB multi-antenna systems," IEEE Microw. Compon. Lett. 23 (2013) 149 (DOI: 10.1109/LMWC.2013.2244872).
- [9] Y. Liang, et al.: "MEMS based true time delay technology for phased antenna array systems," 2007 Asia-Pacific Microwave Conference (2007) (DOI: 10.1109/APMC.2007.4554725).

- [10] J. Perruisseau-Carrier, *et al.*: "Modeling of periodic distributed MEMS-application to the design of variable true-time delay lines," IEEE Trans. Microw. Theory Techn. **54** (2006) 383 (DOI: 10.1109/ TMTT.2005.860297).
- [11] J. Lin: "A 5-bit RF MEMS switch time delay line shifter," 2016 International Symposium on Antennas and Propagation (ISAP) (2016).
- [12] J. Perruisseau-Carrier, et al.: "Design of enhanced multi-bit distributed MEMS variable true-time delay lines," Research in Microelectronics and Electronics, 2005 PhD (2005) (DOI: 10.1109/ RME.2005.1543036).
- [13] B. Jung, *et al.*: "Optical true time-delay for two-dimensional X-band phased array antennas," IEEE Photon. Technol. Lett. **19** (2007) 877 (DOI: 10.1109/LPT.2007.897530).
- [14] J.-D. Shin, *et al.*: "Optical true time-delay feeder for X-band phased array antennas composed of 2/spl times/2 optical MEMS switches and fiber delay lines," IEEE Photon. Technol. Lett. 16 (2004) 1364 (DOI: 10.1109/LPT.2004.826083).
- [15] J.-D. Shin, et al.: "A 4-bit optical-true time-delay for 10-GHz phased array antennas using optical MEMS switches and fiberoptic delay lines," 17th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 2004 (LEOS 2004) (2004) (DOI: 10.1109/ LEOS.2004.1363217).
- [16] J. Zhang, et al.: "A compact and UWB time-delay line inspired by CRLH TL unit cell," TENCON 2010 - 2010 IEEE Region 10 Conference (2010) (DOI: 10.1109/TENCON.2010.5686567).
- [17] S. Abielmona, *et al.*: "Compressive receiver using a CRLH-based dispersive delay line for analog signal processing," IEEE Trans. Microw. Theory Techn. **57** (2009) 2617 (DOI: 10.1109/TMTT. 2009.2031927).
- [18] S. Abielmona, *et al.*: "Experimental demonstration and characterization of a tunable CRLH delay line system for impulse/continuous wave," IEEE Microw. Compon. Lett. **17** (2007) 864 (DOI: 10.1109/LMWC.2007.910492).
- [19] J. Zhang, et al.: "A wideband time-delay line inspired by CRLH TL unit cell," The 2010 International Conference on Advanced Technologies for Communications (2010) (DOI: 10.1109/ATC. 2010.5672734).
- [20] A. S. Nagra and R. A. York: "Distributed analog phase shifters with low insertion loss," IEEE Trans. Microw. Theory Techn. 47 (1999) 1705 (DOI: 10.1109/22.788612).
- [21] H.-T. Kim, et al.: "Millimetre-wave CPS distributed analogue MMIC phase shifter," Electron. Lett. 39 (2003) 1661 (DOI: 10. 1049/el:20031060).
- [22] D. Mercier, *et al.*: "X band distributed phase shifter based on solgel BCTZ varactors," 2017 47th European Microwave Conference (EuMC) (2017) (DOI: 10.23919/EuMC.2017.8231072).
- [23] S. I. M. Sheikh, *et al.*: "Analog/digital ferrite phase shifter for phased array antennas," IEEE Antennas Wireless Propag. Lett. 9 (2010) 319 (DOI: 10.1109/LAWP.2010.2048190).
- [24] W. W. G. Hui, et al.: "Low-cost microstrip-line-based ferrite phase shifter design for phased array antenna applications," IEEE Antennas Wireless Propag. Lett. 6 (2007) 86 (DOI: 10.1109/LAWP. 2007.893068).
- [25] S. Kagita, *et al.*: "Modeling of LTCC-ferrite tunable inductors and development of an L-band phase shifter," IEEE Trans. Magn. **51** (2015) 1 (DOI: 10.1109/TMAG.2015.2442222).
- [26] G. Yang, et al.: "Design and modeling of 4-bit MEMS switchedline phase shifter," 2011 International Conference on Electronics, Communications and Control (ICECC) (2011) (DOI: 10.1109/ ICECC.2011.6066312).
- [27] G. McFeetors and M. Okoniewski: "Distributed MEMS analog phase shifter with enhanced tuning," IEEE Microw. Compon. Lett. 16 (2006) 34 (DOI: 10.1109/LMWC.2005.861350).
- [28] J. Lampen, et al.: "Low-loss, MEMS based, broadband phase shifters," 2010 IEEE International Symposium on Phased Array Systems and Technology (2010) (DOI: 10.1109/ARRAY.2010. 5613368).
- [29] M. Bakri-Kassem, et al.: "Novel millimeter-wave slow-wave phase shifter using MEMS technology," 2011 41st European Microwave Conference (2011) (DOI: 10.23919/EuMC.2011.6101709).

- [30] H. Peng, et al.: "Continuously tunable SIW phase shifter based on the buried varactors," IEICE Electron. Express 12 (2015) 20150165 (DOI: 10.1587/elex.12.20150165).
- [31] F. A. Ghaffar and A. Shamim: "A partially magnetized ferrite LTCC-based SIW phase shifter for phased array applications," IEEE Trans. Magn. **51** (2015) 1 (DOI: 10.1109/TMAG.2015. 2404303).
- [32] Y. Ding and K. Wu: "SIW varactor-tuned phase shifter and phase modulator," 2012 IEEE/MTT-S International Microwave Symposium Digest (2012) (DOI: 10.1109/MWSYM.2012.6259459).
- [33] J. C. Mou, et al.: "Design of a compact Ka-band balanced mixer based on a novel wide-band equivalent circuit of the Schottky diode," J. Infrared Millim. Terahertz Waves 32 (2011) 466 (DOI: 10.1007/s10762-011-9777-6).