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LETTER

A novel sense amplifier to mitigate the impact of NBTI and PVT variations for STT-MRAM

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Abstract STT-MRAM has been considered to be one of the most promising non-volatile memory candidates due its non-volatility, high speed, and unlimited endurance etc. However, with technology scaling down, STT-MRAM suffers from high sensitivity to process voltage and temperature (PVT) variations. Additionally, the negative bias temperature instability (NBTI) effect has become an important factor affecting the life of the pMOSFETs used in an STT-MRAM sense amplifier. Therefore, designing a more reliable sense amplifier has become a critical challenge. In this paper, a novel architecture for a sense amplifier is proposed, which includes switching transistors to decrease the NBTI effect on the pMOS device, and a balanced transistor to decrease the sensitivity of the sense amplifier to process variations.

Keywords: STT-MRAM, sense amplifier, NBTI, high reliability
Classification: Electron devices, circuits and modules

1. Introduction

Spin transfer torque-magnetic random access memory (STT-MRAM) is one of the most promising candidates for universal memory, thanks to its non-volatility, a high read-write speed, unlimited endurance and compatibility with CMOS process technology [1, 2, 3, 4]. An STT-MRAM storage element typically consists of one magnetic tunnel junction (MTJ) and one access transistor driven by a word line (WL), as shown in Fig. 1(a) [5, 6]. A typical MTJ is composed of two ferromagnetic (FM) layers (e.g., CoFeB) and one oxide barrier layer (e.g., MgO) [5]. The magnetization direction of one ferromagnetic layer is pinned, while that of the other ferromagnetic layer is free to take two directions. An MTJ acts as a low resistance (R_P) or a high resistance (R_{AP}) depending on whether the relative magnetization of the two ferromagnetic layers is parallel (P) or anti-parallel (AP). The resistance difference between R_{AP} and R_P can be characterized by the tunnel magneto resistance (TMR = $(R_{AP} - R_P)/R_P$). The R_P and R_{AP} resistances give MTJ the ability to be used as non-volatile binary storage [2, 6].

By using spin transfer torque (STT) mechanism, a low bi-directional switching current (I_{swich}) flowing through the MTJ can switch the magnetization direction of the free layer either parallel or anti-parallel to that of the pinned layer, as shown in Fig. 1(a). Here, I_{swich} is larger than the threshold switching current (I_c).

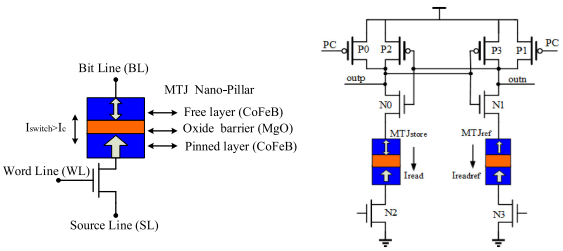

Fig. 1. STT-MRAM sensing Structure (a) storage element with 1 MTJ and 1 access transistor. (b) pre-charge sense amplifier proposed by [5]

During a sensing operation, in order to sense the MTJ binary state, the resistance of MTJ_{store} is compared against that of a reference resistance [5]. Fig. 1(b) shows a typical pre-charge sense amplifier (PCSA) [5, 6, 7, 8], in which the reference resistance is set to the midpoint of the sum of R_P and R_{AP}, i.e., $0.5(R_P + R_{AP})$. As shown in Fig. 1(b), by using the sense amplifier, the sensing operation uses a low current (I_{read}) to detect the MTJ resistance difference between R_{AP} and R_P and then compares I_{read} with the current ($I_{readref}$) passing through the reference cell [5].

However, there are some critical issues in sensing reliability [5, 6]. For thermal activation, the sensing current (I_{read}) flowing through the MTJ can switch the MTJ state described by Eq. (1)–(2) [5], thereby inducing sensing failures.

$$P_r = 1 - \exp(-Duration/\tau_1) \tag{1}$$

$$\tau_1 = \tau_0 \exp\left(\frac{\Delta E}{k_B T}\left(1 - \frac{I_{read}}{I_c}\right)\right) \tag{2}$$

where P_r is the switching probability, *Duration* is the sense-current pulse duration, $\tau_0 \approx 1$ ns is an attempt period, ΔE is the thermal activation energy which determines the thermal stability of the MTJ, and I_{read} is the sensing current.

In recent years, many STT-MRAM circuits have been prototyped on technology scale down nodes [7, 8, 9, 10]. However, with technology scaling down, there are some critical issues associated with the sensing circuits of STT-MRAM because the combination of STT with MTJ suffers from both intrinsic stochastic switching behaviors and a high sensitivity to process variations [11, 12, 13, 14, 15, 16]. In addition, the effect of a negative bias temperature instability (NBTI) on a pMOS device in the sensing circuits of RAM becomes an important factor affecting the speed of a pMOS device and the mismatch of the sensing circuits [17, 18].

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In this paper, based on the pre-charge sense structures, a novel architecture for a sense amplifier is proposed, which includes a switching transistors scheme to decrease the NBTI effect on the pMOS device, as well as a balanced transistor to decrease the sensitivity of the sense amplifier to process variations. The simulation results compared with conventional sensing circuits validate the proposed structure of the sense amplifier.

2. Effect of NBTI and process variations on the sensing circuit

2.1 Effect of NBTI on the sensing circuit

With the continuous shrinking of CMOS process technology, the effect of negative bias temperature instability (NBTI) on a pMOS transistor has become an important factor affecting both the life of a pMOS transistor and the mismatch of pMOS transistors [19, 20, 21].

Logic "0" applied at the gate terminal of a pMOS transistor causes it to be stressed by a negative-bias. As a result, interface traps at the Si/SiO2 interface and positive oxide charge in metal-oxide-silicon (MOS) are generated [21], then NBTI occurs. Consequently, a pMOS transistor will degrade with time for the NBTI effect, which results in the threshold voltage (V_{th}) of the pMOS increasing [20, 21, 22]. The V_{th} variations will affect the speed and the channel resistance (R_{ds}) of a pMOS transistor [20]. STT-MRAM consists of memory cells, write driving, sense amplifier, address decoder, control circuits, etc. These circuits include many pMOS transistors. In this work, only part of the pMOS transistors in a sense amplifier are analyzed, because the sense amplifier is a critical comment, which ensures correct sensing of the MTJ state.

It is worth noting that pre-charge pMOS transistor is used as a switch in PCSA [23]. When pre-charge current is infinitely approaching zero, there is a small voltage difference between the source terminal and the drain terminal of the switch MOSFET [23]. Therefore, with an improvement in the reading speed and the continuous shrinking of CMOS process technology, the voltage difference between outp node and outn node can be enlarged for the NBTI effect at the beginning of the discharge [23]. Furthermore, the temperature and stress time will accelerate this degradation [22]. Consequently, the mismatch between the data branch and reference branch is increased, eventually leading to sense failure. Therefore, it is necessary to explore some solutions to mitigate the NBTI effect.

In reference [17], in order to modulate V_{th}, an appropriate body bias is used by controlling the source-to-body voltage (V_{SB}) of a pMOS transistor. A forward body bias ($V_{\mathrm{SB}} > 0$) can recover the V_{th} increased by NBTI, and then increase the speed of the pMOS transistor. Thereafter, the impact of NBTI degradation can be mitigated. However, this technique requires using complicated monitoring circuits to determine the V_{th} deviation and generating circuits to generate an appropriate body bias voltage, which results in a large area overhead.

It is worth noting that some of the interface traps resulting from NBTI can be eliminated by removing logic "0" applied at the gate terminal of the pMOS transistor. Then, the V_{th} shift caused by the NBTI can be recovered, and the pMOS transistor is put into recovery mode [22]. According to several NBTI models proposed in references [24, 25, 26, 27], the V_{th} degradation is highly dependent on stress voltage (V_{SG}) and stress time (t). A NBTI model based on trapping/de-trapping theory under two voltages cycle to cycle are described by Eq. (3) [26]

$$\begin{aligned}
&\Delta V_{th}(t+t_0) = \Delta 1 + \Delta 2 \\
&\Delta 1 = \phi(\mathrm{A} + \mathrm{B}\log(1+\mathrm{C}t)) \\
&\Delta 2 = \Delta V_{th}(t_0)\left(1 - \frac{k + \log(1+\mathrm{C}t)}{k + \log(1+\mathrm{C}(t+t_0))}\right) \\
&\phi = \phi_0 \exp\left(\frac{\beta V_{SG}}{T_{ox}\cdot KT}\right)\exp\left(-\frac{E_0}{KT}\right)
\end{aligned} \tag{3}$$

where t_0 is the initial time of the stress voltage ($\mathrm{V_{SG}}$) applied, t is the stress time of the $\mathrm{V_{SG}}$ kept, $\mathrm{T_{ox}}$ is the oxide thickness of PMOS, K is Boltzmann constant, T is Kelvin temperature, A, B, C, k, φ_0, β and E0 are model constants related to the process [26].

This NBTI model indicates the variation of $\mathrm{V_{th}}$ (ΔV_{th}) is partially recoverable by reducing the stress voltage bias and the stress time on PMOS [26]. Therefore, the main solutions of mitigating the NBTI is to reduce the stress applied on the pMOS transistor and to enhance the recovery process. Controlling the VDD and reducing the stress time are often used to reduce the stress.

2.2 Effect of process variations on sensing circuit

In STT-MRAM, both the memory bit cells and the sensing circuits include metal-oxide-semiconductor-field-effect-transistors (MOSFETs) [9, 11]. With technology scaling, MOSFETs suffer from process, voltage and temperature (PVT) variations. PVT variations lead to MOSFETs parameter variations [28], such as a variation in the channel length (L), channel width (W), oxide thickness (t_{ox}), etc. These parameter variations can lead to a reduction of the circuit reliability and to more device mismatch in the sensing circuit. For a MOSFET, the V_{th} is expressed as [29]

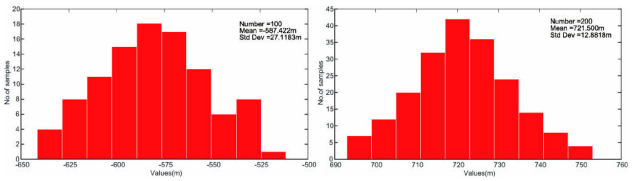
$$V_{th} = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{4}$$

$$V_{T0} = \frac{|Q'_{dep}|}{C_{ox}} - \frac{Q'_{ss}}{C_{ox}} + \phi_{MS} + 2\phi_F \tag{5}$$

$$\gamma = \frac{\sqrt{2e\varepsilon_{si}N_{sub}}}{C_{ox}} \tag{6}$$

where $\mathrm{V_{T0}}$ is the threshold voltage when $V_{SB} = 0$, Q'_{dep} is the charge in the depletion region, C_{ox} is the gate oxide capacitance per unit area, Q'_{ss} is the equivalent charge in the oxide directly adjacent to the oxide-semiconductor interface, Φ_{MS} is the gate-substrate work function difference, $2\Phi_F$ is surface potential at a strong inversion, ε_{si} is the dielectric constant of silicon, and N_{sub} is the doping concentration.

If $V_{SB} = 0$, then V_{th} is dependent on the doping and oxide thickness because $\phi_F = (kT/e)\ln(N_{sub}/n_i)$ and $C_{ox} \propto 1/t_{ox}$. Here, n_i is the carrier concentration. According to the random variations modeling in reference [28], the standard deviations of V_{th} due to the t_{ox} fluctuation are derived in Eq. (7). The standard deviation of the V_{th}



(a) (b)

Fig. 2. Monte Carlo statistical Simulation of V_{th} with 200 Numbers: (a) V_{th} of pMOSFET; (b) V_{th} of nMOSFET

fluctuation is inversely proportional to the square root of the transistor size.

$$\sigma V_{th} \propto \frac{1}{\sqrt{2WL}} \tag{7}$$

Fig. 2 shows both the V_{th} of pMOS and nMOS by a Monte Carlo statistical simulation. The figure shows that the V_{th} of pMOS and nMOS both fluctuate due to process variations.

The process variations can affect the channel resistance (R_{ds}) and current driving capability (I_{ds}) of the MOSFET. In the line region [29], R_{ds} and I_{ds} can be expressed by

$$R_{ds} = \frac{1}{g_{ds}} = \frac{L}{W\mu C_{ox}(V_{GS} - V_{th})} \tag{8}$$

$$I_{ds} = \frac{W\mu C_{ox}}{2L}[2(V_{GS} - V_{th})V_{DS} - {V_{DS}}^2] \tag{9}$$

In the saturation region [28, 29], R_{ds} is a finite value for the channel length modulation effect. I_{ds} can be expressed by

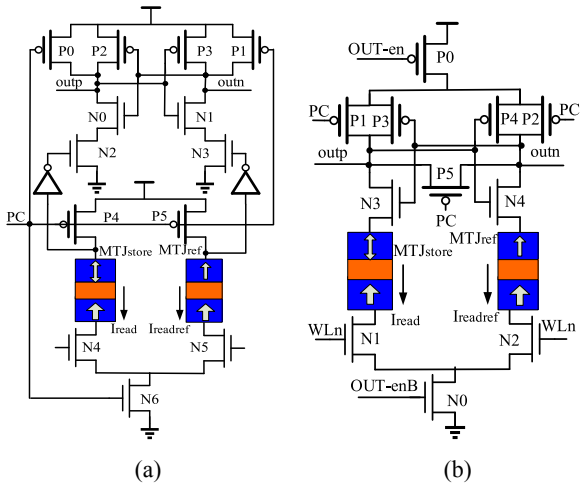
$$I_{ds} = \frac{W\mu C_{ox}}{L}(V_{GS} - V_{th})^2 \tag{10}$$

Therefore, whether in the saturation region or in the line region, the channel resistance has a negative correlation to $(V_{GS} - V_{th})$, and I_{ds} has a positive correlation to $(V_{GS} - V_{th})$. Due to the R_{ds} fluctuation of MOSFETs in the sense amplifier, the effective resistances of data branch are different from that of reference branch. Consequently, the difference in the effective resistance leads to a mismatch between data branch and reference branch, eventually leading to sense failure.

3. A proposed sense amplifier with switching transistors and balanced transistor

3.1 Sensing circuit scheme

With the research and development of STT-MRAM, many sense amplifiers have been proposed in order to obtain a higher reliability performance [5, 6, 30]. A pre-charge sense amplifier (PCSA) proposed by [5] increases the sensing speed and reduces the sensing power. However, the reliability of this scheme will decrease due to the reduced supply voltage and increased process variations. A separated pre-charge sense amplifier (SPCSA) proposed by [6], as shown in Fig. 3(a), separates the discharging and evaluation stages of the sensing operation and thus operates at a lower supply voltage. Unfortunately, the mismatch characteristics between the transistor N2 and N3 shown in Fig. 3(a) become worse due to the reduced supply voltage and increased process variations.



(a) (b)

Fig. 3. STT-MRAM sensing Structures with reference cell in P state (a) Separated pre-charge SA [6]; (b) the proposed sense amplifier with switching transistors and a balanced transistor

Based on the pre-charge sense structure [5, 6], we propose a sense amplifier, as shown in Fig. 3(b). The basic circuit configuration is similar to the PSCA, including the pre-charge transistors P1 and P2, the word selection transistors N1 and N2, and the two cross-coupled inverters (P3, N3) and (P4, N4). The MTJ_{ref} in the P state is used to make MTJ_{ref} immune to erroneous switching [13].

In addition, this sense amplifier includes a balanced transistor P5 controlled by signal "PC". The channel charge injection of the balanced transistor gives the proposed circuit a low sensitivity to process, voltage and temperature (PVT) variations. When PC is logic "0", the added balanced transistor is turned on, and a charge is stored in the channel equal to

$$Q_{ch} = -WLC_{ox}(V_G - V_{out} - V_{th}) \tag{11}$$

where V_G is the value of the PC signal when the balanced transistor is on. When the balanced transistor is turned off, this charge is injected into the source terminal and drain terminal (i.e., outp node and outn node) [23]. Because the pre-charge transistor P1 is the same as the pre-charge transistor P2, the charge splits evenly, then the change in voltage (ΔV) across the capacitor CL_{out} (i.e., the capacitor from the outp node to the GND node or the capacitor from the outn node to GND node) is

$$\Delta V = \frac{Q_{ch}}{2C_{Lout}} = \frac{-WLC_{ox}(V_G - V_{out} - V_T)}{2C_{Lout}} \tag{12}$$

Therefore, the voltage of the outp node and outn node increase at the beginning of the discharge operation. Consequently, the sensing current is increased, which enlarges the voltage difference between the outp node and the outn node. Then, the sensing margin is improved, which results in a lower read error rate.

This sense amplifier includes the switching transistors P0 and N0 controlled by signal "OUT-en" and "OUT-enB", respectively. These two added transistors can decrease the stress on the pMOSFETs P1 and P2 when logic "0" is applied at the gate terminal of P1 and P2. As a result, the NBTI effect is effectively decreased.

As shown in Fig. 3(b), the number and size of the MOSFETs in the reference branch is the same as that in the data branch. Therefore the parasitic resistances capacitances (e.g. R_S, R_D C_{GSP}, and C_{GDP} etc.) of CMOS transistors and the effective resistance of the MOSFETs in the data branch are same as those in the reference branch. Because of the t_{ox} fluctuation, a mismatch between the data branch and reference branch can occur, which leads to sense failure. Additionally, because the TMR of MTJ is limited by the MTJ material and MTJ process technology, the channel resistance of MOSFET needs to be low in order to increase the current difference between I_{read} and $I_{readref}$. Therefore, both nMOS and pMOS are used for minimum channel resistances in both directions.

As seen from Fig. 3(b), the sensing operation of the proposed sense amplifier is described in detail as followed. When the output enable signal "OUT-en" is logic "0", the switching transistors P0 and N0 are turned on. The balanced transistor P5 controlled by the PC signal is turned on at the same time, then the outp and outn nodes will be pre-charged through P1 and P2 enabled by the PC signal (i.e., logic "0" input). When the PC signal changes from logic "0" to logic "1", the sensing circuit will be put into an evaluation stage, then outp node and outn node will begin to discharge with different speeds for the different resistances between the MTJ_{store} and the MTJ_{ref}. For example, if the MTJ_{store} state is in low resistance, the outp node will discharge more quickly than the outn node. Then, the outp node will discharge to GND, and the outn node will be pre-charged to VDD though the P4 device turned on by the outp node. When "OUT-en" is logic "1", if the PC signal changes from logic "1" to logic "0", the V_{GS} of the pre-charge pMOS (P0 and P1) in conventional sensing circuits will be −VDD. Then, the pre-charge pMOS transistors are always under the stronger negative bias stress. As a result, the threshold voltage of the pre-charge pMOS is increased because of the increasing negative bias stress time. This undesirable situation is modified in the proposed sensing amplifier. Because the switching transistor P0 is turned off while "OUT-en" is logic "1", the V_{GS} values of pre-charge transistors P1 and P2 in the proposed sense amplifier are smaller than that of conventional sensing circuits. Therefore, according to the NBTI recovery theory [22, 26], the threshold voltage variation of pre-charge pMOS P1 and P2 will be reduced when the Negative Bias stress is decreased. Unfortunately, the proposed sense amplifier needs 3 added transistors, which result in an area overhead. However, this area overhead can be negligible because not only are all the MOSFETs in the sensing amplifier at the minimum size but also one sense amplifier is often widely shared in many elements of a memory array.

3.2 Simulation results

Using an accurate perpendicular anisotropy CoFeB/MgO MTJ compact model [13] and a commercial 40 nm CMOS design-kit, hybrid spice simulations and Monte-Carlo statistical simulations have been performed for the conventional sense amplifier and the proposed sense amplifier. Compared with conventional circuits, the simulation results of the proposed circuit exhibit better performance, as shown in Fig. 4 and Fig. 5. Table I gives a number of experimental parameters adopted in the MTJ compact model [13].

Table I. Major device parameters included in simulation

Parameter	Description	Default value
alpha	Gilbert Damping Coefficient	0.025
P	Electron Polarization Percentage	0.52
Ms	Saturation Field in the Free Layer	7.6×10^5 A/m
RA	Resistance area product	$5\,\Omega\,\mu m^2$
tsl	Thickness of the Free Layer	1.3 nm
a	Length or Width of surface long axis	40 nm
tox	Thickness of the Oxide Barrier	0.85 nm
TMR(0)	TMR with Zero Volt Bias Voltage	120%

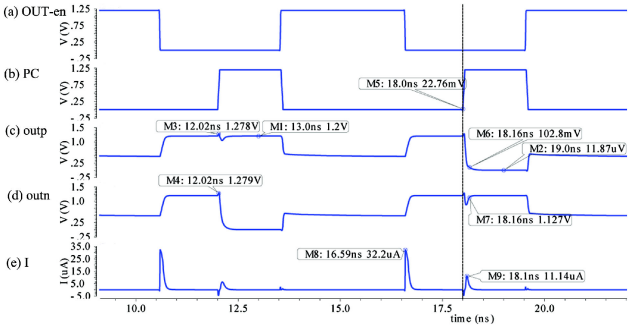


Fig. 4. The transient simulation of the proposed sensing circuit: (a) OUT-en signal; (b) PC signal; (c) outp node signal; (d) outn node signal; (e) current flowing through the sensing circuits.

Fig. 4 shows the transient simulations of the proposed sensing circuits, where TMR is 1.0 and the supply voltage VDD is 1.2 V. During the output enable signal "OUT-en" is logic "0" (e.g., time range from ∼10.5 ns to ∼13.5 ns or from ∼16.5 ns to ∼19.5 ns), and the switching transistor P0 and N0 are turned on. Consequently, outp node and outn node are pre-charged to VDD when the PC signal is logic "0" (e.g., time range from ∼10.5 ns to ∼12 ns or from ∼16.5 ns to ∼18 ns). When the PC signal changes from logic "0" to logic "1" (e.g., at ∼12 ns and ∼18 ns), the sensing circuits will be put into evaluation stage. As shown in Fig. 4(c) and (d), at ∼13 ns and ∼19 ns, the MTJ state in high resistance (e.g., point M1) and low resistance (e.g., point M2) are read out correctly, respectively. As shown in Fig. 4(c) and Fig. 4(d), when the PC signal changes from "0" to "1" (i.e., VDD) at ∼12.02 ns, the voltage of outp node (e.g., point M3) and that of outn node (e.g., point M4) are up to ∼1.278 V for the channel charge injection of the balanced transistor. As a result, the voltage between the output node and the common node of the data branch and reference branch are increased. Consequently, the sensing current is increased, which increases the voltage difference between the outp node and the outn node. Then, the sensing margin is improved, which results in a lower read error rate. Unfortunately, the switching transistors cut off the schematic from VDD to GND, which theoretically brings sensing delay. However, as seen from Fig. 4, the sensing delay (i.e., time range taken from point M5 to point M6 or to point M7) is only ∼160 ps,

which means the reading speed can still be up to 5 GHz. In addition, as seen from Fig. 4(e), the pre-charge peak current is approximately 32.2 µA and the sensing current is only 11.14 µA. Thereby, the power per bit of the sense amplifier can be calculated, which is approximately 3.88 fJ. Table II. gives the performance comparison between the proposed circuit and the conventional circuits.

Table II. Performance comparison between the proposed S.A and the conventional S.A [5, 6] (TMR = 100%)

	Proposed S.A	Conventional PCSA [5]	Conventional SPCSA [6]
Power (fJ)	3.88	2.26	5.8
Delay (ps)	154	155	114
Num. of transistor	15	12	21
Error Rate (%)	2.0	15	5.3

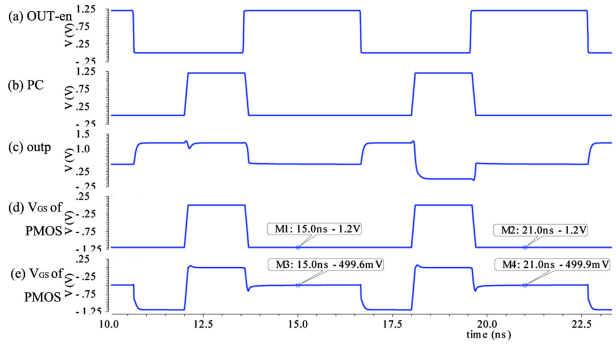


Fig. 5. The transient simulation: (a) OUT-en signal; (b) PC signal; (c) outp node signal; (d) the V_{GS} of pre-charge transistors P0 and P1 in conventional sense amplifiers; (e) the V_{GS} of pre-charge transistors P1 and P2 in the proposed sense amplifier.

Fig. 5 shows the transient simulation of the conventional sensing circuits and the proposed sensing circuit. When output enable signal "OUT-en" changes from logic "0" to logic "1" (e.g., at ~13.5 ns or ~19.5 ns), switching transistors P0 and N0 are turned off, then the V_{GS} of transistors P1 and P2 are increased. As seen from Fig. 5(d), when "OUT-en" is logic "1", the V_{GS} of pre-charge transistors P0 and P1 in conventional sense amplifiers are −1.2 V (i.e., −VDD) if the pre-charge signal "PC" is logic "0" (e.g., point M1 at ~15 ns or point M2 at ~21 ns). Then, transistors P0 and P1 are under the negative bias stress. However, as seen from Fig. 5(e), the V_{GS} of the pre-charge transistor P1 and P2 in the proposed sense amplifier is only −0.499 V (e.g., point M3 at ~15 ns or point M4 at ~21 ns), which is much smaller than V_{GS} (−1.2 V) of pre-charge transistors P0 and P1 in conventional sense amplifiers (shown in Fig. 5(d)). Therefore, according to the NBTI model [26], when the negative bias stress is decreased, the threshold voltage variation of both P1 and P2 will be reduced. Moreover, the threshold voltage variation can be calculated from Eq. (3) by setting model constants (i.e. A, B, C, k, φ_0, β and E0) related to the process [26].

Through 1000 Monte-Carlo simulations, the reading error rates of different sense amplifier schemes versus different TMR ratios are shown in Fig. 6. There are some

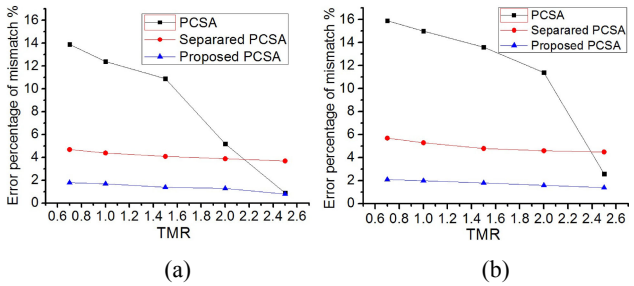


Fig. 6. The reading error rate comparison of different sense amplifier schemes according to different TMR ratios: (a) the process variations from only CMOS transistors; (b) the process variations from both CMOS transistors and MTJ devices.

mismatches of circuit components, for example, the process variations from both CMOS transistors and MTJ devices, and the parasitic resistances and capacitances (i.e. R_{line} and C_{line}) of the interconnections. By optimizing placement and routing of sensing circuit layout, the difference of the parasitic RCs of the interconnections between the data branch and the reference branch can be decreased to a minimum. The process variations from the MTJ device result in the variation of the insulator thickness (t_{ox}), the free layer thickness (t_f), and the MTJ surface area etc., which can lead to a variation of MTJ resistance. This resistance variation has been taken into account in the MTJ model. By using a convenient component description format parameter to enable or disenable resistance variation, the effect of resistance variation can be chosen to be integrated or not. Fig. 6(a) shows the simulation results, in which only the process variation from CMOS transistors is taken into account. Fig. 6(b) shows the simulation results, in which the process variations from both CMOS transistors and MTJ devices are taken into account. The difference of the reading error rates between Fig. 6(a) and Fig. 6(b) shows the resistance variation increases sensing error rate. Both Fig. 6(a) and Fig. 6(b) show that the reading error rate will be reduced if the TMR becomes larger. Additionally, compared with the PCSA and the separated PCSA, the reading error rate of the proposed sense amplifier is always minimum and depends weakly on the TMR value. Though the TMR can reach 604% at room temperature in laboratory devices [31], it is still limited by the MTJ material and MTJ process technology. Therefore, the sensitivity to process variations of proposed circuits is reduced and more suitable for highly reliable STT-MRAMs.

4. Conclusion

In this paper, by adding switching transistors and a balanced transistor, a novel sense amplifier architecture has been presented to improve the reliability of the sense amplifier. The performance based on the proposed sense amplifier and theoretical calculations has been performed. The simulation results reveal that the proposed sense amplifier not only decreases the NBTI effect on the pMOS device but also decreases the sensitivity of the sense amplifier to the PVT. Therefore, this novel sense amplifier scheme can be used for an STT-MRAM with a high reliability requirement.

Acknowledgments

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