

LETTER

# Design of broadband Class EF power amplifier based on low-pass filter matching structure

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**Abstract** This paper proposes a broadband Class EF power amplifier based on a low-pass filter matching structure. Based on the theory of Class EF power amplifiers, the optimal fundamental load impedance required is derived. A broadband matching circuit is then designed using a low-pass filter prototype. In the meantime, a compact harmonic control circuit is proposed to meet the harmonic impedance requirements of class EF power amplifiers. In order to validate the effectiveness of the proposed method, a 2.6–3.6 GHz broadband class EF power amplifier is designed and fabricated. Measurement results show that the output power is between 40.68 dBm and 41.6 dBm at 1 dB compression point in 2.6–3.6 GHz. From 62% to 78% drain efficiency is obtained with gain greater than 10 dB.

**Keywords:** class EF power amplifier, low-pass filter matching, broadband, harmonic control

**Classification:** Microwave and millimeter-wave devices, circuits, and modules

## 1. Introduction

The rapid development of mobile communications requires the better performance of RF front-end circuits [1, 2]. Especially for power amplifiers (PAs), the related characteristics such as bandwidth and efficiency must be greatly improved. Recently, many high-efficiency RF PAs have been reported in [3, 4, 5, 6, 7, 8, 9, 10, 11]. The traditional harmonic control PAs such as Class F PAs [12, 13, 14, 15] and switch PAs like class E PAs [16, 17, 18, 19] have become the research hotspots because of their ideal 100% drain efficiency. The hybrid class EF PAs presented in [20] have received more and more attention recently for which they have the advantages of both class E and class F PAs. The class EF PAs absorb the soft switching characteristic of class E that enables it to achieve 100% drain efficiency while having a low peak drain voltage that is similar to that of class F PAs [21, 22, 23]. However, due to the influence of the output capacitance of the transistor, the class EF PAs often cannot have a wider bandwidth at higher frequencies [24, 25]. Therefore, it brings many limitations for development of class EF PAs.

In this paper, the optimal fundamental load impedance is derived based on the theory of Class EF PAs in order to realize the broadband class EF PA. Then the low-pass filter

model is applied to design the broadband fundamental output matching network. In addition, a compact harmonic control network is proposed to achieve the required harmonic impedance in a wide band. In order to validate the effectiveness of the proposed method, a broadband class EF PA is designed and fabricated.

## 2. Analysis and design of class-EF PA

The basic circuit schematic of the class EF PA is shown in Fig. 1 [26].

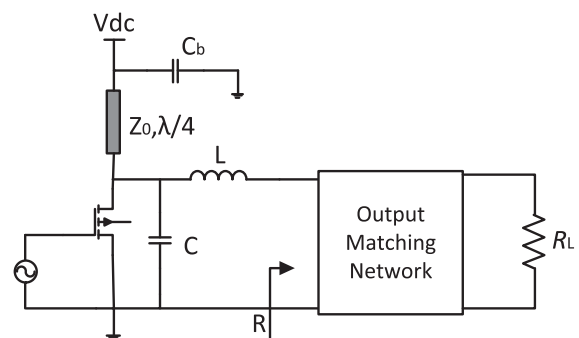


Fig. 1. The schematic of Class-EF PAs

As shown in the Fig. 1, the  $C$  is output capacitance of the transistor which can be calculated as [26]

$$C = \frac{\pi}{2} \left( \frac{\sin \tau_D}{1 + \cos \tau_D} \right)^2 \frac{P_o}{\omega_0 V_{DC}^2} \quad (1)$$

Where  $\tau_D$  is the turn-off time of the transistor (in radians).  $P_o$ ,  $V_{DC}$  represent the output power and the DC voltage of the power supply, respectively.

The inductance  $L$  can be written as [26]

$$L = \frac{\tau_D - 0.5 \sin(2\tau_D)}{\sin^2 \tau_D} \frac{R}{\omega_0} \quad (2)$$

The resistance  $R$  can be expressed as [26]

$$R = \frac{2(1 + \cos \tau_D)^2}{\pi^2} \frac{V_{DC}^2}{P_o} \quad (3)$$

Then, the optimal fundamental load impedance  $Z_{opt}$  can be obtained as [26]

$$Z_{opt} = R + j\omega_0 L \quad (4)$$

The expression of the optimal load impedance can be obtained by combining Eq. (1), (2), (3) and (4).

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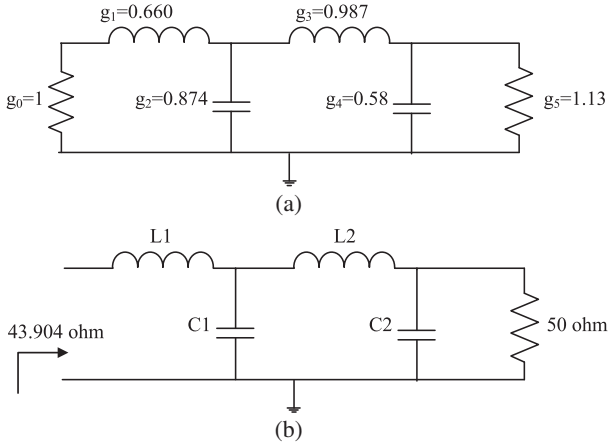
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$$Z_{opt} = \left(1 + j \frac{\tau_D - 0.5 \sin(2\tau_D)}{\sin^2 \tau_D}\right) \frac{2(1 + \cos \tau_D)^2}{\pi^2} \frac{V_{DC}^2}{P_o} \quad (5)$$

According to [21],  $\tau_D = 48.5^\circ$  is taken for obtaining the maximum PAE. Therefore, Eq. (5) can be simplified as

$$Z_{opt} = (1 + j0.616) \frac{0.56 V_{DC}^2}{P_o} \quad (6)$$

Low-pass filter model is applied to achieve a wideband fundamental matching circuit. To simplify the design process, the real impedance of  $Z_{opt}$  is first considered in designing a low-pass matching network. For 10 W of output power, 28 V of DC voltage, the real part of impedance can be obtained as 43.904 by Eq. (6). Then the impedance ratio between load of 50  $\Omega$  and  $Z_{opt}$  can be calculated as 1.13:1. According to [27], a second-order low-pass filtering should be adopted for 32% fractional bandwidth in 2.6–3.6 GHz. Fig. 2(a) shows the second-order low-pass filtering prototype according to [28]. And Fig. 2(b) is the actual schematic diagram under 50  $\Omega$  load system.



**Fig. 2.** The low-pass filter matching diagram (a) low-pass filtering prototype (b) schematic diagram under 50  $\Omega$  load system.

The center frequency  $f_0$  is taken at 3.1 GHz. The values of the inductance  $L$  and the capacitance  $C$  in Fig. 2(b) can be calculated by Eq. (7) and (8):

$$L_n = g_{2n-1} \frac{\omega'_0}{\omega_0} \frac{50}{g_0} \quad (7)$$

$$C_n = g_{2n} \frac{\omega'_0}{\omega_0} \frac{g_0}{50} \quad (8)$$

Where the  $\omega'_0$  and  $g_0$  are the normalized angular frequency and impedance, respectively. And the parameter values of each  $L$  and  $C$  are shown in Table I.

**Table I.** Parameter values of low-pass filter matching network elements

Elements	Value
$L_1$	0.77 nH
$C_1$	10.26 pF
$L_2$	1.16 nH
$C_2$	6.81 pF

The PA circuit designed in this paper operates at GHz frequency. The values of inductance  $L$  and the capacitance  $C$  are not easy to maintain precise in so high frequency [29]. Therefore, the LC matching networks shown in Fig. 2(b) should be transformed into a matching network of distributed parameters. During the conversion process, inductors  $L_1$  and  $L_2$  should be replaced by high-impedance transmission-line sections. In addition, the capacitors  $C_1$  and  $C_2$  are replaced by low-impedance open-circuit stubs [30]. The relationships between distributed circuits parameters and LC networks are shown as follows:

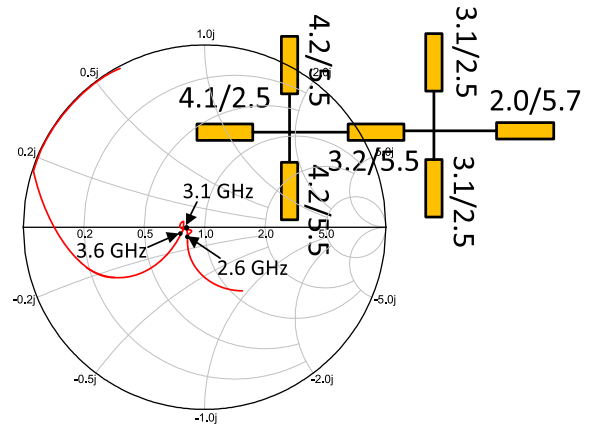
$$\omega L \cong Z_H \beta l \quad (9)$$

$$l \cong \frac{v_p L}{Z_L} \quad (10)$$

$$\frac{1}{\omega C} = 2 \frac{Z_L}{\tan \beta l} \quad (11)$$

$$l \cong \frac{\arctan(2\omega Z_L C)}{\beta} \quad (12)$$

Where  $Z_H$ ,  $Z_L$  are the characteristic impedance of the high-impedance transmission-line and the low-impedance transmission-line, respectively.  $\beta$ ,  $v_p$  are the propagation constant and phase velocity of the transmission line, respectively. Then the overall circuit optimization will be performed in the ADS software. At this time, the imaginary reactance of the  $Z_{opt}$  can be dealt with through continuously optimizing and adjusting. The low-pass filter matching circuit of distributed parameters is shown in Fig. 3. In the meanwhile, Fig. 3 also shows the input impedance of the matching circuit. It can be found that the input impedance of the distributed parameters matching circuit is about 48  $\Omega$  in the frequency range of 2.6 GHz to 3.6 GHz.



**Fig. 3.** The low-pass filter matching circuit and the simulated input impedance of the circuit.

It is also very critical that the design of the harmonic control circuit for the class EF PAs. This paper proposes a compact harmonic control microstrip circuit. As shown in Fig. 4,  $TL_1$ ,  $TL_2$  and  $TL_3$  make the second harmonic impedance zero. The  $TL_1$ ,  $TL_4$ ,  $TL_5$  and the arc microstrip open the third harmonic. The simulated output harmonic impedances of the transistor are also shown in Fig. 4 by connecting to the harmonic control circuit. It can be seen

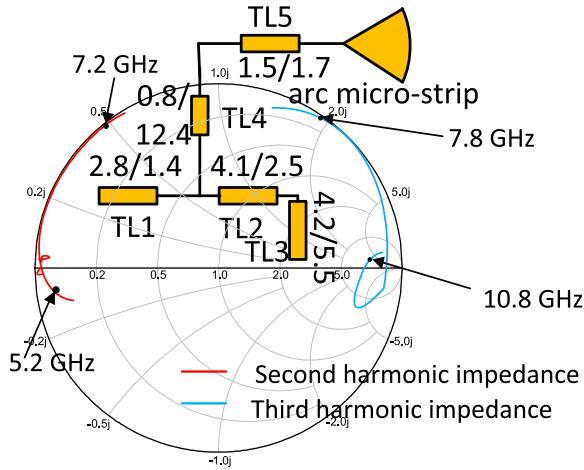


Fig. 4. The proposed compact harmonic control circuit and output harmonic impedances of the transistor.

that the second harmonic impedances are approximately 0 and the third harmonic impedances are about infinity.

### 3. Fabrication and measurement results

In order to validate the effectiveness of the proposed design method, a broadband class EF PA is designed and fabricated using CGH40010F transistor, based on the Rogers 4350B substrate ( $\epsilon_r = 3.66$ ,  $H = 30$  mil). The bias voltages of drain and gate are 28 V and  $-2.8$  V, respectively. The designed complete schematic is shown in Fig. 5. And a photograph of the fabricated PA is shown in Fig. 6.

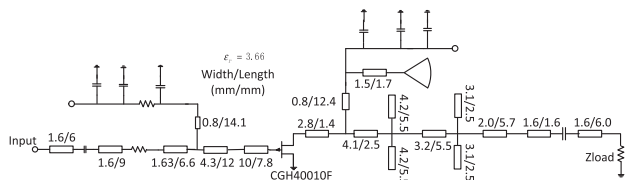


Fig. 5. Complete circuit schematic of proposed class EF PA

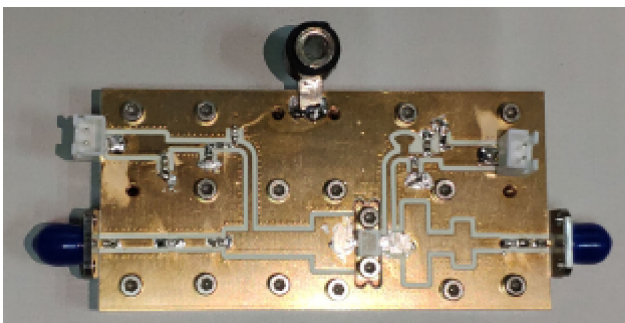


Fig. 6. Photograph of the fabricated PA

The implemented PA is measured by using a continuous signal when driving to the 1 dB compression point. The measured results are plotted in Fig. 7 and Fig. 8. It can be seen from Fig. 7 that the measured output power is between 40.68 dBm and 41.6 dBm in 2.6–3.6 GHz. Between 62% and 78% of drain efficiency can be obtained. In addition, the gain is greater than 10 dB. Fig. 9 shows the

ACLR in the frequency range under the 5 MHz WCDMA signal testing. It can be seen that the ACLR is better than  $-25$  dBc with 35.6 dBm of average output power in 2.6–3.6 GHz.

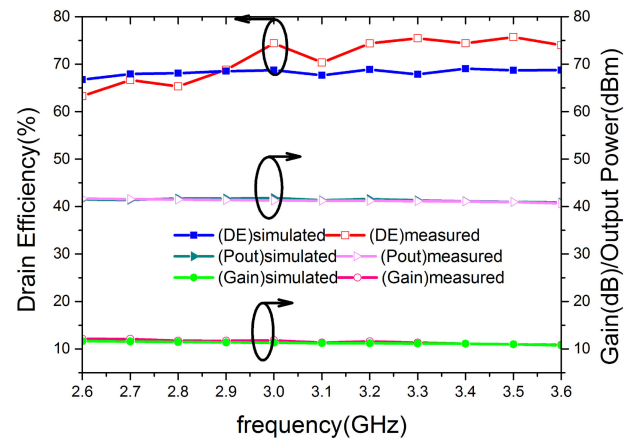


Fig. 7. The measured and simulated output power, drain efficiency and gain.

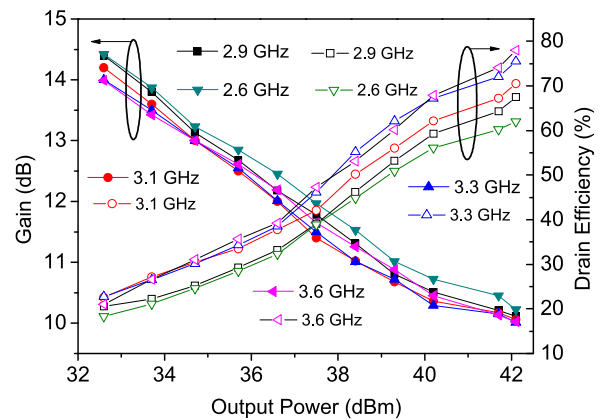


Fig. 8. The measured drain efficiency and gain versus output power

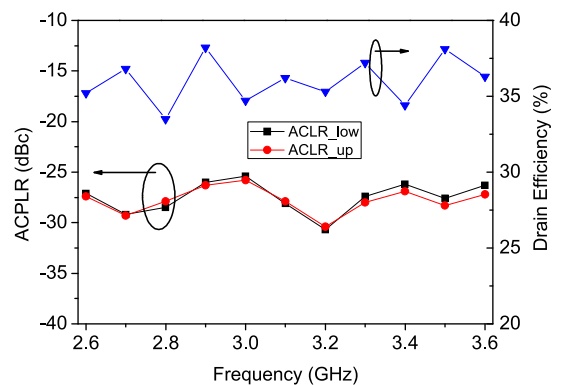


Fig. 9. Measured ACLR and drain efficiency in 2.6–3.6 GHz at an output power about 35.6 dBm, using a 5 MHz WCDMA signal with PAPR @6.5 dB.

Table II lists the performance comparison between the proposed class EF PA and related PAs reported in previous papers. It is obvious that the class EF PA designed in this paper has a bandwidth beyond the previously reported class EF PA. In addition, compared with related high-

efficiency PAs such as Class E and class F, the proposed PA has the better output power with similar drain efficiency.

**Table II.** Performance comparison of broadband high efficiency PAs

Ref	Class	Frequency (GHz)	FBW (%)	DE (%)	Pout (dBm)
[8]	J	2.6–3.5	20.6	60–71	40.1–40.5
[12]	F	1.5–2.2	37.8	61–72	39.6–40.5
[16]	E	2.5–3.5	33.3	50–69	37.2–38.4
[21]	EF	1.4–1.9	30.3	42–73	36.3–38.7
[22]	EF	2.9–3.8	26.8	65–70	39.6–43.1
This Work	EF	2.6–3.6	33.5	62–78	40.7–41.6

#### 4. Conclusion

This paper presents a method for designing broadband class EF PAs. The optimal fundamental load impedance is derived based on the theory of class EF PA. Then the low-pass filter prototype is applied for designing the broadband fundamental matching network. At the same time, a compact harmonic control network is proposed to achieve the adjustment of harmonic impedance in a wide frequency range. The designed and fabricated class EF PA has a bandwidth that exceeds the previously reported class EF PA. In addition, it is better than other high efficiency PAs in term of output power.

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