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LETTER

Enhanced voltage swing of rapid-single-flux-quantum distributed output amplifier equipped with double-stack superconducting quantum interference devices

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Abstract We report the enhanced voltage swing of a rapid-single-flux-quantum (RSFQ) distributed amplifier by replacing a single superconducting quantum interference device (SQUID) with a double-stack-SQUID (DSS). A DSS is composed of two stacked 2-junction SQUIDs sharing one sensing inductor. Thanks to its stack structure, a DSS is expected to generate twofold output voltage. We have designed a 12-stage RSFQ distributed amplifier equipped with DSSs. The maximum output voltage swing reached 10.2 mV in simulation. Test chips were fabricated using a 25-μA/μm^2 Nb integration process. In measurements, a test chip was cooled in a liquid helium bath. The experimental output voltage swing was up to 8.34 mV.

Keywords: superconducting integrated circuits, single flux quantum, Josephson effects, niobium, cryogenic electronics

Classification: Superconducting electronics

1. Introduction

The development of superconducting digital circuits has been accelerated for the last three decades [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]. Among several superconducting circuit configurations, the rapid single-flux-quantum (RSFQ) technology, where the existence and absence of a single flux quantum (SFQ) in a superconducting loop represent the binary digital states of "1" and "0", is the most developed and widely used [1]. One example is a 33 GHz-clock RAM-embedded microprocessor comprising 10,603 Nb Josephson junctions [16].

An SFQ signal propagating on a Josephson transmission line (JTL) has a pulse shape. To make a data link from superconducting RSFQ digital IC to room-temperature electronics, digital states represented by SFQ pulses should be converted to digital states in voltage levels. The most common device for SFQ–voltage conversion is an SFQ-to-DC (s/d) converter, which converts an SFQ pulse to a non-return-to-zero (NRZ) voltage signal [1]. One drawback of an s/d converter is its small swing of output voltage. It is on the order of 100 μV for Nb Josephson junctions, for which a pre-amplifier is necessary to make a data link to room-temperature electronics. As a result, the bandwidth is often limited by that of a pre-amplifier.

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To lift limits on the bandwidths on SFQ–voltage conversion, many groups have developed on-chip RSFQ output amplifiers that realize voltage swings beyond 1 mV. On-chip RSFQ output amplifiers are classified in terms of their biasing schemes. A Suzuki stack [17, 18] and a four-junction loop (4JL) gate [19, 20] are AC biased, whereas a hybrid unlatching flip-flop logic element (HUFFLE) gate [21, 22], a superconducting quantum interference device (SQUID) array [23, 24], and a distributed single-SQUID amplifier [25] are DC biased. In this paper, we focus on a DC-biased distributed amplifier. A decade ago, a 12-stage distributed single-SQUID amplifier realized a data link bandwidth as wide as 10 Gbps, while its voltage swing was limited less than 2 mV [25].

In our previous work, we enhanced the voltage swing of a distributed amplifier by replacing a single-SQUID with a double-stack-SQUID (DSS) [26]. A DSS is a 4-junction SQUID with two superconducting loops [27]. In other words, it is composed of two stacked SQUIDs sharing one sensing inductor. Thanks to its stack structure, a DSS is expected to generate twofold output voltage [27, 28]. Figs. 1 and 2 illustrate the configuration of a distributed DSS amplifier and the equivalent circuit of one stage, respectively. Its operation sequence is explained as follows. The input SFQ pulses are transferred alternatively to either "set" or "reset" JTL via a toggle flip-flop (TFF). Then, they set/reset the storage loop of each stage and switch on/off the DSS, resulting in an NRZ output signal. Numerical simulation demonstrated that a 4-stage distributed DSS amplifier generated a 204% voltage swing in comparison with a 4-stage distributed single-SQUID amplifier. We designed and fabricated a 4-stage distributed DSS amplifier using a Nb integration technology. Low-speed test results demonstrated correct operation with the maximum voltage swing of 2.93 mV [26].

In this paper, we describe our design and operation of a 12-stage distributed DSS amplifier.

2. Design and fabrication of RSFQ distributed output amplifier equipped with double-stack-SQUIDs

In designing a 12-stage distributed DSS amplifier, we used the same cell layout as our previous work [26]. That is, we simply increased the number of stages by connecting the fundamental cells shown in Fig. 2 and JTLs. Except for DSSs, we used digital cells (JTLs, a TFF, splitters, etc.) in the library referred to as "CONNECT" [29].

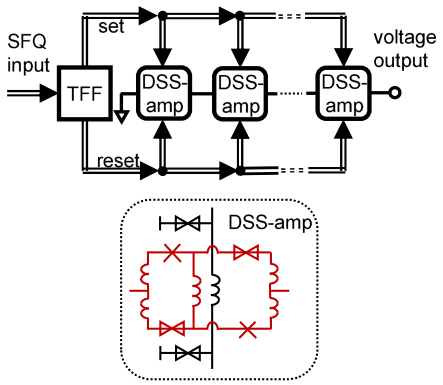

Fig. 1. Schematic illustration of a distributed DSS amplifier. "DSS-amp" denotes an amplifier element comprising a DSS coupled with an SFQ storage loop.

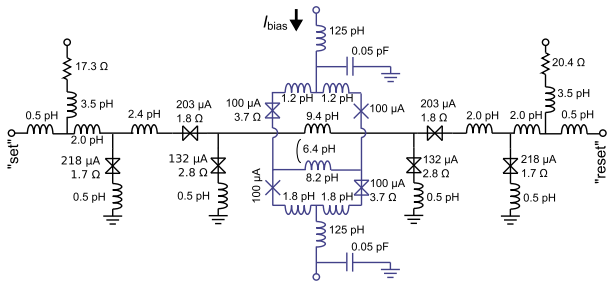

Fig. 2. Equivalent circuit of one stage of a distributed DSS amplifier. "X" and hourglass symbols represent an unshutned (under-damped) junction and a critically-damped junction, respectively. Resistance values near hourglass symbols are the values of shunting resistors.

Test chips were fabricated using a 25-μA/μm^2 Nb/AlO_x/Nb integration process [30] at the National institute of Advanced Industrial Science and Technology, Japan. Fig. 3 shows a photomicrograph of a 12-stage distributed DSS amplifier. A DC-to-SFQ converter (d/s) [1] is placed at the input terminal of the circuit.

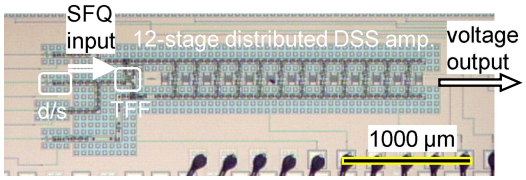

Fig. 3. Photomicrograph of a 12-stage distributed DSS amplifier on Nb IC.

In measurements, a test chip was cooled in a liquid helium bath. The output voltage was acquired with a digital oscilloscope as an open-end voltage via a 40-dB low-noise preamplifier. Due to the limitation of our experimental setup, the input signal frequency was set below 100 kHz. That is, quasi-static characteristics were measured.

3. Results and discussion

Typical waveforms of a sinusoidal input current and an NRZ output voltage are shown in Fig. 4, where an SFQ is fed to the distributed DSS amplifier via the DC-to-SFQ converter at every rising slope of the input voltage signal.

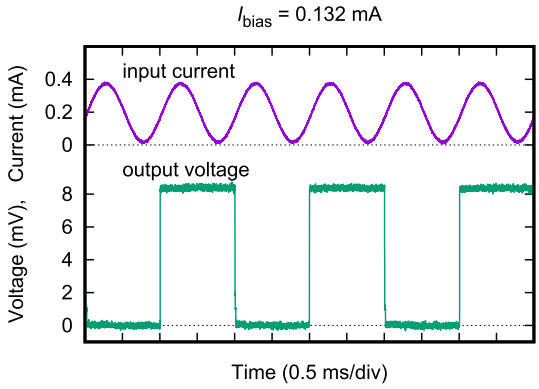

Fig. 4. Waveform example of a sinusoidal input current and an NRZ output voltage. The bias current to the DSSs (I_{bias}) is 0.132 mA.

From here, the term of "voltage swing (V_{swing})" is defined as the voltage difference calculated by subtracting the voltage at the "reset" state from the voltage at the "set" state. The value of V_{swing} shown in Fig. 4 is 8.34 mV.

V_{swing} depends on I_{bias}. To evaluate the I_{bias} dependence of V_{swing} in detail, the output voltages for the "reset" and "set" states were measured for various I_{bias} values. The results are shown in Fig. 5 with the corresponding numerical results. (We used a Josephson circuit simulator referred to as "JSIM" [31] for numerical simulation.) From Fig. 5, experimental and numerical V_{swing} values are derived and plotted in Fig. 6 as functions of I_{bias}.

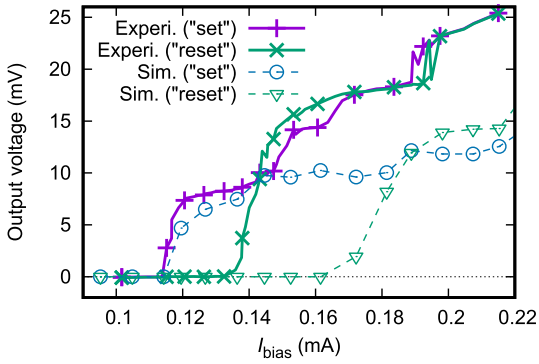

Fig. 5. Experimental and numerical I_{bias}–voltage characteristics of the 12-stage distributed DSS amplifier for both the "set" and "reset" states.

Under the condition of $I_{bias} < 0.135$ mA, the experimental results agreed well with the numerical ones as shown in Figs. 5 and 6. The experimental V_{swing} value reached 8.34 mV.

On the other hand, it can be found in Fig. 6 that the experimental operation margin for I_{bias} was reduced to one-third of the numerical margin. The experimental V_{swing} values decreased rapidly for $I_{bias} > 0.135$ mA. The numerical maximum V_{swing} value of 10.2 mV was obtained under the condition of $I_{bias} = 0.162$ mA, which was out of the operation condition in experiments.

The direct reason of the difference in the numerical and experimental I_{bias} margins is the difference of the zero-voltage regions for the "reset" state. That is, in experiments, the I_{bias} region for the zero-voltage state is quite narrower than the numerical results.

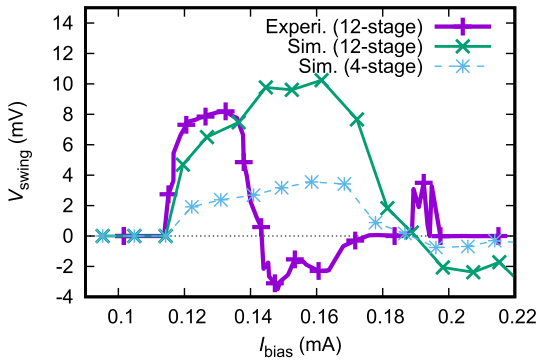

Fig. 6. Voltage swing (V_{swing}) plotted as functions of the bias current (I_{bias}). Experimental and numerical results for the 12-stage distributed DSS amplifier are represented by the solid curves, whereas numerical results for the 4-stage distributed DSS amplifier are plotted by a dashed curve.

Such considerable reduction of the I_{bias} margin was not observed in our previous 4-stage distributed DSS amplifier. In addition, it is also found in Fig. 6 that the numerical I_{bias} margins of the 4-stage and 12-stage distributed DSS amplifiers are almost the same. Although it is unclear at the moment what caused the margin reduction, possible origins are inadequate layouts around the DSSs and non-uniform critical currents in 12 DSSs due to flux trapping or fabrication variations. Tolerance design should be improved to obtain wider operation margins.

4. Conclusion

We enhanced the voltage swing of an RSFQ distributed DSS amplifier. The output voltage was expected to be doubled by employing a DSS in place of a single-SQUID. A test circuit was fabricated on niobium integrated circuits and tested in a liquid helium bath. The enhanced voltage swing was confirmed, of which the maximum value was 8.34 mV.

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