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LETTER

An efficient background timing skew calibration technique for time-interleaving analog-to-digital converters

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Abstract An efficient background timing skew calibration algorithm is proposed in this article, which detects the sampling time mismatches in time-interleaving analog-to digital converter (TIADC) by estimating the skew-related errors with a reference channel and aligns the sampling edge of each sub-ADC to that of the reference channel by analog variable-delay lines in the negative feedback loop. Compared with conventional background calibration methods based on complex algorithms or serious input restrictions, the proposed technique detects timing skews by only negligible hardware consisting of simple digital blocks and is applicable for a wide range of input including completely random signals. The detailed theoretical analysis and sufficient simulated results revealed that this algorithm is not sensitive to some non-ideal components in actual circuits like mismatches between channels or jitters in clock circuits, which verifies the practicability and robustness of this method.

Keywords: time-interleaving analog-to-digital converter, timing skew calibration, background calibration, reference channel

Classification: Electron devices, circuits and modules

1. Introduction

TIADC structure is a usual way for high-speed and low-power analog-to-digital converters (ADC) [1]. By multiplexing several ADCs in parallel, TIADCs can achieve multiplication of conversion speed in a power-efficient manner. However, mismatches between channels introduce undesirable errors and degrade the overall performance of the system. The major errors are caused by offset, gain mismatches and timing skews. The previous two types of errors can be calibrated easier relatively since they are all static errors. In contrast, timing skews are hard to be corrected since the skew-induced errors are dependent on input content. Worse still, errors caused by timing skews, as shown in Fig. 1, are proportional to the frequency of input signals and hence become the primary concern in high-speed TIADCs.

There are many researches on timing skew in recent two decades [2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30], along with numerous relevant calibration methods raised. Reference-signal-injection methods in [2, 3, 4, 5] detect timing skew with a predetermined input signal, which are straightforward and effective. But like all other foreground calibration methods, the calibration procedures cannot be performed without interrupting ADC's work. FIR filters can eliminate skew-related errors in parallel with normal system's operation [6, 7, 8, 9, 10, 11, 12], but this approach places certain restrictions on the bandwidth of input. What's worse, the increase of ADC's resolution rate will lead to an explosive boosting of the filters scale, which limited its application for high precision requirement. To solve these problems, blind adaptive calibration techniques are proposed in [13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25], they utilize statistics of the input and behave well in high precision applications. However, on account of the complex algorithms, their high cost in power consumption and area of the digital calibration block cannot be neglected, even in modern CMOS technology. Another kind of statistic-based techniques is autocorrelation calibration algorithm [26, 27, 28, 29, 30]. The autocorrelation intensity between adjacent channels has negative relation with their timing skews, in case of the input is wide-sense stationary signal or its statistic property is stationary. So the timing skews can be eliminated by adjusting the sampling clock of each channel to search the maximum autocorrelation intensity. Autocorrelation-based calibration methods are popular recently since they impose little restrictions on input signals and provide a good trade-off between the calibration accuracy and the algorithm complexity. Nevertheless, the main disadvantage of this class of methods is that they all rely on the statistics of the input signal. In practice, the amplitude, bandwidth and statistics of input could vary from time to time. In such cases, autocorrelation-based calibration will induce larger mistakes.

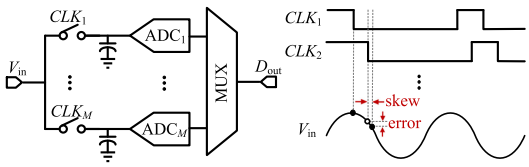

Fig. 1. The block diagram of the TIADC with timing skew diagrams

Taking into account the drawbacks of these calibration schemes above, this article proposed an efficient background timing skew calibration algorithm that is appropriate for completely random input. Better still, the calibration is achieved by simple digital blocks and low power consumption. In Section II, the proposed calibration algorithm is introduced in detail. Section III describes some concerns related to this scheme in practical circuits. Simulated

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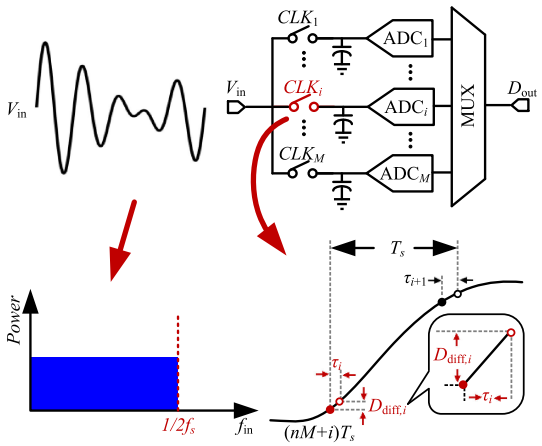

Fig. 2. The first order approximation of skew-related errors in ith channel with the maximum input frequency limited in the first Nyquist domain

results are revealed and discussed in Section IV, followed by the conclusion in Section V.

2. Proposed timing skew calibration algorithm

A block diagram of the M channels TIADC is shown in Fig. 2. The input $V_{\text{in}}(t)$ is sampled by each sub-ADC and converted to digital outputs. The clock input and the digital output of the ith ADC are CLK_i and D_i[n], respectively. i equals $1, 2, \ldots, M$. The sampling period of TIADC is T_s, which is also the ideal time-shifting between CLK_i and CLK_{i+1}. It's obvious that

$$D_{out,i} = V_{in}(t - (nM + i)T_s) \tag{1}$$

Multiplexing all sub-ADC outputs results in

$$D_{out}[n] = V_{in}(nT_s) \tag{2}$$

However, timing skews will modifies the time-shifting into $T_s + \tau_i$, where τ_i is the timing skew between the actual CLK_i and the ideal CLK_i. For the Nyquist sampling,

$$f_{in,\max} < \frac{1}{2} f_s \tag{3}$$

where $f_{\text{in,max}}$ is the maximum frequency of $V_{\text{in}}(t)$ and f_{s} is the frequency of the TIADC ($f_s = 1/T_{\text{S}}$), as exhibition in Fig. 2. Since $\tau_i \ll T_{\text{S}}$, it's assumed without loss of generality that

$$|\tau_i| \leq 0.1 T_s \tag{4}$$

Therefore, the different output values of the ith ADC with and without τ_i, $D_{\text{diff},i}$ can be described with a Taylor expansion as

$$D_{diff,i} \approx \tau_i \left. \frac{\partial V_{in}(t)}{\partial t} \right|_{t=(nM+i)T_s} \tag{5}$$

which is demonstrated in Fig. 2.

The ith channel samples $V_{\text{in}}(t)$ repetitively along with the systems working and a battery of varying $D_{\text{diff},i}$ is generated. Accumulating $|D_{\text{diff},i}|$ by N times, then the sum can be represented mathematically as

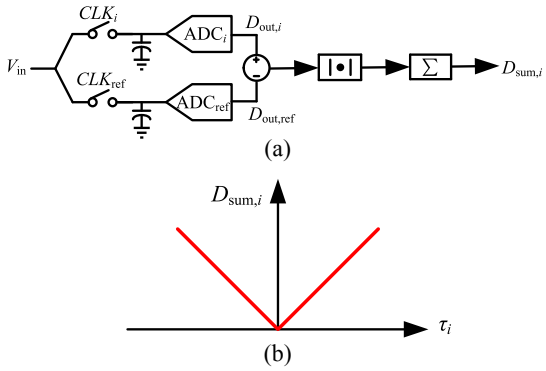

Fig. 3. (a) The proposed timing skew detection diagram. (b) The relationship between $D_{\text{sum},i}$ and $|\tau_i|$ in theory.

$$\begin{aligned} D_{sum,i} &= \sum_{n=n_i}^{n_i+N} \left(\left| \tau_i \times \frac{\partial V_{in}(t)}{\partial t} \right|_{t=nMT_s+iT_s} \right) \\ &= |\tau_i| \times \sum_{n=n_i}^{n_i+N} \left(\left| \frac{\partial V_{in}(t)}{\partial t} \right|_{t=nMT_s+iT_s} \right) \end{aligned} \tag{6}$$

where $D_{\text{sum},i}$ is the sum of $|D_{\text{diff},i}|$ and n_i is the initial point of this accumulation. Denote the Fourier transform of $V_{\text{in}}(t)$ as $X(j\omega)$, the derivative of $x(t)$ can be estimated as:

$$\begin{aligned} \frac{\partial V_{in}(t)}{\partial t} &= \frac{1}{2\pi} \int_{-\infty}^{+\infty} j\omega X(j\omega) e^{j\omega t} d\omega \\ \left| \frac{\partial V_{in}(t)}{\partial t} \right| &\in \left[0, \left(\frac{\partial V_{in}(t)}{\partial t} \right)_{\max} \right] \end{aligned} \tag{7}$$

where $(\partial V_{\text{in}}(t)/\partial t)|_{\max}$ is the maximum value of the derivative of $V_{\text{in}}(t)$. Since $V_{\text{in}}(t)$ is band-limited, $(\partial V_{\text{in}}(t)/\partial t)|_{\max}$ is a finite value. Consequently, when $N \to +\infty$, $D_{\text{sum},i}$ can be expressed as

$$\begin{aligned} D_{sum,i} &= |\tau_i| \times \sum_{n=n_i}^{n_i+N} \left(\left| \frac{\partial V_{in}(t)}{\partial t} \right|_{t=nT_s} \right) \\ &= |\tau_i| \times N \times \left| \frac{\partial V_{in}(t)}{\partial t} \right|_{t=t'} \Bigg| \end{aligned} \tag{8}$$

where

$$\left| \frac{\partial V_{in}(t)}{\partial t} \right|_{t=t'} \Bigg| \in \left[0, \left(\frac{\partial V_{in}(t)}{\partial t} \right)_{\max} \right]$$

From (8) it can be discovered that $D_{\text{sum},i}$ is proportional to $|\tau_i|$ when N is infinite. Thus, timing skews can be estimated from the variance of $D_{\text{sum},i}$, which could be obtained by a reference channel, as plotted in Fig. 3(a). ADC_{ref} is the reference channel that samples $V_{\text{in}}(t)$ at the same time with ADC_i, ideally. The value of $D_{\text{sum},i}$ is a function of timing skew between the sampling edges ($|\tau_i|$) of these two ADCs, and is minimized when $|\tau_i|$ is reduced to zero, as depicted in Fig. 3(b).

The sampling edges of ADC_{ref} should coincide with the ideal sampling points of all sub ADCs. In order to cycle through and calculate $D_{sum,i}$ for each sub-ADC, the period of the reference channel's clock (CLK_{ref}) is chosen as $l \times T_s$, where l and M are relatively prime. Fig. 4 shows the timing grid of each CLK_i and CLK_{ref} while $l = M + 1$. The first sampling edge of CLK_{ref} coincides with the ideal sampling edge of CLK_1, the second sampling edge of CLK_{ref} coincides with the ideal sampling edge of CLK_2,

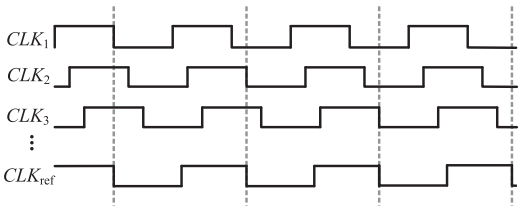

Fig. 4. Sampling time diagram for CLK_i and CLK_{ref}.

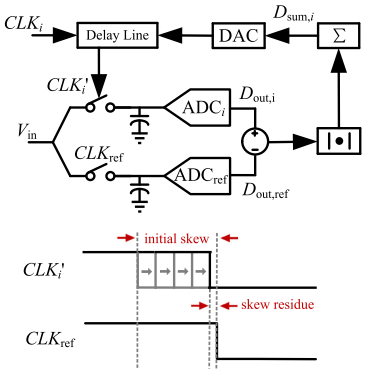

Fig. 5. The background calibration diagram of the ith channel

and so on for all M ADCs. This allows digital detection circuits to calculate each $D_{sum,i}$ severally. The whole behavioral calibration model includes $D_{sum,i}$ computation scheme, register, DAC and variable digital-control sampling-time delay lines. After computation all $D_{sum,i}$, the calibration model drives each delay line with negative feedback, just as exhibited in Fig. 5. Since each sub-ADC has its own delay line, the digital backend minimizes $D_{sum,i}$ between each sub-ADC and ADC_{ref} by adjusting the M delay lines independently. The minimized timing skews after correction are related to the unit time delay of the delay lines, which is determined by the maximum tolerable *SNDR* penalty, as revealed in [9]. For the same maximum tolerable *SNDR* penalty, the system with a higher speed and higher resolution rate needs smaller τ_i, which means a finer unit delay time.

The proposed timing skew calibration technique has no extra restriction on input but only its bandwidth limitation described by (3), which is the basic precondition of all types of Nyquist ADCs. Therefore, this calibration algorithm is widely applicable to a variety of input, including sine signals, wide sense stationary signals, completely random signals and so on. In contrast to other conventional calibration techniques with too complex algorithms that are hard to devise in circuits or only applicable to software implementation, the scheme presented above may be more practical for it simplifies the calibration logic using only addition and subtraction, not some expensive multiplication or division. The existence of ADC_{ref} may bring large power consumption during the calibration process. In fact, all calibration circuits including ADC_{ref} could operate at very low speed since the cycle of ADC_{ref} could be adjustable and large enough with a big l, which means low-power dissipation. In other words, the variable l provides a trade-off between correction rate and power consumption of the calibration block.

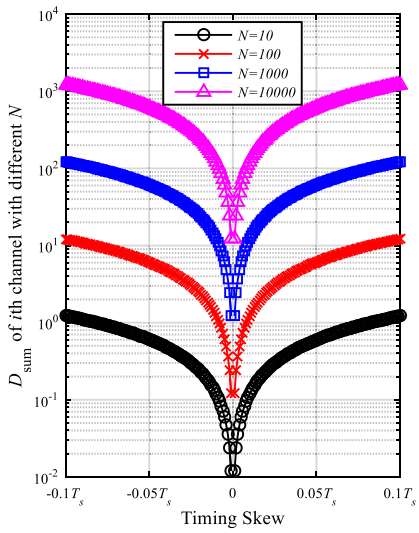

Fig. 6. The detection result of the ith channel with varying N

3. Design concerns in implementation

Although the proposed timing skew calibration method has the merits of robustness against the completely random signal and algorithm simplicity, there are some concerns should be taken into account in practical.

3.1 The selection of the accumulative frequency (N) in practice

$D_{sum,i}$ is obtained by accumulating $D_{diff,i}$ N times, as exhibited in Section II. (8) is true only when N is infinite, which is impossible in real design. This precondition may support a point of view that N should be large enough for adequate calibration accuracy in actual application. Well, that is exactly the truth. But a large N would result in immense additional hardware consumption and a long-time calibration cycle, made this scheme worthless. In fact, a large N is not necessary for most instances, as clarified in Fig. 6. It's obvious that the $D_{sum,i}$ of the ith channel is proportional to $|\tau_i|$ within a wide range of N. This relationship could be maintained even when N is 10. But the contrary, N should not be too small as well in practice since the accumulation itself plays an important role in the calibration process. A proper N will suppress non-ideal concerns in circuits, especially jitters in clock paths, thus improves the stability in skew detection.

3.2 Effects of mismatches in sub-ADCs and the reference channel

Considering that the timing skew calibration process is aided by the reference channel outputs, the influences of mismatches between channels including offsets and gain errors in real circuits should be analyzed. Fig. 7(a) shows how offsets effect $D_{sum,i}$ ($N = 1000$) in variable timing skew. The simulated results are based on channels with unit of 12-bit LSBs. When there is no timing skew, $D_{sum,i}$ ($N = 1000$) should be zero ideally since the reference channel samples the same points of input with the channel to be calibrated. With offsets exist, $D_{sum,i}$ became the sum of those N offsets each, obviously. The same goes for other

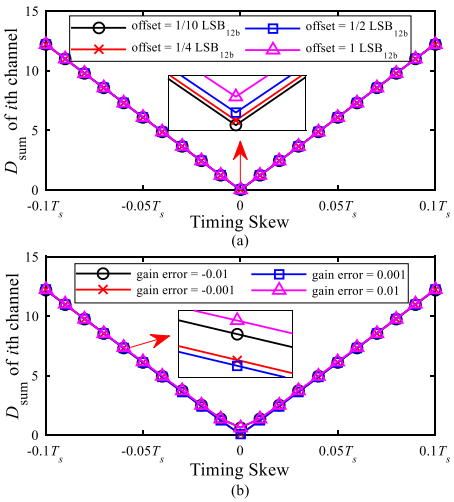

Fig. 7. The skew-related errors detection along with different mismatches between channel to be calibrated and the reference channel (with N equals 1000 in each D_{sum}). (a) The effect of varying offsets in 12-bit sub-ADC. (b) The effect of varying gain errors

timing skews, made the curves move lines up and down with the extent proportional to the value of their corresponding offsets. A similar result is shown by the effect of gain error, as demonstrated in Fig. 7(b). Different gain errors cause various slopes of the curves. Fortunately, $D_{\text{sum},i}$ is proportional to $|\tau_i|$ all through, whatever the offset or gain error is. The minimum $D_{\text{sum},i}$ appears only when timing skew is zero, same as in the ideal case. Furthermore, the timing skews of each channel will be detected severally by the reference channel and the mismatches between them have no effects on calibration. As a whole, the mismatches in sub-ADCs and the reference channel will not degrade the performance of the calibration result.

3.3 The restriction of the calibration for low-frequency input

It must be pointed out that the proposed calibration technique does not detect the value of timing skew directly, but measure the related error caused by timing skew. Thus, for the same accuracy of error measurement, the accuracy of timing skew and the skew residue after correction will vary for different input signals. As revealed by Fig. 8, the error from a fixed timing skew is proportional to the derivative of the input signal. The voltage of high-frequency input has a violent change in the time domain, which could form larger D_{diff} and D_{sum} for the same skew. Then the relatively larger skew can be identified more easily. It means that the calibration method performs better for high-frequency applications. However, the correction results for inputs with most of their energy concentrated on the low-frequency band may have larger residual skews but the same power of skew tones. Considering DC input (the most extreme status), the testing result will always be zero whatever the real timing skew is. Fortunately, skew related errors decrease also with low-frequency inputs.

4. Simulation results

This proposed timing skew calibration technique are verified with a 8 bit 4 GS/s four channel TIADC designed in 65 nm 1.1 V CMOS technology to test its feasibility and practicability, as Fig. 9 shows. The flash ADC is chosen to be the sub-ADC architecture and the same as the reference channel. The analog core area is 0.46 mm^2 and the digital calibration area is 0.017 mm^2.

Fig. 10 shows the DFT spectrums of this TIADC outputs before and after calibration. The initial timing skews added into each channel are [$\tau_1 = 0.6\%$Ts, $\tau_2 = -2\%$Ts, $\tau_3 = 2.2\%$Ts, $\tau_4 = 0.9\%$Ts], separately. Some other non-ideal factors like offsets are entered in these models to

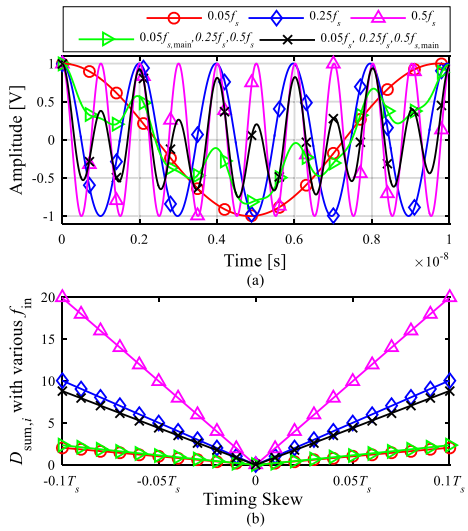

Fig. 8. (a) Different input signals in time domain. (b) The detection results of various inputs (with N equals 1000 in each D_{sum})

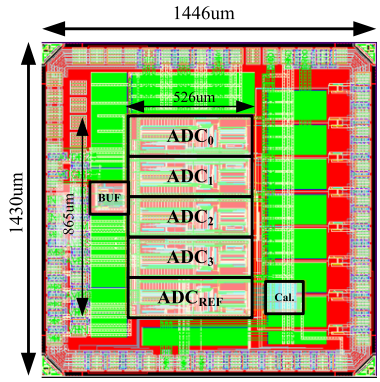

Fig. 9. Layout of the 4G 8 bit TIADC

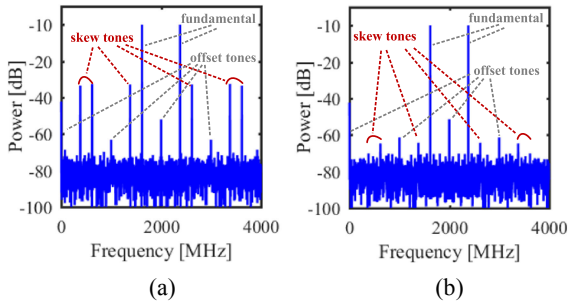

Fig. 10. Simulated DFT performances of the TIADC before and after the timing skew calibration, with fundamental tones and offsets in each channels exists. N equals 1000. (a) Before calibration. (b) After calibration

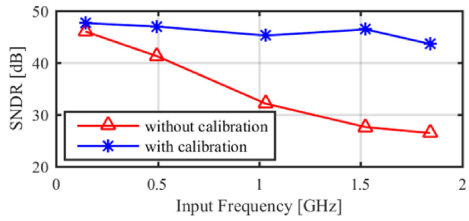

Fig. 11. Simulated dynamic performance of the TIADC in relation to the input frequency before and after calibration

replicate a real environment. With the maximum tolerable *SNDR* penalty, 3 dB, the unit calibration step of each clock phase delay line is set to approximate 100 fs. As denoted in Fig. 10, the output spectrum is limited by the spurs due to timing skews without calibration. After calibration, the magnitude of these spurs have dropped about 30–35 dB even in the presence of offsets. Because the spurs of timing skews and gain mismatches appear at the same places of the spectrum, the gain mismatches were not introduced into this simulation to prevent the confusion of these two types of spurs. Similar result would emerge with gain mismatches exist since they do not interfere with the final calibration result, as expound in Section III. This comparison reveal the accuracy of this proposed timing skew calibration algorithm is insensitive to mismatches between channels, in contrast to other conventional calibration algorithms utilizing reference channels on which mismatches residue after calibration impose a serious restriction.

Fig. 11 shows the *SNDR* of this TIADC as functions of f_{in} around the entire Nyquist band. As discussed above in Section III, though the proposed algorithm goes against input with low-frequency, the skew-related errors are also vulnerable under the present circumstance. These two opposite effects combined to make *SNDR* after calibration be approximate "flat" on the whole during all frequency band of input.

Table I gives a performance summary of this work and comparison with some other related works. The proposed timing skew calibration method had lower digital hardware cost than [7, 9, 30] for its easier skew estimation block with no multipliers or filters.

Table I. Performance comparison.

	[7][1]	[9][1]	[30][1]	This Work[2]
Timing Skew Estimation	FIR + correlator	subtraction detection	auto-correlation detection + Auxiliary ADC	subtraction detection + auxiliary ADC
# of FIR filter	1	1	0	0
# of Multiplier[3,4]	2	2	4	0
# of Adder[3,4]	7	7	9	1
Convergence Time (Samples)	10 K	80 K	32 K	44 K[5]

1. Measurement result
2. Post layout simulation result
3. for per subADC channel
4. for the estimation and correction of timing skew
5. for the correction of $\tau_{\max} = 10\%$ of T_s and $N = 1000$

5. Conclusion

An efficient background timing skew calibration technique has been proposed in this paper, which estimates the sampling clock errors of each sub-ADC with a reference channel and corrects them by minimizing the related errors caused by timing skews. The skew detection process requires only some simple add/subtract operation that could be easily realized by a spot of digital logic cells but not some complex digital blocks, like multipliers or dividers. The calibration result is not affected by mismatches between the sub-ADCs to be calibrated and the reference channel. A suitable N of estimation errors in algorithm made it insensitive to jitters from clock circuits. This timing skew calibration technique can be implemented in TIADCs with arbitrary channels and complex random input. Although the maximum frequency of input is limited in the Nyquist frequency for all types of Nyquist ADCs, the algorithm itself can operate properly even with over-Nyquist input until (5) is not valid. The practicability and robustness of this timing skew calibration technique were confirmed through in-depth simulations.

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