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LETTER

An implementation of belief propagation decoder with combinational logic reduced for polar codes

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Abstract In this letter, a combinational logic reduced belief propagation (BP) decoder for polar codes is designed in 55 nm CMOS technology. The authors first introduced the BP decoding algorithm for polar codes, and then analyzed the architectures of the conventional BP decoders. Finally, the hardware implementation with the proposed multiplexed process element architecture is presented. Synthesis results show that the consumption of hardware resources is reduced by 36%. The architecture and circuit techniques reduce the power to 398 mW for an energy efficiency of 292 pJ/b. The throughput is improved to 4.36 Gbps by applying the G-matrix early stopping criteria.

Keywords: polar codes, belief-propagation, scaled min-sum, muxed-pe
Classification: Integrated circuits

1. Introduction

Polar codes, which were invented by E. Arıkan, have been proven to be able to achieve the capacity of binary-input discrete memoryless channels (B-DMCs) with low encoding and decoding complexity [1]. The basic decoding algorithm of polar codes is the successive-cancellation (SC) decoding algorithm that was proposed by E. Arıkan [1]. In addition to the SC-based decoders [2, 3, 4, 5, 6, 7], the belief-propagation (BP) decoding algorithm was also applied by some researchers to polar codes [8, 9, 10, 11, 12]. The SC-based decoders of polar codes are sequential in nature, which leads them to suffer from high decoding latency. Compared with SC, BP has a parallel data processing architecture, which offers some improvements to the decoding throughput [13, 14, 15, 16, 17]. However, a major problem with BP is that it consumes too much hardware resources in parallel computing.

Several BP decoders have been designed for polar codes in [15], [16] and [17], with the aim to reduce the hardware complexity and decoding latency. In [15], an overlapped-scheduling approach at iteration level was proposed to reduce the overall decoding latency. Since the iteration-level overlapping schedule has high hardware utilization, its hardware complexity is relatively high, although the decoding latency can be effectively reduced. To further reduce the decoding latency, a double-column architecture was designed in [16] for a better utilization of a clock period. In [16], the operations of two adjacent columns are merged in one clock cycle, which means that it sacrifices the critical path in exchange for decoding latency. In [17], a stage-combined BP decoding algorithm was proposed to reduce the memory usage, where two adjacent columns are combined into one so that intermediate messages do not need to be stored. However, none of the above papers consider the fact that the message propagation in BP is unidirectional to allow only one of left-to-right or right-to-left messages to be propagated, which means that some hardware resources can be reused in the time domain.

In this letter, a combinational logic reduced belief propagation decoder for polar codes is presented. The conventional factor graph of polar BP decoding is based on bidirectional process element (PE). The PE updates both left-to-right and right-to-left messages, whereas the message propagation is unidirectional to allow only one of left-to-right or right-to-left messages to be propagated. Therefore, some hardware resources can be reused in the time domain. Based on this fact, a multiplexed process element (muxed-pe) architecture is introduced to reduce the consumption of combinational logic. Based on synthesis in 55 nm CMOS technology, the muxed-pe decoder provides a decoding throughput of 1.37 Gbps at 400 MHz using 15 iterations at the worst-case 1.08 volts and 125°C. Compared with the conventional scaled min-sum (SMS) decoder [13], the proposed muxed-pe decoder reduces the consumption of hardware resources by 36%.

The remainder of the letter is organized as follows. Section 2 briefly reviews the principle of the belief propagation decoding algorithm for polar codes. Section 3 proposes a new muxed-pe architecture for BP-based polar decoders. Section 4 illustrates performance analysis and comparisons. Finally, Section 5 concludes the letter.

2. Review of belief propagation polar decoders

As a class of linear block error correcting code, polar codes can be identified as a parameter vector (N, K), where N is the block length, K is the information size.

The polar code BP decoder was proposed in [8] based on the factor graph representation. Fig. 1 shows the basic process elements (PEs) of the polar code BP decoder. For a polar code with a block length of $N = 2^n$, its factor graph contains n stages, and each stage has $N/2$ PEs [18]. Here,

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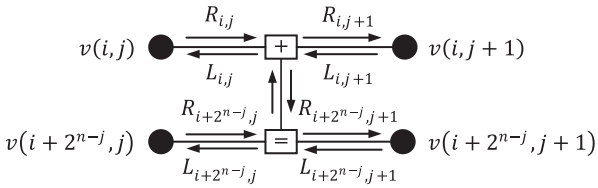

Fig. 1. Basic process elements of the BP decoder.

$R_{i,j}$ and $L_{i,j}$ are the log-likelihood ratio (LLR) of the left-to-right message and the right-to-left message of the node $v(i, j)$, respectively.

An example of BP factor graph for the case of $(8, 4)$ polar code is given in Fig. 2. Here the factor graph has a total of $n = log_2 8 = 3$ stages. Each stage consists of $N/2 = 4$ process elements that are used to update the propagated messages.

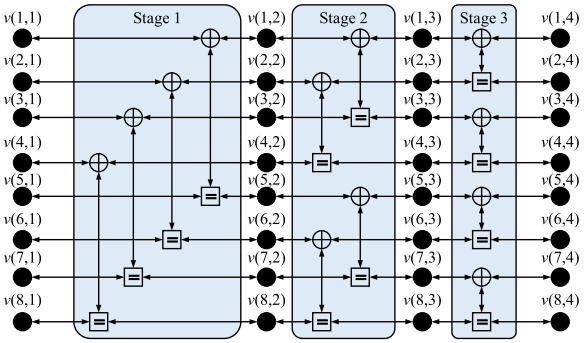

Fig. 2. Factor graph of $(8, 4)$ polar codes.

In general, the BP algorithm can be simplified using the min-sum (MS) approximation [19, 20, 21, 22], which greatly reduces the complexity of the hardware implementation, but incurs a degradation in decoding performance. In [13], a scaled min-sum (SMS) belief-propagation decoder was proposed to perform a linear message updating process without losing error performance. For a SMS-BP decoder, the computational process includes two steps. The first step delivers the LLRs in the factor graph from the right-most nodes to the left-most nodes. For node i of j layer at t-th iteration, the update rules provided in [13] are

$$\begin{cases} L_{i,j}^{t} = \lambda \times g(L_{i,j+1}^{t-1}, R_{i+2^{n-j},j}^{t} + L_{i+2^{n-j},j+1}^{t-1}) \\ L_{i+2^{n-j},j}^{t} = \lambda \times g(L_{i,j+1}^{t-1}, R_{i,j}^{t}) + L_{i+2^{n-j},j+1}^{t-1} \end{cases} \tag{1}$$

Similarly, the second step delivers the LLRs in the factor graph from the left-most nodes to the right-most nodes. The update rules are

$$\begin{cases} R_{i,j+1}^{t} = \lambda \times g(R_{i,j}^{t}, R_{i+2^{n-j},j}^{t} + L_{i+2^{n-j},j+1}^{t-1}) \\ R_{i+2^{n-j},j+1}^{t} = \lambda \times g(R_{i,j}^{t}, L_{i,j+1}^{t-1}) + R_{i+2^{n-j},j}^{t} \end{cases} \tag{2}$$

where $g(\alpha, \beta) = sign(\alpha)sign(\beta)\min(|\alpha|, |\beta|)$ is the propagation function that updates the LLR messages, λ is the scale factor that reduces the approximation error.

After updating the left-to-right LLRs of all nodes, one iteration is completed. In general, a sufficiently large number of iterations can provide a good error performance. However, experience shows that when the channel has a low noise level (high SNR scenario), the BP decoders can always decode the valid output without achieving the maximum number of iterations [23, 24, 25, 26]. In order to reduce the redundant iterations of BP-based polar decoders, some efforts have been made in [27]. Inspired by the H-matrix of low-density parity-check (LDPC) decoders [28], G-matrix early stopping criterion was proposed in [27]. The generator matrix of polar codes plays a key role in G-matrix method. After each iteration, the detected left-most bits ($\hat{u}$) are re-encoded by the generator matrix (G) of polar codes. After that, the re-encoded bits ($\hat{u}G$) and the decoded right-most bits ($\hat{x}$) are applied to Eq. (3). If the result of Eq. (3) is zero, the decoding is finished according to the G-matrix criteria.

$$\sum(\hat{u}G \oplus \hat{x}) \tag{3}$$

By applying the G-matrix early stopping criteria to the BP-based polar decoders, the number of iterations can be effectively reduced and the decoding throughput can be greatly improved [27, 29, 30].

3. Proposed muxed-pe architecture

Recall that the LLR calculations of the SMS algorithm are described by Eq. (1) and Eq. (2). In general, these four equations can be categorized into two types: Type-I $d = \lambda \times sign(a)sign(b + c)min(|a|, |b + c|)$ and Type-II $d = a + \lambda \times sign(b)sign(c)min(|b|, |c|)$. Accordingly, the high-level architectures of these two types of computation are given in Fig. 3 and Fig. 4, respectively. Here, the S2C unit converts the number representation of the sign-magnitude form into the two's complement form, and C2S unit performs the inverse conversion. Besides, the scale unit implements the scaling function. It can be seen that these two types of computations involve a large amount of combinatorial logic. In addition, the high-level architecture of the conventional PE represented by these two types of computations is given in Fig. 5. As illustrated, Type-I and Type-II are used independently for the computation of the left-to-right and right-to-left LLR messages [15, 16, 17].

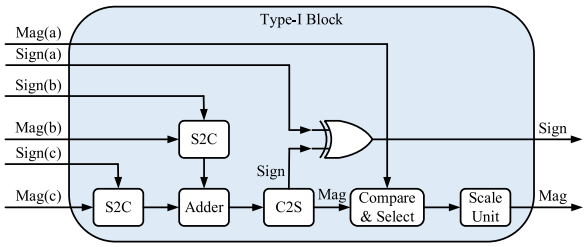

Fig. 3. High-level architecture of the Type-I block.

Since the BP decoder contains a large number of PEs, if the resource usage of Type-I and Type-II is lowered, the hardware resource consumption of the BP decoder can be effectively reduced. For the BP-based polar decoders, an indisputable fact is that the message propagation in BP is unidirectional to allow only one of left-to-right or right-to-left messages to be propagated [8], which means that some hardware resources can be reused in the time domain.

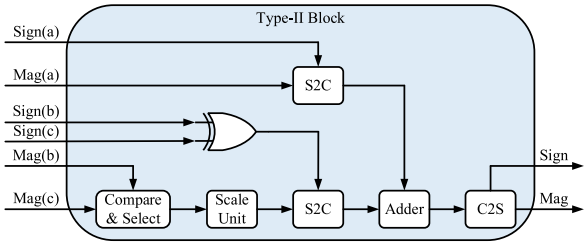

Fig. 4. High-level architecture of the Type-II block.

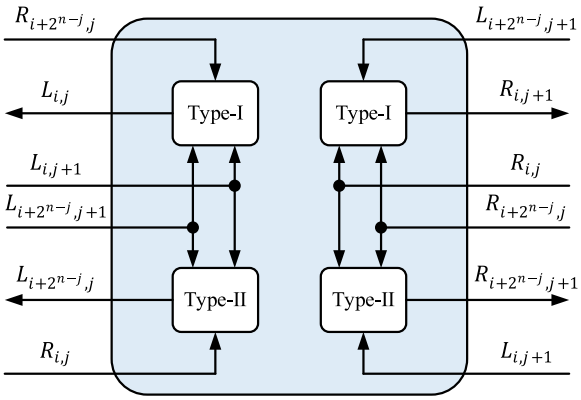

Fig. 5. High-level architecture of the conventional PE.

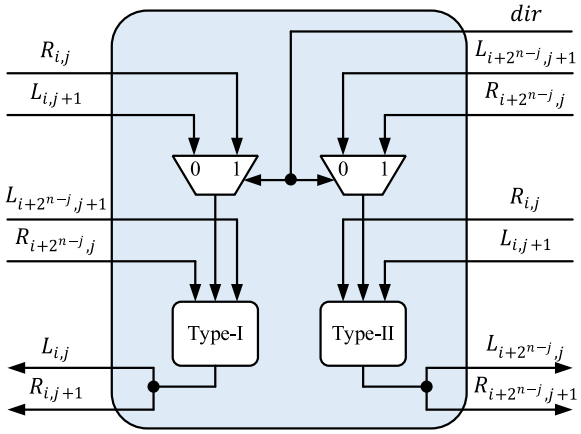

Fig. 6. High-level architecture of the proposed muxed-pe.

Based on this fact, we designed a multiplexed process element (muxed-pe) architecture to reuse Type-I and Type-II to achieve the purpose of reducing combinatorial logic, as shown in Fig. 6. The proposed muxed-pe architecture introduces a control signal *dir* for selecting the input LLR messages. When *dir* is equal to 0, the LLR messages propagating from right to left are selected, and when *dir* is equal to 1, the LLR messages propagating from left to right are selected, which means that Eq. (1) and Eq. (2) are activated respectively in these two cases.

Since the proposed muxed-pe architecture is a general solution that optimizes MS-based operations, it can also be applied to any other type of BP-based polar decoders.

4. Performance analysis and comparisons

In this section, the performance of different BP-based polar decoding architectures is analyzed. Here, polar codes with a block length of $N = 1024$ and a code rate of $R = 0.5$ are used. The SMS-BP decoder is selected with a scale factor of $\lambda = 0.9375$ [13]. The maximum number of iterations is set to 15 and the Monte Carlo method is utilized to assess the average number of iterations.

Fig. 7 shows the FER (frame error rate) performance of the G-matrix and original BP decoding without early stopping methods. As illustrated, there is no performance loss because of using early stopping method.

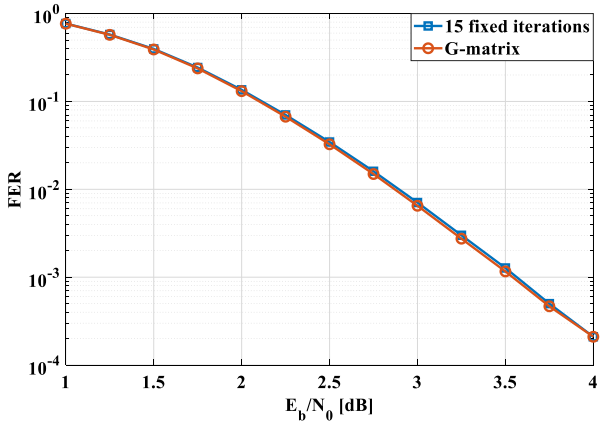

Fig. 7. FER comparisons of the (1024, 512) polar codes.

Fig. 8 shows the average number of iterations of the G-matrix early stopping criterion under various SNRs. It can be seen that the number of iterations of the BP decoder can be effectively reduced by using the G-matrix method, which helps to reduce the decoding latency and improve the throughput.

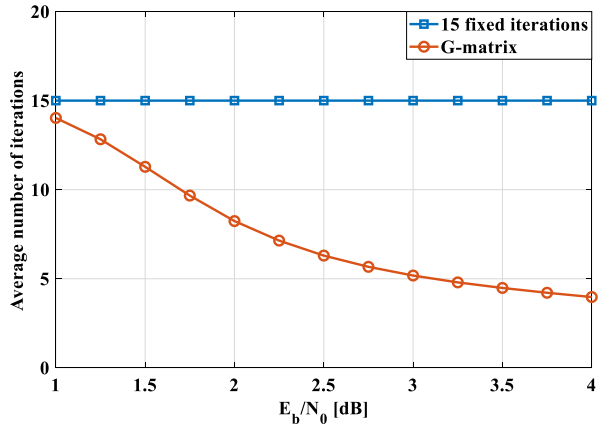

Fig. 8. Average number of iterations with the G-matrix method for (1024, 512) polar BP decoding.

The RTL (Register Transfer Level) models of the optimized SMS-BP polar decoder with proposed muxed-pe architecture are developed with Verilog HDL (Verilog Hardware Description Language). The designs are synthesized by Synopsys Design Compiler with SMIC (Semiconductor Manufacturing International Corporation) CMOS 55 nm library. The supply voltage is 1.08 volts with worst timing model at 125°C. For a fair comparison, the same parameters are used for the conventional SMS-BP polar decoder. The comparison results in terms of hardware efficiency and energy efficiency are shown in Table I. Here,

Table I. Performance of different (1024, 512) polar decoders.

Design (7-bit Quantization)	SMS Decoder	SMS Decoder with muxed-pe	SMS Decoder with muxed-pe and G-matrix
CMOS Technology	55 nm	55 nm	55 nm
Maximum Clock Frequency (MHz)	400	400	400
Total Gate Counts	1986419	1278299	1563359
Power (mW)	496	398	431
Average Number of Iterations @3.5 dB	15	15	4.5
Average Latency (Cycles) @3.5 dB	300	300	94
Average Throughput (Gbps) @3.5 dB	1.37	1.37	4.36
Hardware Efficiency (Normalized)	1	1.55	4.06
Energy Per Bit (pJ/bit) @3.5 dB	363	292	99

the hardware efficiency (HE) is the ratio of throughput to total gate counts and the energy per bit (EPB) is the ratio of power to throughput. The values of HE and EPB are calculated as Eq. (4) and Eq. (5), respectively.

$$HE = \frac{ClockFrequency \times N}{DecodingLatency \times TotalGateCounts} \tag{4}$$

$$EPB = \frac{Power \times DecodingLatency}{ClockFrequency \times N} \tag{5}$$

where the power is reported by Synopsys Design Compiler, N is the block length and the unit of decoding latency is clock cycle.

From Table I, it can be seen that the proposed muxed-pe decoder can achieve a 36% reduction in hardware resources and a 55% increase in hardware efficiency compared to the conventional SMS decoder. Since the throughput of the conventional SMS decoder and the proposed muxed-pe decoder are the same, the hardware efficiency represents the inverse value of the reduction ratio of hardware resources. In addition, the power consumption of the SMS decoder with muxed-pe is lowered thanks to the reduction of the combinational logic compared with the conventional SMS decoder. Therefore, the EPB of the proposed muxed-pe decoder is reduced to 292 pJ/b, which is further reduced to 99 pJ/b by applying the G-matrix method. With a simple early termination scheme of G-matrix, the average number of iterations is lowered to 4.5 at a 3.5 dB SNR with no loss in error correcting performance. In addition, the use of G-matrix criterion leads to an additional latency of four clock cycles. Early termination enables a higher throughput of 4.36 Gbps at 431 mW. Therefore, the proposed muxed-pe architecture is a good candidate for low-complexity and high-performance polar decoder designs.

5. Conclusion

In this letter, a combinational logic reduced belief propagation decoder for polar codes is designed in 55 nm CMOS technology. With the proposed muxed-pe architecture, optimized SMS-BP polar decoder is developed. Synthesis results show that the proposed architecture has significant advantages with respect to hardware reduction. Since the proposed muxed-pe architecture is a general solution that optimizes MS-based operations, it can also be applied to any other type of BP-based polar decoders.

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