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LETTER

Layout optimization methodology for ring-based on-chip optical network

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Abstract When integrating an optical network into a chip, the communication characteristics and the power cost of the network should be considered. In this letter, to fulfill data coherence communication, a non-intention ring-based optical network which supports multicast and broadcast is studied. To further eliminate the power penalty cost due to waveguide crossing, a layout optimization methodology is proposed. By dividing an optical network into several sections and placing them part-by-part into different areas, the total number of cross points is reduced by 83.3%, 71.7% and 70.2% in networks supporting four-, six- and eight-core communication respectively.

Keywords: optical, on-chip network, interconnect, layout optimization
Classification: Optical hardware

1. Introduction

On-chip optical network has been a promising candidate for many-core computing system. The on-chip network serves the communication of cores or processing units. The building of a network should fully consider performance requirements, power constraints and area limitations [1]. The structure of the optical on-chip network can be divided into two categories: one is based on routers, and the other is based on switching fabric(s).

A distinctive property of a router-based network is the variance of hops and latency costs for message transmission. Mesh, torus and folded torus are typical router-based optical interconnects [2, 3]. Many studies, such as the router architecture design [4], application mapping on mesh [5, 6], crosstalk noise analysis [7], power adaption [8], mesh network simulator [9], etc., are based on the mesh network. Some other network structures can be regarded as derivatives of mesh or torus networks [10, 11, 12, 13, 14].

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Compared to a router-based network, the number of hops is constant in switching-based network. Therefore, the latency generated by the network can be much more easily predicted and controlled. Some switching-based networks such as fat tree [15] are multi-hop, and messages will be buffered along the path. Other switching-based networks are bufferless during the transmission from an input port to the output port, and the transmission can be regarded as one hop [16, 17, 18, 19]. In addition to the network topology, the layout optimization methodologies are proposed to eliminate the gap between logic design and chip layout [20, 21, 22, 23].

In a multicore computing system, data coherence occurs in hierarchically shared memory [24, 25, 26]. For cache coherence communications, a predictable network latency is a key requirement for maintaining the order of packets. In this letter, a switching-based on-chip optical network, which is derived from our previous work [19], is selected as the research target for many-core communication and we further optimize the topology layout to reduce optical insertion loss. The switching-based network consists of multi ring-based waveguides and is suit for data coherence communication which contains multicast and broadcast. For simplicity, we refer the target network as ring-based network in the following sections. Considering the layout of waveguides and microresonators, a layout optimization methodology to minimize the waveguide cross points is proposed. By optimizing the layout locations, the number of cross points is reduced significantly. Fewer cross points induce better performance in laser power cost and crosstalk performance. Our proposed ring-based network optimization methodology can cooperate with the other layout optimization tools for further optimization gains, considering the on chip optical devices' geometries [27], interfaces' locations [28], and chip thermal management [29].

2. The ring-based network and the layout optimization methodology

Considering the number of cores is much larger than that of memory modules in a computing system, we select an improved version of our previously proposed ring-based network for core-to-core communication. Compared with the previously proposed network, the improved version utilizes different ring waveguide to distinguish different destinations. Therefore, for N-core system, the number of ring waveguide in the improved network will be

N − 1 instead of N. The decrease of the ring waveguide reliefs the waveguide layout complexity and reduce the unnecessary waveguide crossing. Another change is that considering the potential inter-wavelength crosstalk in one waveguide, optical messages to/from different destinations will be injected/ejected from/to modulator/detector through dependent waveguides (referred as auxiliary waveguides in this letter). Though the structure of the improved version has changed, it is still a non-intention broadcast supported network. Therefore, the network performance can be kept the same as the previous one.

An example of the initial network for six-core communication is shown in Fig. 1. For simplicity, the topology is shown with five rounded rectangles and several lines with arrows. The rounded rectangle is the ring waveguide. Line pointing to the ring waveguide from modulator represents an auxiliary waveguide and a microresonator for injection. Line pointing to the detector means another auxiliary waveguide and another microresonator for ejection. Multicast and broadcast data coherence communication is enabled by using multi-ring waveguides simultaneously. It is observed that the interference between different ring waveguides is severe in the initial non-optimized network. Cross points are distributed in every ring waveguide non-uniformly. Furthermore, if the number of cores increases, the number of cross points will increase dramatically. In this letter, we focus on the reduction of cross points in the improved ring-based network.

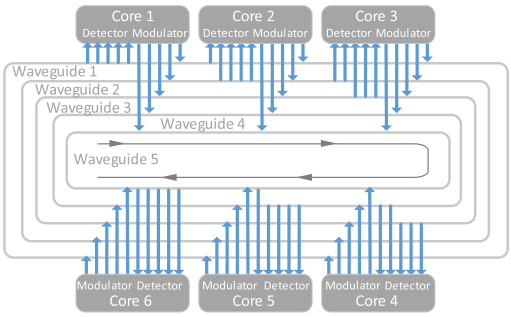


Fig. 1. Non-optimized state of the proposed ring network for six-core communication

As the optimization methodology requires, each ring waveguide, along with the related auxiliary waveguides and microresonators, is divided into several sections. These sections can be classified into two types. One is called the **Injection and Ejection Section (IES)**, and the other is called the **Transmission Section (TS)** (shown in Fig. 2, the arrow in the auxiliary waveguide is omitted for simplicity).

An IES is responsible for a core's messages injection or ejection to a specific ring waveguide. It contains several microresonators, auxiliary waveguides and part of the related ring waveguide. Considering the function of an IES, it can be represented by two subscripts: the core's id and the waveguide index. $IES_{i,j}$ means the IES is used for $core_i$'s messages injection and ejection to the jth waveguide. Observing Fig. 1, the number of microresonators in each IES is different. For example, $IES_{1,1}$ contains 6 microresonators in which 5 are used for ejection and one is used for injection. The number of microresonators in each IES can be expressed into a matrix and we refer this matrix to be the *IES configuration matrix*. For an N-core system, the size of the matrix will be $N \times N - 1$. The total number of microresonators in $IES_{i,j}$ is $Num_{i,j}$ which is one of the elements in the *IES configuration matrix*. A TS is used for connecting two adjacent IESs and it only includes part of a ring waveguide. A TS can be represented as TS_i which means it is used to connect $IES_{i,j}$ and $IES_{i-1,j}$. It can be observed that waveguide cross points are influenced by both IESs and TSs.

For an N-core system, N cores' interfaces will be placed at the optical layer. A circle called the dimension boundary is formed by connecting all interfaces. The area inside the dimension boundary is called the *inner dimension area*, and that outside the dimension boundary is called the *outer dimension area*. The dimension areas will be further divided into several subareas because of the placing of IESs. Subareas are used to decide the next IES's placement location. It should be noted that the concept of subarea is only valid when placing IESs that serve the same core's communication. Fig. 2 shows the inner and outer dimension areas and the subareas. Two IESs for Interface_m are placed and the outer dimension area is separated into 3 subareas by these two IESs. When it comes to Interface_1, the outer dimension area is divided into two subareas by one IES. The framework of the methodology is shown in Algorithm 1. It should be noted that IESs are placed before TSs. A TS will be generated only if the two IESs that it connects with are both be placed. Overall, the optimization process can be divided into several steps.

Step 1: Select a ring waveguide. The maximum element in the *IES configuration matrix* will be chosen and the column id of this maximum element will indicate the to be placed ring waveguide at this time. After finishing optimizing a ring waveguide, all elements in the respective column will be set to zero. The placement sequence of the remainder of waveguides is generated based on the same principle. When another ring waveguide is to be placed, another search for the largest element in this matrix is performed anew.

Step 2: Decide the selection sequence of IESs in a ring waveguide. After a ring waveguide is selected based on **step 1**, IESs that belong to this waveguide will be sorted and placed according to the $Num_{i,j}$ in descending order. If two or more elements are determined to be equal during the sorting, the IES located next to the already placed IES has a higher priority during the selection. Otherwise, the elements will be selected randomly. To fully use the dimension sources, the first and second selected ring waveguide will be placed in the outer dimension and inner dimension areas respectively. Therefore, the two ring waveguide will not cause any cross points.

Step 3: Determine which area or subarea an IES should be placed. We refer $\mathrm{IES}_{i,j}^{next}$ as the IES that needs to be placed next. $\mathrm{IES}_{m,n}^{k}$ refers to the kth IES that has been placed. The total number of placed IESs for core_m's communication is K_m. There will be $K+2$ subareas that are needed to be considered when placing the $\mathrm{IES}_{m,j}^{next}$. These subareas are formed by all placed $\mathrm{IES}_{m,n}^{k}$, $\mathrm{k}=1,2,\ldots,\mathrm{K}_m$, and the inner and outer dimension area boundary. An *impact factor* named $\mathrm{F}_{m,j}$ is defined based on Eqs. 1, 2 and 3. In Eq. 1, since the cross points generated in TSs will influence both two ring waveguides, when calculating the impact factor, a coefficient 2 is added before this TS term in Eq. 1. In Eq. 2, $CP(IES_{m,j}^{next}, IES_{m,n_k}^{k})$ is used to calculate the cross points when $\mathrm{IES}_{m,j}^{next}$ interferes with IES_{m,n_k}^{k}. The sum of $CP(IES_{m,j}^{next}, IES_{m,n_k}^{k})$ shows the total number of cross points caused by the IES to be placed and the placed IESs. Equation 3 shows the cross points induced by TSs' interference. Unlike an IES, a TS is formed between two adjacent IESs. Therefore, $\mathrm{TS}_{m+l,j}$ refers to the transmission section that connects $\mathrm{IES}_{m+l,j}$ and $\mathrm{IES}_{m+l-1,j}$. $CP(TS_{m+l,j}, TS_{m+l,n_k})$ shows the number of cross points formed by the interference between the already placed ring waveguide's TSs and the to-be-placed ring waveguide's TS. In Equation 3, the interference might occur on both the left and right sides of $\mathrm{IES}_{m,j}^{next}$. If $\mathrm{IES}_{m+1,j}$ or $\mathrm{IES}_{m-1,j}$ has not been placed yet, the cross points related with the $\mathrm{IES}_{m+1,j}$ or $\mathrm{IES}_{m-1,j}$ will be regarded as zero.

The subarea with the lowest impact factor will be chosen to place the $\mathrm{IES}_{m,j}^{next}$. The cross points induced by both IES and TS will be considered. It should be noted that as the cross points in the TS will influence two ring waveguides; thus, the number of cross points in TS is doubled during the calculation.

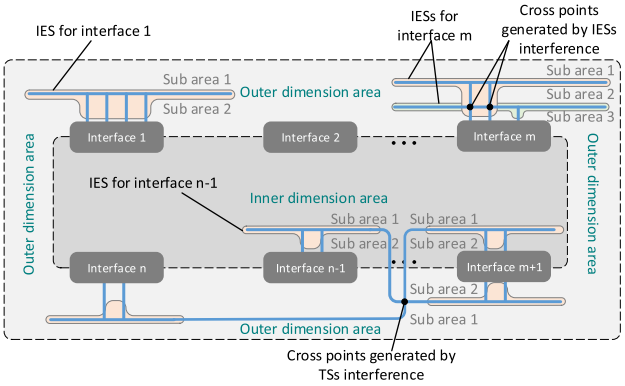


Fig. 2. Dimension area, IES and TS

$$F_{m,j}^{subarea} = CrossPoint_{IES} + 2 \times CrossPoints_{TS} \quad (1)$$

$$CrossPoint_{IES} = \sum_{k=1}^{K_m} CP(IES_{m,j}^{next}, IES_{m,n_k}^{k}) \quad (2)$$

$$CrossPoint_{TS} = \sum_{l=0}^{1} \sum_{k=1}^{K_m} CP(TS_{m+l,j}, TS_{m+l,n_k}) \quad (3)$$

Algorithm 1 Ring-based network layout optimization algorithm

$N \leftarrow$ *Number of Cores*(*Interfaces*)
$S[N][N-1] \leftarrow$ *IES Configuration Matrix*
$M[N][N-1] \leftarrow 0$ {records the already placed IESs}
{Set two flags to test whether IESs have been placed in inner or outer dimension area}
InnerFlag$[N] \leftarrow 0$
OutterFlag$[N] \leftarrow 0$
for $i = 0$ to $N-2$ **do**
  repeat
    compare values in $S[N][N-1]$
  until find the maximum element $\mathrm{Num}_{a,b}$
  for $i = 0$ to $N-1$ **do**
    WaveguideIES$[i] \leftarrow S[i][b]$
  end for
  for $i = 0$ to $N-1$ **do**
    repeat
      compare values in WaveguideIES$[N]$
    until find the maximum element WaveguideIES[w] in WaveguideIES[N]
    if InnerFlag[w] == 0 **then**
      Place $IES_{w,b}$ *in inner dimension area*
      InnerFlag$[w] \leftarrow 1$
      $M[w][b] \leftarrow 1$
      $S[w][b] \leftarrow 0$
      WaveguideIES$[w] \leftarrow 0$
    else if OutterFlag[w] == 0 **then**
      Place $IES_{w,b}$ *in Outter dimension area*
      OutterFlag$[w] \leftarrow 1$
      $M[w][b] \leftarrow 1$
      $S[w][b] \leftarrow 0$
      WaveguideIES$[w] \leftarrow 0$
    else
      if In $\mathrm{waveguide}_b$, IESs next to $\mathrm{IES}_{w,b}$ have not been placed yet **then**
        Iterate all sub areas formed by $IES_{w,i}$,
        s.t. $M[w][i] \neq 0$, $i \in (0, N-2)$
        Select the sub areas that induce the fewest cross points in IES
        $M[w][b] \leftarrow 1$
        $S[w][b] \leftarrow 0$
        WaveguideIES$[w] \leftarrow 0$
      else
        Iterate all sub areas formed by $IES_{a,i}$
        s.t. $M[a][i] \neq 0$, $i \in (0, N-2)$,
        Select the sub areas that induce the fewest cross points in IES and TS
        $M[w][b] \leftarrow 1$
        $S[w][b] \leftarrow 0$
        WaveguideIES$[w] \leftarrow 0$
      end if
    end if
  end for
end for

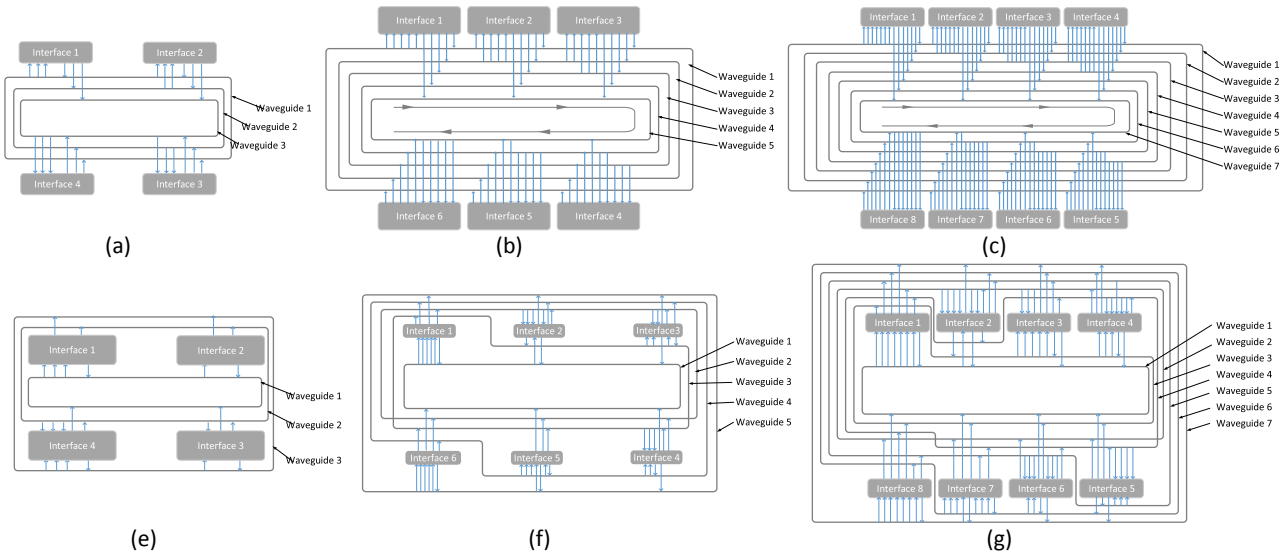


Fig. 3. The proposed non-optimized and optimized ring-based networks for 4-, 6- and 8-core systems. (a), (b) and (c) are non-optimized networks. (e), (f) and (g) are optimized networks.

It is possible that more than one subarea has the lowest impact factor. In this case, the already placed IESs' location will be considered as another decision criterion. Such a criterion tends to place a new $\mathrm{IES}_{m,j}^{next}$ into the subarea where the majority of IESs from $\mathrm{waveguide}_j$ have been placed.

3. Optimization results

In Fig. 3, the optimization results of four-, six- and eight-interface ring-based networks are shown. All optical messages are transmitted clockwise. The network layouts of the non-optimized and optimized networks are compared. Compared to the non-optimized cases, in the optimized cases, the ring waveguides are rearranged and distributed both in the inner and outer dimension area. As the ring waveguides are placed part-by-part according to the IESs and TSs, a single waveguide may be placed in the outer dimension in some parts, and in the inner dimension area in other parts.

The non-optimized and optimized ring-based networks, a typical kind of switch-based network called λ-router and a fat-tree network with an optimized layout [30] will be compared with respect to the total number of cross points. The network size will be set to support 4, 6, and 8 cores' unicast, multicast and broadcast communication without any intention between cores. Therefore, the *lambda*-router and fat-tree networks should be duplicated by several times because the traditional ones cannot support conflict-free multicast and broadcast. It is obvious that additional waveguide cross points will be generated when duplicating and placing the two networks. In order to show the inherent advantage of our proposed networks in multicast and broadcast communication, it is assumed that a 3D dimension layout is deployed. By placing parts of the networks into a different optical layer, there are no additional cross points added when duplicating the λ-router case or fat-tree case. Even under this assumption, the comparison result shows the proposed ring-based networks to have great advantages for supporting data coherence communication.

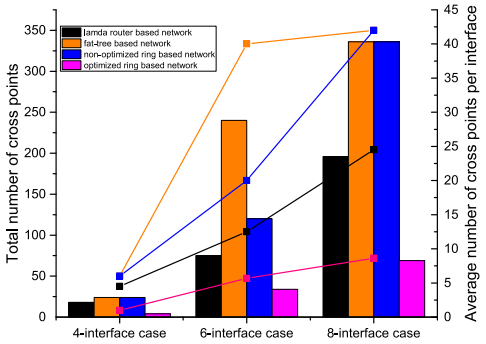
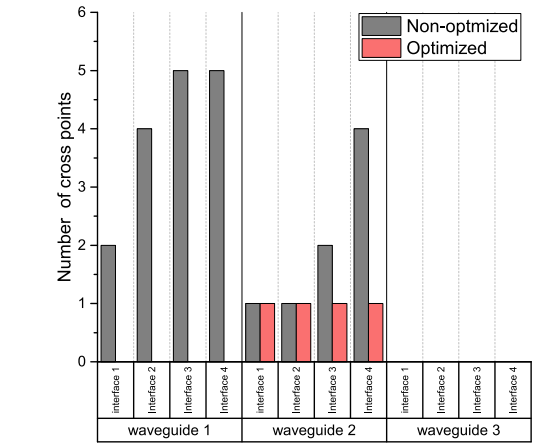


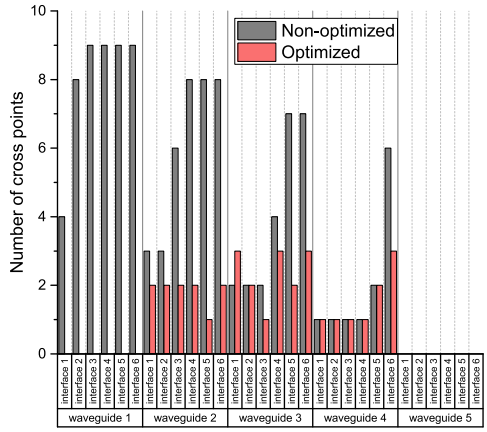
Fig. 4. Comparison of the total number of cross points (the bars) and average number (the curves) of cross points in various networks.

Fig. 4 shows the comparison of the total number of cross points and the average number of cross points per interface in the λ router-based, optimized fat tree-based, non-optimized ring-based, and optimized ring-based networks. Three different network sizes are considered. Due to the scalability defect of the fat tree-based network, if the number of interfaces is between 2^{n-1} and 2^n, to maintain the routing algorithm, the network will be built the same as in the 2^n-interface case. The fat tree-based network shows the worst results for various network scales. The proposed optimized ring-based network performed the best among these four networks regardless of the network scale. Compared to the non-optimized case, the total cross points in 4-, 6- and 8-interface networks are reduced by 83.3%, 71.7%, and 70.2%, respectively. The average cross points per interface in the optimized ring-based network are also lower than in any other cases.

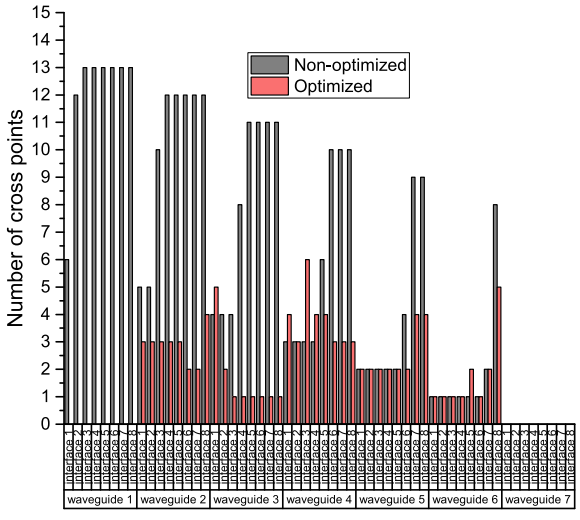
In Fig. 5(a), 5(b) and 5(c), the detailed comparisons of cross points distributions for non-optimized and optimized networks are shown. If the network is non-optimized, a



(a)



(b)



(c)

Fig. 5. Non-optimized and optimized network cross point statistics, including three, five and seven ring waveguide cases shown in sub-figure (a), (b) and (c) respectively.

large number of cross points are distributed in all ring waveguides except the innermost ring waveguide. The total number of cross points in each waveguide is unbalanced. The proportion of cross points in each waveguide is 66.7%, 33.3% and 0% in the four-interface network case. Furthermore, cross points in waveguide$_1$ take up 40% and 28.6% in the 6- and 8-interface cases, respectively. The average cross points per interface per waveguide is 2, 4 and 6 in the non-optimized 4-, 6- and 8-core system cases. This can be explained by the layout shown in Fig. 3. Messages injected into or ejected from the innermost ring waveguide will interfere with all the other waveguides. Therefore, the outermost waveguide suffers from the most severe case of cross points. After the optimization, the proportion of cross points in each waveguide is more uniform, and the total number of cross points is clearly reduced. The average cross points per interface per waveguide is 0.33, 1.33 and 1.79 in the optimized 4-, 6- and 8-core cases.

In addition, in the optimized cases, all cores tend to confront the same number of cross points when sending or receiving messages from the same waveguide. Though in certain cases the number of cross points still varies, the change range is small.

4. Conclusion

In this letter, to further reduce the cross losses in a proposed ring-based on-chip optical network, we propose a waveguide layout optimization methodology to fully utilize the space of the 2D optical plane. The proposed optimization methodology reduces the total cross points in the network and makes the cross points distribution in each waveguide more uniform. By utilizing a hierarchical structure to scale the network up and extending the optimization methodology into 3D with multiple optical layers, this network can support more cores. In summary, the ring-based network and the optimization methodology support the creation of a power-efficient optical network for data coherence communication.

Acknowledgments

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